Double-cell Memory for Plug & Play

EDID Memory

BR24C21/F/FJ/FV, BU9882/F/FV-W

BR24C21/F/FJ/FV

●**Description**

The BR24C21 series ICs are serial EEPROMs that support DDC1™/DDC2™ interfaces for Plug and Play displays.

●**Features**

1) Compatible with both DDC1™/DDC2™
2) Operating voltage range: 2.5V to 5.5V
3) Page write function: 8bytes
4) Low power consumption
   Active (at 5V) : 1.5mA (typ)
   Stand-by (at 5V) : 0.1 μA (typ)
5) Address auto increment function during Read operation
6) Data security
   Write enable feature (VCLK)
   Write protection at low Vcc
7) Various packages available: DIP-T8 / SOP8 / SOP-J8 / SSOP-B8
8) Initial data=FFh
9) Data retention: 10years
10) Rewriting possible up to 100,000 times

●**Absolute maximum ratings** (Ta=25℃)

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc	-0.3～+6.5	V
Power Dissipation	Pd	800 (DIP-T8) *1	mW
		450 (SOP8) *2	
		450 (SOP-J8) *3	
		350 (SSOP-B8) *4	
Storage Temperature	Tstg	-65～+125	℃
Operating Temperature	Topr	-40～+85	℃
Terminal Voltage	-	-0.3～Vcc+0.3	V

* Reduce by 8.0 mW/°C over 25°C (*1), 4.5mW/℃ (*2,3), and 3.5mW/℃ (*4)

●**Recommended operating conditions**

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc	2.5～5.5	V
Input Voltage	VIN	0～Vcc	V

●**Memory cell characteristics**

Parameter	Limits			Unit
	Min.	Typ.	Max.	
Write/Erase Cycle	100,000	-	-	Cycle
Data Retention	10	-	-	Year

●**Electrical characteristics** - DC (Unless otherwise specified, Ta=-40℃～+85℃、Vcc=2.5V～5.5V)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
“H” Input Voltage 1	VIH1	0.7Vcc	—	—	V	SCL, SDA
“L” Input Voltage 1	VIL1	—	—	0.3Vcc	V	SCL, SDA
“H” Input Voltage 2	VIH2	2.0	—	—	V	VCLK
“L” Input Voltage 2	VIL2	—	—	0.8	V	VCLK, Vcc≧4.0V
“L” Input Voltage 3	VIL3	—	—	0.2Vcc	V	VCLK, Vcc＜4.0V
“L” Output Voltage	VOL	—	—	0.4	V	SDA, IOL=3.0mA
Input Leakage Current	ILI	-1	—	1	μA	SCL, VCLK, VIN=0V～Vcc
Output Leakage Current	ILO	-1	—	1	μA	SDA, VOUT=0V～Vcc
Operating Current	ICC	—	—	3.0	mA	Vcc=5.5V, fSCL=400kHz
Standby Current	ISB	—	10	100	μA	Vcc=5.5V, SDA=SCL=Vcc,VCLK=GND *1

Note: This IC is not designed to be radiation-resistant

*1 Transmit-Only Mode - After power on, the BR24C21/F/FJ/FV is in Standby mode and does not provide the clock to the VCLK pin. After the clock is provided to VCLK, the device is switched from Standby to Transmit-Only Mode, and the operating current flows.

Bi-directional Mode - The BR24C21/F/FJ/FV is in Standby mode after each command is performed.

●**Block diagram**

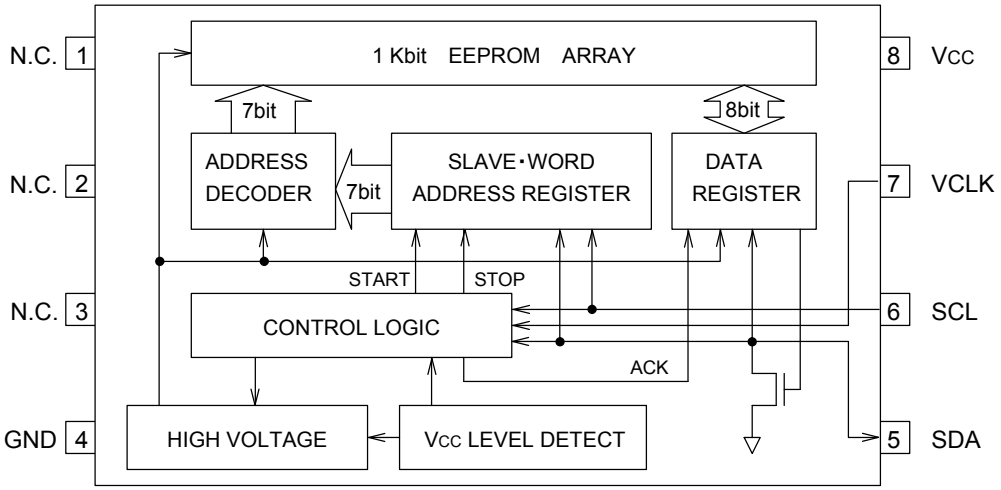


Fig.1 Block Diagram

●**Pin layout diagram**

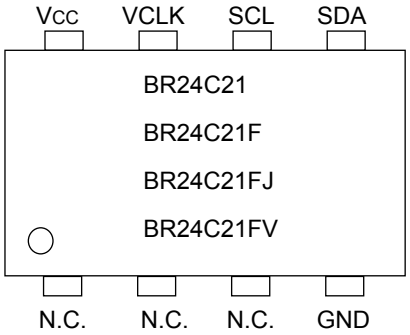


Fig.2 Pin Layout

Pin Name	I/O	Functions
Vcc	—	Power Supply
GND	—	Ground （0V）
N.C.	—	No Connection
SCL	IN	Serial Clock Input for Bi-directional Mode
SDA	IN/OUT	Slave and Word Address, Serial Data Input, Serial Data Output *1
VCLK	IN	Clock Input (Transmit-Only Mode) Write Enable (Bi-directional Mode)

*1 An open drain output requires a pull-up resistor.

●**Electrical characteristics** - AC (Unless otherwise specified, Ta=-40℃～+85℃,Vcc=2.5V～5.5V)

Parameter	Symbol	Fast-mode Vcc=2.5V～5.5V			Standard-mode Vcc=2.5V～5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	fSCL	—	—	400	—	—	100	kHz
Data Clock High Period	tHIGH	0.6	—	—	4.0	—	—	μs
Data Clock Low Period	tLOW	1.3	—	—	4.7	—	—	μs
SDA and SCL Rise Time	tR	—	—	0.3	—	—	1.0	μs
SDA and SCL Fall Time	tF	—	—	0.3	—	—	0.3	μs
Start Condition Hold Time	tHD:STA	0.6	—	—	4.0	—	—	μs
Start Condition Setup Time	tSU:STA	0.6	—	—	4.7	—	—	μs
Input Data Hold Time	tHD:DAT	0	—	—	0	—	—	ns
Input Data Setup Time	tSU:DAT	100	—	—	250	—	—	ns
Output Data Delay Time(SCL)	tPD	—	—	0.9	—	—	3.5	μs
Stop Condition Setup Time	tSU:STO	0.6	—	—	4.0	—	—	μs
Bus Free Time	tBUF	1.3	—	—	4.7	—	—	μs
Write Cycle Time	tWR	—	—	10	—	—	10	ms
Noise Spike Width (SDA and SCL)	tI	—	—	0.1	—	—	0.1	μs
AC OPERATING CHARACTERISTICS (Transmit-Only Mode)								
Output Data Delay Time(VCLK)	tVPD	—	—	1.0	—	—	2.0	μs
VCLK High Period	tVHIGH	0.6	—	—	4.0	—	—	μs
VCLK Low Period	tVLOW	1.3	—	—	4.7	—	—	μs
VCLK Setup Time	tVSU	0	—	—	0	—	—	μs
VCLK Hold Time	tVHD	0.6	—	—	4.0	—	—	μs
Mode Transition Time	tVHZ	—	—	0.5	—	—	1.0	μs
Transmit-Only Powerup Time	tVPU	0	—	—	0	—	—	μs
Noise Spike Width (VCLK)	tVI	—	—	0.1	—	—	0.1	μs

●**Synchronous data timing**

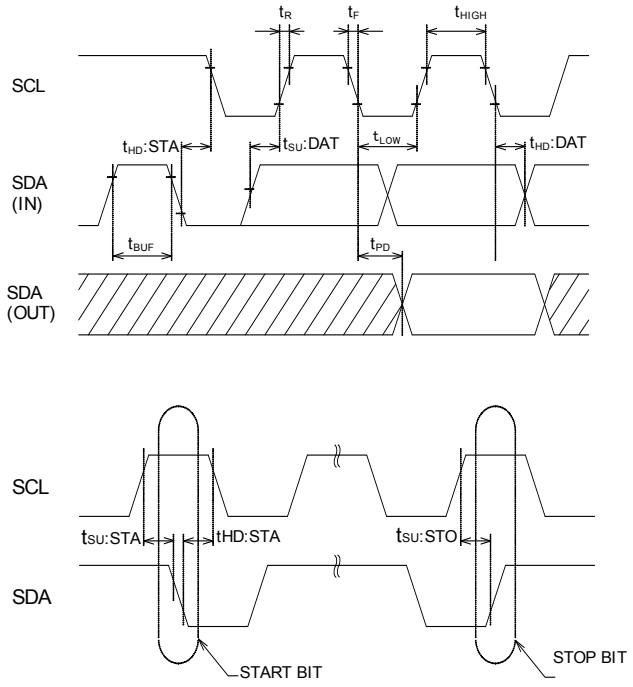


Fig.3 Synchronous Data Timing

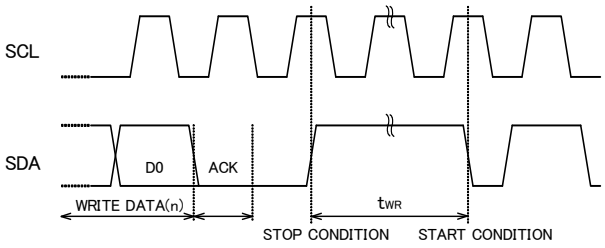


Fig.4 Write Cycle Timing

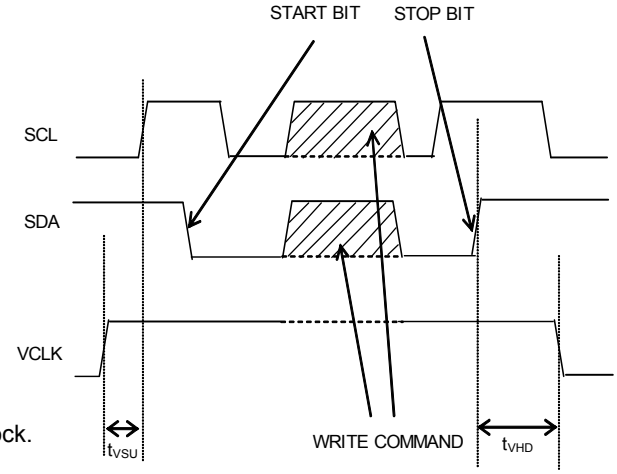


Fig.5 Write Enable Timing

・SDA data is latched into the chip at the rising edge of the SCL clock.

・Output data toggles at the falling edge of the SCL clock.

●Transmit-only mode

・After power is on, the BR24C21/F/FJ/FV is in Transmit-Only Mode. In this mode data can be output by providing the clock to the VCLK pin.

・When the power is on, the SCL pin needs to be set to Vcc(High level).

・SDA is at high-impedance during input of the first 9 clocks. At the 10th rising clock edge of VCLK data is output. After power on, the output data is as follows:

00h address data → 01h address data → 02h address data → ⋯

The address is incremented by one, after every 9 clocks of VCLK. All addresses are output in this mode.
When the counter reaches the last address, the next output data is 00h address data. (See Fig. 6)

・In this mode, the NULL bit (High data) is output between the address data and the next address data. (See Fig. 7)

・The read operation is in Transmit-Only Mode and can be started after the power is stabilized.

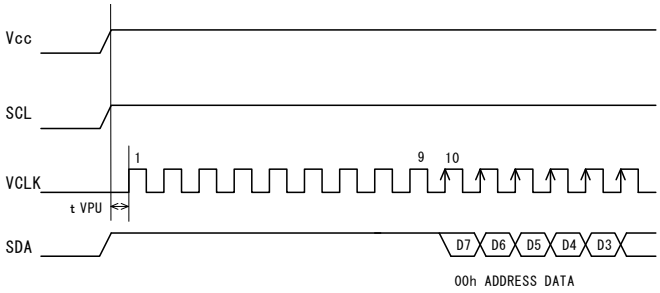


Fig.6 Transmit Only Mode

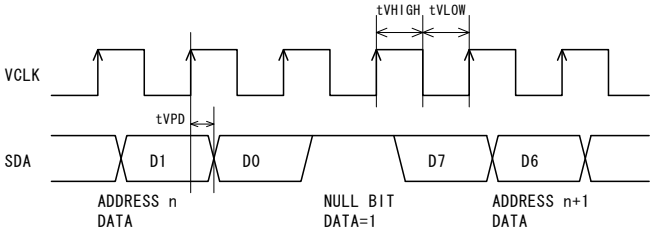


Fig.7 Null Bit

●Bi-directional mode

○Bi-directional Mode and Recovery Function

・The BR24C21/F/FJ/FV can be switched from Transmit-Only Mode to Bi-directional Mode by providing a valid High to Low transition at the SCL pin, while the state of SDA is at high-impedance.

・After a valid high to low transition on the SCL pin, the BR24C21/F/FJ/FV begins to count the VCLK clock. If the VCLK counter reaches 128 clocks without the command for Bi-directional Mode, the device reverts to Transmit-Only Mode (Recovery function). The VCLK counter is reset by providing a valid high to low transition at the SCL pin. After reversal to Transmit-Only Mode the device begins to output data (00h address data) with the 129th rising clock edge of VCLK.

・If the BR24C21/F/FJ/FV is switched from Transmit-Only Mode and receives the command for Bi-directional Mode and responds with an Acknowledge, it is impossible to revert to Transmit-Only Mode. (Power down is the only way to revert to Transmit-Only Mode.) Unless the input device code is “1010”, the device does not respond with an Acknowledge. If the VCLK counter reaches 128 clocks afterwards, it is possible to revert to Transmit-Only Mode for Recovery function. If the Master generates a STOP condition during the Slave address, before an Acknowledge is input, it is possible to revert to Transmit-Only Mode.

・When the device is switched from Transmit-Only Mode to Bi-direction Mode, the period of tVHZ needs to be held.

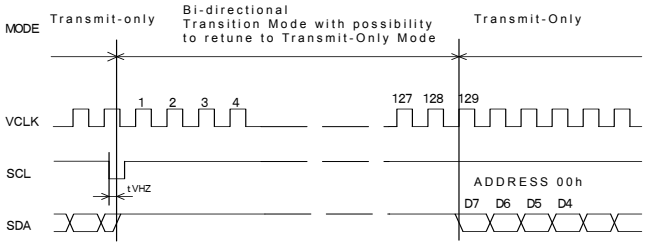


Fig.8 Recovery Mode

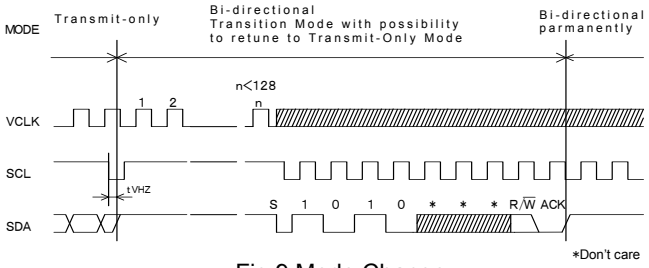


Fig.9 Mode Change

○Bi-directional Mode

START Condition

・All commands are proceeded by the START condition, which is a High to Low transition of SDA when SCL is High.

・The BR24C21/F/FJ/FV continuously monitors the SDA and SCL lines for the START condition and will not respond to any commands until this condition has been met.
(See Fig. 3 Synchronous Data Timing)

STOP Condition

・All commands must be terminated by a STOP condition, which is a Low to High transition of SDA when SCL is High.

・The STOP condition causes the internal write cycle to write data into the memory array after a write sequence.

・The STOP condition is also used to place the device into standby power mode after read sequences.

・A STOP condition can only be issued after the transmitting device has released the bus.
(See Fig.3 Synchronous Data Timing)

Device Addressing

・Following the START condition, the Master outputs the device address of the Slave to be accessed. The most significant four bits of Slave address are the “device type indentifier,” For the BR24C21/F/FJ/FV this is fixed as “1010.”

・The next three bits of the slave address are inconsequential.

・The last bit of the stream determines the operation to be performed. When set to “1”, a READ operation is selected. When set to “0”, a WRITE operation is initiated.

R/$\overline{W}$ set to "0" ・・・・・・・・・ WRITE (This bit is also set to "0" for random read operation)
R/$\overline{W}$ set to "1" ・・・・・・・・・ READ

1010	*	*	*	R/$\overline{W}$

* : Don’t care

○Write Protect Function

・Write Enable (VCLK)

When using the BR24C21/F/FJ/FV in Bi-directional Mode, the VCLK pin can be used as a write enable pin. Setting VCLK High allows normal write operations, while setting VCLK low prevents writing to any location in the array.（See Fig.5 Write Enable Timing）

Changing VCLK from High to Low during the self-timed program operation will not halt programming of the device.

●Bidirectional mode command

○Byte Write

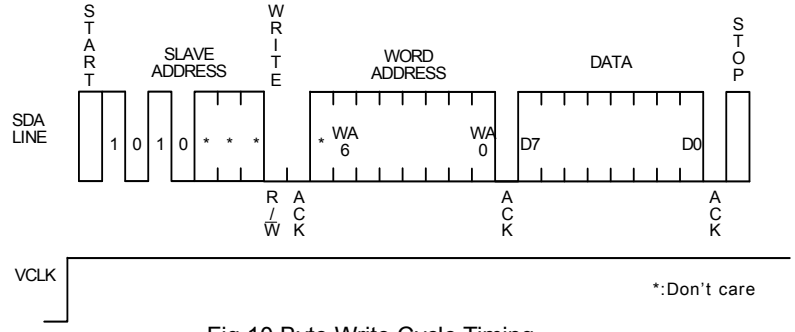


Fig.10 Byte Write Cycle Timing

When the Master generates a STOP condition, the BR24C21/F/FJ/FV begins the internal write cycle to the nonvolatile array.

○Page Write

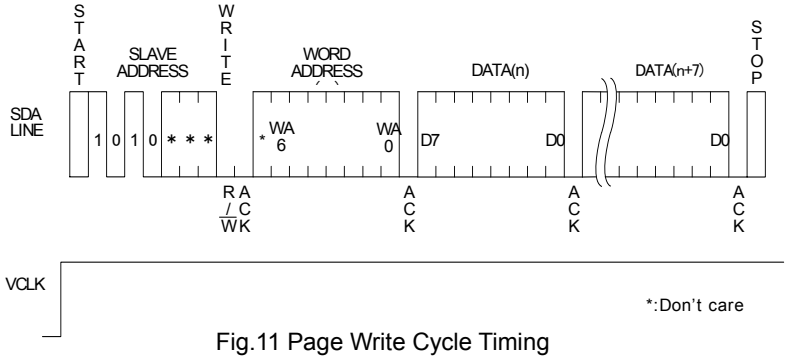


Fig.11 Page Write Cycle Timing

If the Master transmits the next data instead of generating a STOP condition during the byte write cycle, the BR24C21/F/FJ/FV transfers from byte write function to page write function. After receipt of each word, the three lower order address bits are internally incremented by one, while the high order four bits of the word address remains constant.

If the master transmits more than eight words, prior to generating the STOP condition, the address counter will “roll over,” and the previous transmitted data will be overwritten.

○Current Read

The BR24C21/F/FJ/FV contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last accessed address is address “n” in a Read operation, the next Read operation will access data from address “n+1” and increment the current address counter. If the last accessed address is address ”n” in a Write operation, the next Read operation will access data from address “n”. If the Master does not transfer an Acknowledge, but does generate a STOP condition, the current address read operation will only provide a single byte of data. At this point, the device discontinues transmission.

(See Fig.14 Sequential Read Cycle Timing)

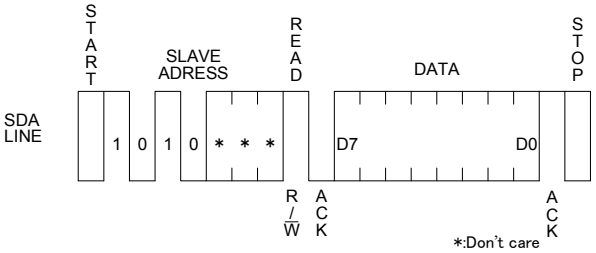


Fig.12 Current Read Cycle Timing

○Random Read

The Random read operation allows the Master to access any memory location. This operation involves a two-step process. First, the Master issues a Write command that includes the START condition and the Slave address field (with R/$\overline{W}$ set to “0”) followed by the word address of the word to be read. This procedure sets the internal address counter of the BR24C21/F/FJ/FV to the desired address. After the word address Acknowledge is received by the Master, the Master immediately re-issues a START condition followed by the Slave address field with R/$\overline{W}$ set to “1.” The device will respond with an Acknowledge and then transmit the 8-data bits stored at the addressed location. If the Master does not acknowledge the transmission but does generate the STOP condition, the IC will discontinue transmission.

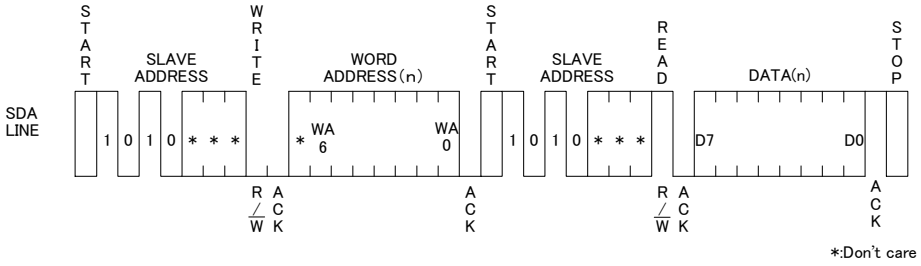


Fig.13 Random Read Cycle Timing

○Sequential Read

- ·If the Master does not transfer an Acknowledge and does not generate a STOP condition during the current Read operation, the BR24C21/F/FJ/FV continues to output the next address data in sequence. For Read operations, all bits in the address counter are incremented, allowing the entire array to be read during a single operation. When the counter reaches the top of the array, it will “roll over” to the bottom of the array and continue to transmit data.
- ·If the Master does not acknowledge the transmission but does generate a STOP condition, at this point the device discontinues transmission.
- ·The sequential Read operation can be performed with both Current Read and Random Read.

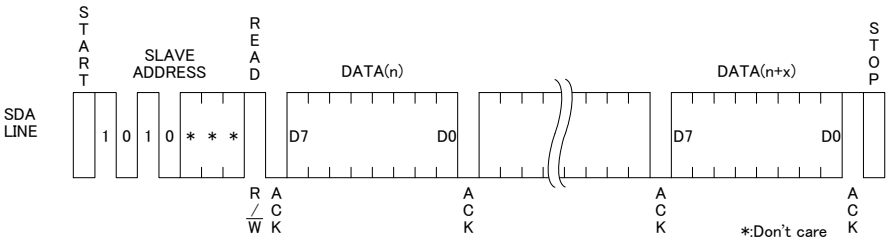


Fig.14 Sequential Read Cycle Timing
(Current Read)

●Description

The BU9882 ICs are dual port EEPROMs compatible with the DDC2™. 2 independent ports allow 2 EDID channels to be read simultaneously.

●Features

1) Designed for use with DDC2™
2) 2-port simultaneous read function
3) Operating voltage range: 2.5V-5.5V
4) Page write function: 8bytes
5) Low power consumption:
   Active (at 5V) : 1.5mA(typ)
   Stand-by (at 5V) : 0.1μA(typ)
6) Data security
   Write protection with $\overline{WP}$
   Write protection at low power supply voltage
7) Various package types available: DIP14 / SOP14 / SSOP14
8) Initial data: FFh
9) Data retention: 10years
10) Rewriting possible up to 100,000 times

●Absolute maximum ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc	-0.3～+6.5	V
Power Dissipation	Pd	950 (DIP14) *1	mW
		450 (SOP14) *2	
		350 (SSOP14) *3	
Storage Temperature	Tstg	-65～+125	℃
Operating Temperature	Topr	-40～+85	℃
Terminal Voltage	-	-0.3～Vcc+1.0 *4	V

* Reduce by 9.5 mW/℃ over 25℃ (*1), 4.5mW/℃(*2), 3.5mW/℃(*3).

*4 6.8V (Max.)

●Recommended operating conditions

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc	2.5～5.5	V
Input Voltage	VIN	0～Vcc+1.0	V

●Memory cell characteristics

Parameter	Limits			Unit
	Min.	Typ.	Max.	
Write/Erase Cycle	100,000	-	-	Cycle
Data Retention	10	-	-	Year

●Electrical characteristics – DC (Unless otherwise specified, Ta=-40℃～+85℃,Vcc=2.5V～5.5V)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
“H” Input Voltage 1	VIH1	2.0	—	—	V	
“L” Input Voltage 1	VIL1	—	—	0.8	V	Vcc≧4.0V
“L” Input Voltage 2	VIL2	—	—	0.2Vcc	V	Vcc＜4.0V
“L” output Voltage	VOL1	—	—	0.4	V	SDA_PC0/1, IOL=3.0mA * 1
Input Leakage Current 1	ILI1	-1	—	1	μA	SCL_PC0/1,DDCENA, BANKSEL, VIN=0V～Vcc+1.0
Input Leakage Current 2	ILI2	-1	—	50	μA	$\overline{WP}$
Output Leakage Current	ILO	-1	—	1	μA	SDA_PC0/1,SCL/SDA_MON(DDCENA=GND), VOUT=0V～Vcc+1.0
Operating Current	ICC	—	1.5	3.0	mA	fSCL=400kHz, Vcc=5.5V tWR=10ms
Standby Current	ISB	—	0.1	5	μA	SCL/SDA_PC0/1=Vcc SCL/SDA_MON=H-Z DDCENA=WPB=BANKSEL=GND DUALPCB=Vcc

Note: This IC is not designed to be radiation-resistant

*1 IOL at monitor mode (DDCENA＝HIGH) is the sum of current flowing from the pull up resistor at the SDA_MON side to the pull up resistance at SDA_PC0/PC1

●**Block diagram**

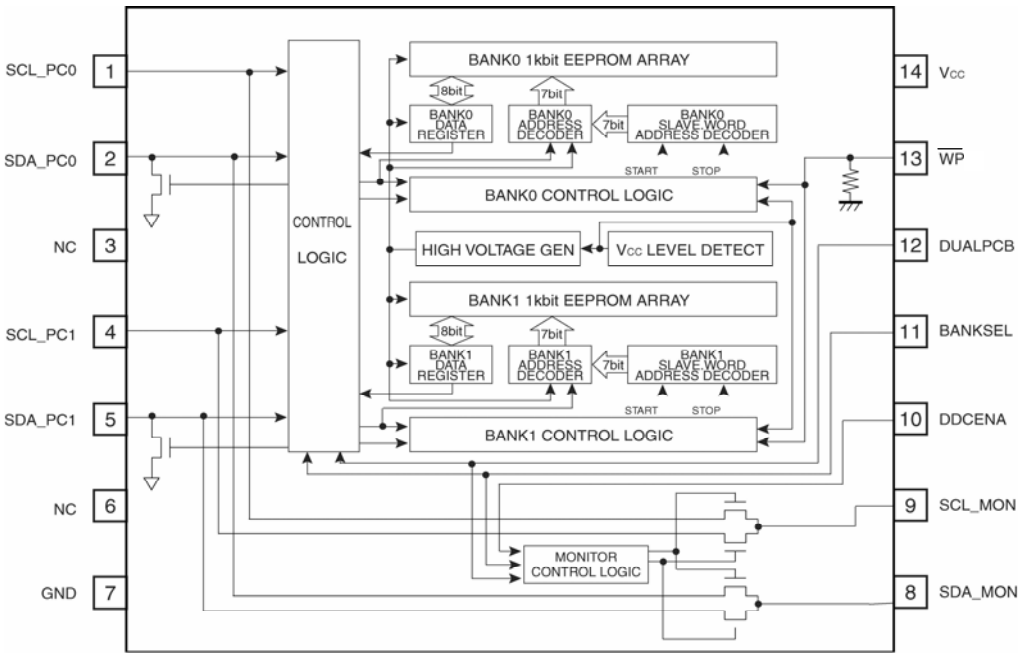


Fig.15 Block Diagram

●**Pin layout diagram**

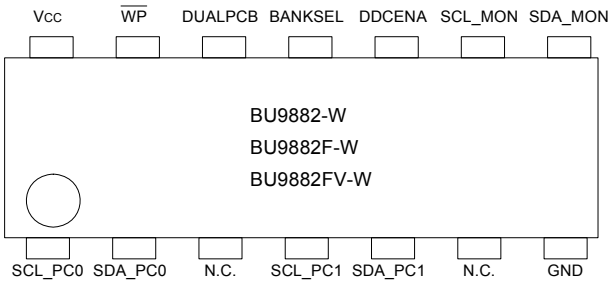


Fig.16 Pin Layout

●**Pin description**

Pin Name	I/O	Functions
Vcc	−	Power Supply
GND	−	Ground （0V）
N.C.	−	No Connection
SCL_PC0	IN	Serial Clock Input, Access to BANK0 at DUAL PORT mode Access to BANK0 or to BANK1 at SINGLE PORT mode
SDA_PC0	IN/OUT	Slave and Word Address Serial Data Input, Serial Data Output Access to BANK0 at DUAL PORT mode, Access to BANK0 or to BANK1 at SINGLE PORT mode
SCL_PC1	IN	Serial Clock Input Access to BANK1 at DUAL PORT mode, Don't Care at SINGLE PORT mode
SDA_PC1	IN/OUT	Slave and Word Address Serial Data Input, Serial Data Output Access to BANK1 at DUAL PORT mode, Don't Care at SINGLE PORT mode
SCL_MON	OUT	Serial Clock Output Connected to SCL_PC0/1 at DDCENA="High", "Hi-Z" output at DDCENA="Low"
SDA_MON	OUT	Slave and Word Address Serial Data Output Connected to SCL_PC0/1 DDCENA="High", "Hi-Z" output at DDCENA="Low"
DDCENA	IN	Control of SCL_MON, SDA_MON
BANKSEL	IN	Select a SCL/SDA_MON Connected Port at DUAL PORT mode Selected a BANK at SINGLE PORT mode
DUALPCB	IN	Control of DUAL PORT/SINGLE PORT mode
$\overline{WP}$	IN	Write Protect Control

An open drain output requires a pull-up resistor.

●**Electrical characteristics** – AC (Unless otherwise specified, Ta=-40℃～+85℃、Vcc=2.5V～5.5V)

Parameter	Symbol	Fast-mode Vcc=2.5V～5.5V			Standard-mode Vcc=2.5V～5.5V			Unit Typ.
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	fSCL	–	–	400	–	–	100	kHz
Data Clock High Period	tHIGH	0.6	–	–	4.0	–	–	μs
Data Clock Low Period	tLOW	1.3	–	–	4.7	–	–	μs
SDA and SCL Rise Time	tR	–	–	0.3	–	–	1.0	μs
SDA and SCL Fall Time	tF	–	–	0.3	–	–	0.3	μs
Start Condition Hold Time	tHD:STA	0.6	–	–	4.0	–	–	μs
Start Condition Setup Time	tSU:STA	0.6	–	–	4.7	–	–	μs
Input Data Hold Time	tHD:DAT	0	–	–	0	–	–	ns
Input Data Setup Time	tSU:DAT	100	–	–	250	–	–	ns
Output Data Delay Time(SCL)	tPD	–	–	0.9	–	–	3.5	μs
Stop Condition Setup Time	tSU:STO	0.6	–	–	4.0	–	–	μs
Bus Free Time	tBUF	1.3	–	–	4.7	–	–	μs
Write Cycle Time	tWR	–	–	10	–	–	10	ms
Noise Spike Width (SDA and SCL)	tI	–	–	0.1	–	–	0.1	μs

●**Synchronous data timing**

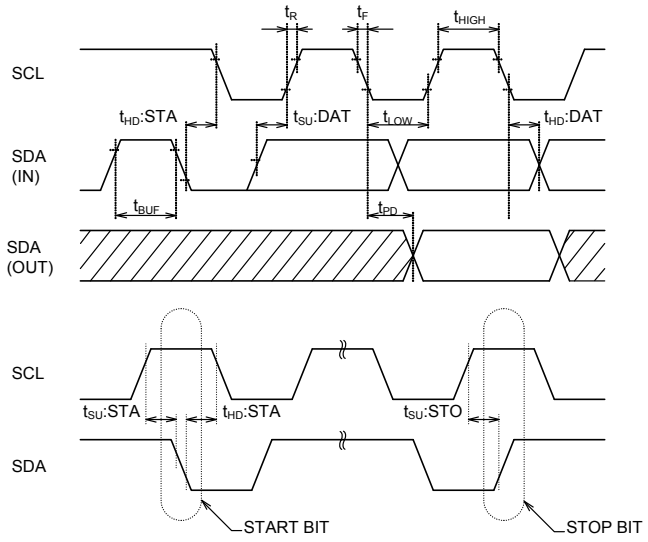


Fig.17 Synchronous Data Timing

●**Write cycle timing**

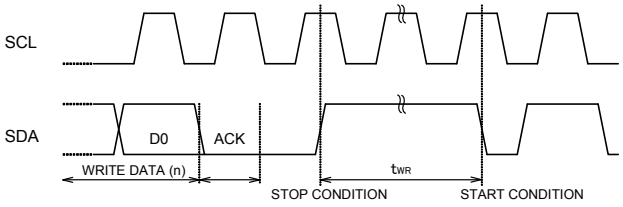


Fig.18 Write Cycle Timing

・SDA data is latched into the chip at the rising edge of the SCL clock.

・The output date toggles at the falling edge of the SCL clock.

●**Operation notes**

○DDCENA Operation

When DDCENA is set to High, SCL_PC0/1 and SDA_PC0/1 will be connected to SCL_MON and SDA_MON, respectively. Therefore, monitoring of the communications between the PC and EEPROM, and the communications of the MONITOR and PC, is possible.

Selection of PC0/PC1 is determined according to the state of the DUALPCB and BANKSEL inputs.

When DDCENA is Low, the SCL/SDA_MON output is set to "Hi-Z".

DUALPCB	BANKSEL	SCL_MON,SDA_MON (CONNECTION PORT)
Low (DUAL PORT)	Low	PC0 PORT
	High	PC1 PORT
High (SINGLE PORT)	Low	PC0 PORT
	High	

○BANKSEL

BANKSEL serves as an input for connection port of SCL/SDA_MON during DUAL PORT mode.
It turns into the BANK selection terminal of internal memory in SINGLE PORT mode.
Only the PC0 port can access the memory in SINGLE PORT mode.

DUALPCB	BANKSEL	CONNECTION BANK
Low (DUAL PORT)	Low	PC0 PORT : BANK0
	High	PC1 PORT : BANK1
High (SINGL PORT)	Low	BANK0
	High	BANK1

○$\overline{WP}$

When $\overline{WP}$=Low, all data at all addresses are write-protected. The terminal has a built-in pull down resister. Make sure that $\overline{WP}$=High when writing data.
Utilize this function in order to prevent incorrect write command input from the PC, as well as incorrect input during communication between the PC and monitor.

○Data Read

The data read function allows simultaneous read from SCL_PC0/1, SDA_PC0/1 in DUAL PORT mode.

○Data Write

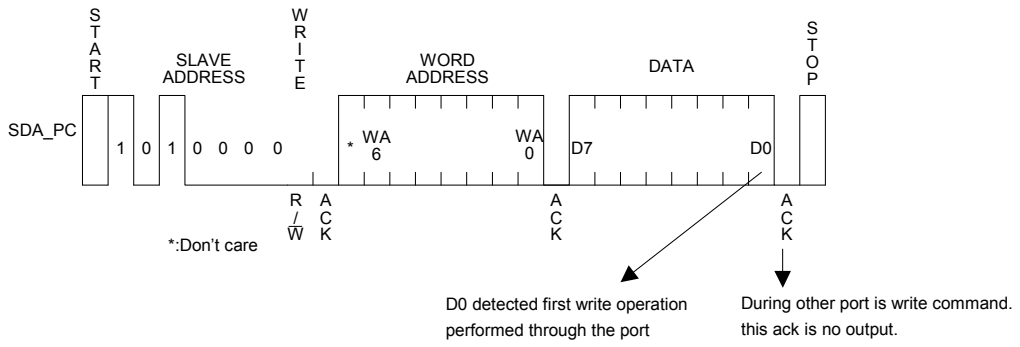


Fig.19 Write Cycle Timing

Write operation is performed using either PC0/1 (SCL or SDA) even when accessed simultaneously in DUAL PORT mode. Port selection is made by detecting the data D0 of the first byte of the WRITE command input.
After this, the other port is made unavailable for both READ and WRITE commands until the write operation is completed.

○START Condition

All commands are preceeded by the START condition, which is a High to Low transition of SDA when SCL is High. This IC continuously monitors the SDA and SCL lines for the START condition and will not respond to any commands until this condition has been met.

○STOP Condition

All commands must be terminated by a STOP condition, which is a Low to High transition of SDA when SCL is HIGH. (See Fig.17)

○WRITE Command

Unless a STOP condition is executed, the data will not be written into the memory array.

○DEVICE ADDRESSING

Following a START condition, the Master outputs the device address of the slave to be accessed.
The most significant four bits of the Slave address are the "device type indentifier".
For the IC this is fixed as "1010".
The next three bits are "000".
The last bit of the stream determines the operation to be performed.
When set to "1", Read operation is selected ; when set to "0", Write operation is selected.

R/$\overline{W}$ set to "0" ・・・・・・・・・ WRITE
R/$\overline{W}$ set to "1" ・・・・・・・・・ READ

1010	0	0	0	R/$\overline{W}$

●Commands

○Byte Write

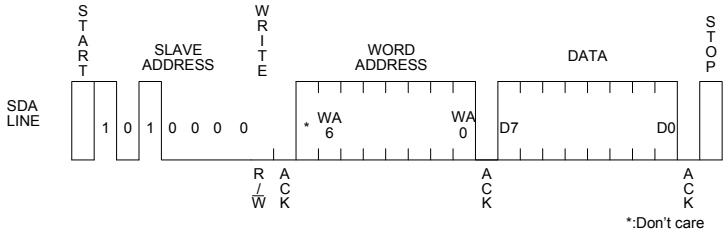


Fig.20 Byte Write Cycle Timing

When the Master generates a STOP condition, the IC begins an internal write cycle to the nonvolatile array.

○Page Write

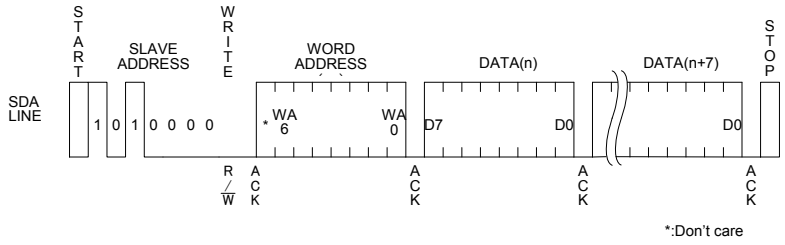


Fig.21 Page Write Cycle Timing

After the receipt of each word, the three low order address bits are internally increased by one. The four higher order bits of the address(WA6～WA3) remain constant. This IC is capable of eight byte page write operation.

If the master transnmits more than eight words, prior to generating the STOP condition, the address counter will "roll over", and the previous transmitted data will be overwritten.

○Current Read

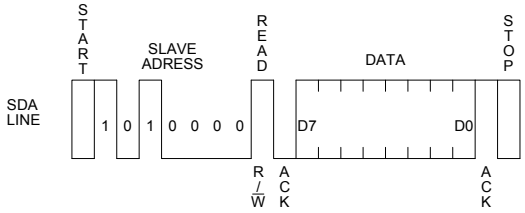


Fig.22 Current Read Cycle Timing

In case the previous operation is random or current read (which includes sequential read), the internal address counter is increased by one from the last acceseed address (n). Thus current read outputs the data of the next word address (n+1).

If the last command is byte or page write, the internal address stays at the last address(n). Thus current read outputs the data of the word address (n).

If the master does not transfer the Acknowledge, but does generate a stop condition, the current address read operation only provides a single byte of data.

At this point, the BU9882/F/FV-W discontinues transmission.

○Random Read

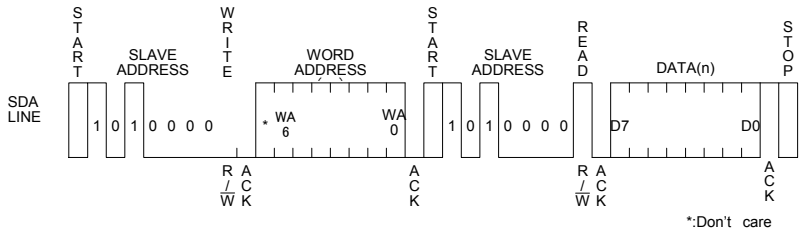


Fig.23 Random Read Cycle Timing

Random read operation allows the master to access any location.

If the master does not transfer the Acknowledge but does generate a stop condition, the current address read operation only provides a single byte of data. (At 1Kbit all address read possible).

This communication must be terminated by a stop condition, which is a Low to High transition of SDA when SCL is High.

○Sequential Read

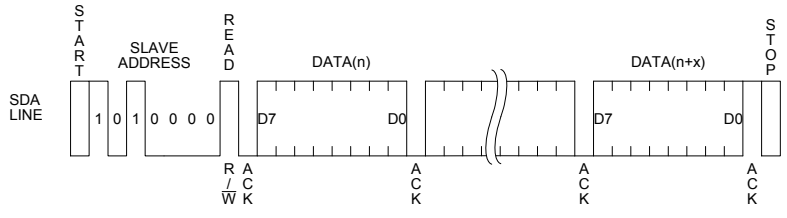


Fig.24 Sequential Read Cycle Timing

During the Current read operation, if an Acknowledge is detected, and no STOP condition is generated by the master(μ-COM), the device will continue to transmit the data. (It can transmit all data(1Kbit 128word)). If an Acknowledge is not detected, the devive will terminate further data transmissions and await a STOP condition before returning to the standby mode. The Sequential Read operation can be performed with both Current Read and Random Read.

●Peripheral Circuits

○DUAL PORT

DUAL PORTs are used to connect two PCs to one monitor. PC0 is connected to BANK0 and PC1 to BANK1. Each bank operates as 1Kbit EEPROM.

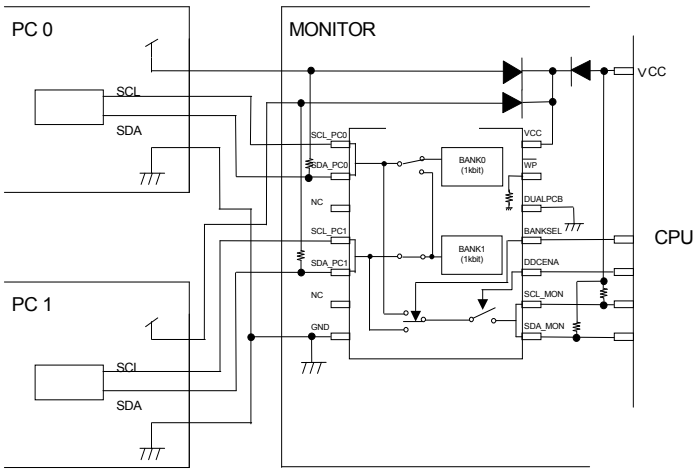


Fig.25 Example of Peripheral Circuit with Dual Port

○ To Use DUAL PORT

Start the operation of the DUAL PORT by following the instructions below:

1. Set the DUAL PCB to LOW with neither of the ports being operated by commands.
2. Input the command from PC0 or PC1.

○ Simultaneous Access

<READ OPERATION>

EEPROM data read allows simultaneous access from PC0, PC1 ports.

<WRITE OPERATION>

Write operation is performed for either of PC0/1 even when accessed simultaneously from both. Port selection is made by detecting the data D0 of the first byte of the WRITE command input. Write operation is performed only for the port where D0 of the first byte of the write data is detected first.

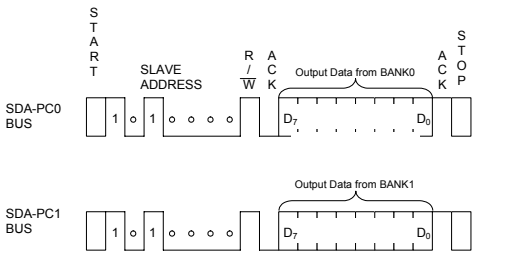


Fig.26 Simultaneous Access of Read Operation

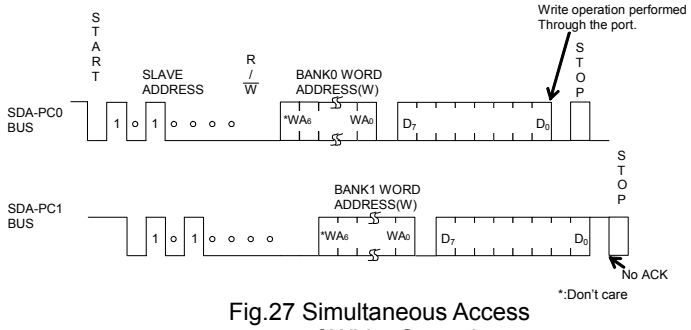


Fig.27 Simultaneous Access of White Operation

○MONITOR OUTPUT

BU9882/F/FV-W has a monitor output terminal. This allows communication between the PC and monitor CPU. The monitor output for the use of DUAL PORT can be switched with BANKSEL input, as shown in the table below.

BANKSEL input	SCL_MON,SDA_MON connection port
Low	PC0 PORT
High	PC1 PORT

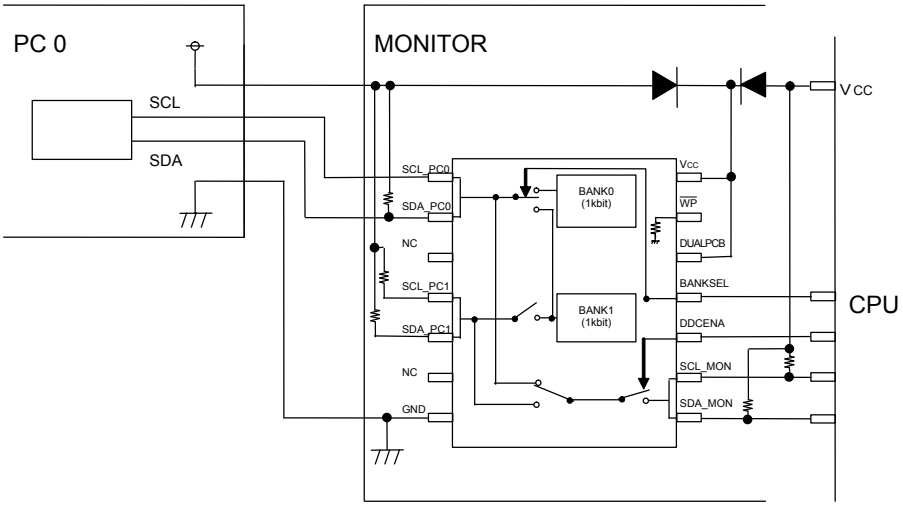


Fig.28 Example of Peripheral Circuit with Single Port

○ SINGLE PORT

SINGLE PORT is for connecting one PC to one monitor. In this case, it is accessible only from PC0. BANK selection is made with BANKSEL. Switching this BANKSEL allows access to the total of 2kbit EEPROM, with BANK0 and BANK1, from PC0.

○ To use SINGLE PORT

Start the SINGLE PORT operation by following the instructions below:

1. Set the DUAL PCB to High with neither of the ports being operated by commands.
2. Select the BANK with BANKSEL.
3. Input the command from PC0.

Common Application Note

●Software Reset

Execute software reset in case the device is at an unexpected state after power up and/or the command input needs to be reset. The following figures (Fig.29-(a), Fig.29-(b), Fig.29-(c))

During dummy clock, please release SDA BUS (tied to Vcc by pull up resistor).

During that time, the device may pull the SDA line Low for acknowledge or outputting read data. If the master controls the SDA line High, it will conflict with the device output Low then it makes a current overload. It may cause instantaneous power down and may damage the device.

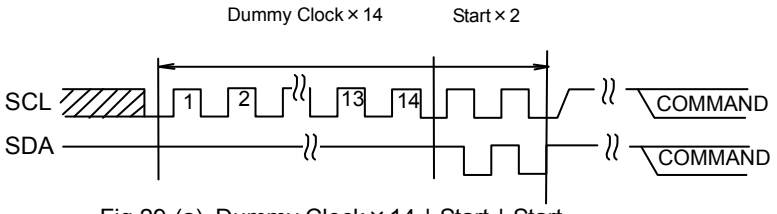


Fig.29-(a) Dummy Clock × 14 + Start + Start

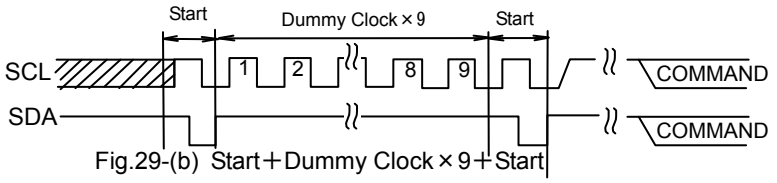


Fig.29-(b) Start + Dummy Clock × 9 + Start

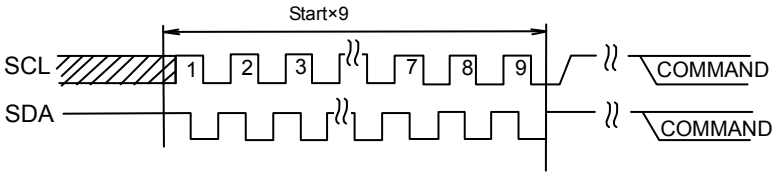


Fig.29-(c) Start × 9

●Acknowledge Polling

Since the device ignores all input commands during the internal write cycle, no ACK will be returned. When the master sends the next command following the write command, and the device returns the ACK, it means that the program is completed. If no ACK is returned, it means that the device is still busy. By using Acknowledge polling, the waiting time is minimized to less than tWR=5ms. To prevent operating Write or Current Read immediately after Write, first send the slave address (R/$\overline{W}$ is "High" or "Low"). After the device returns the ACK, continue word address input or data output, respectively.

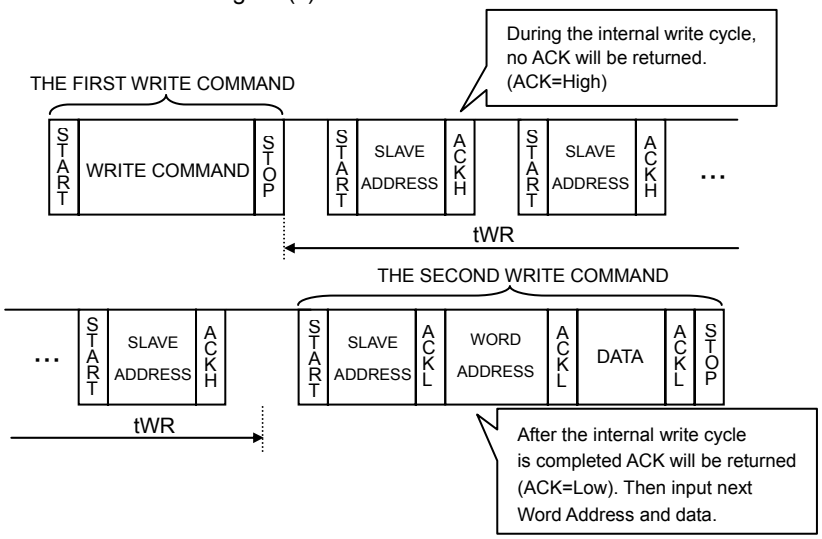


Fig.30 Successive Write Operation By Acknowledge Polling

●Command Cancellation By Start And Stop Condition

During a command input, command is canceled by the successive inputs of start condition and stop condition (Fig.31). However, during ACK or data output, the device may output the SDA line Low. In such cases, operation of start and stop condition is impossible, making the reset inoperable. Execute the software reset in the cases. (Fig.29)

Operating the command cancel by start and stop condition during the command of Random Read or Sequential Read or Current Read, internal address counter is not confirmed. Therefore operation of Current Read after this is not valid. Operate a Random Read in this case.

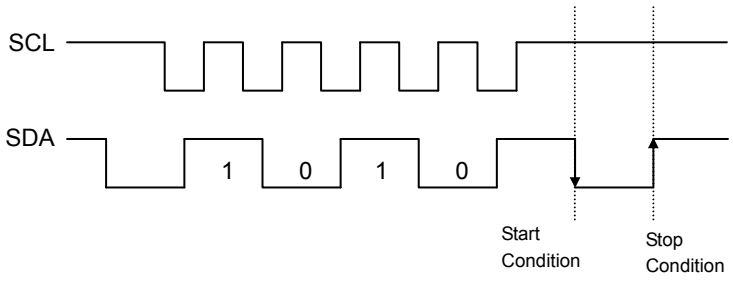


Fig.31 Command Cancellation

●I/O Circuit

○SDA Pin Pull-up Resister

The pull up resister is needed because SDA is NMOS open drain. Choose the correct value of this resister(R_{PU}), by considering VIL, IL characteristics of a controller which control the device and VOH, IOL characteristics of the device. If large R_{PU} is chosen, clock frequency needs to be slow. In case of small R_{PU}, the operating current increases.

○Maximum Rpu

Maximum value of R_{PU} is determined by following factors:

①SDA rise time determined by R_{PU} and the capacitance of bus line(CBUS) must be less than tR.
Other timing must keep the conditions of AC spec.

②When SDA bus is High, the voltage Ⓐ of SDA bus determined by a total input leak(IL) of the all devices connected to the bus. R_{PU} must be significantly higher than the High level input of a controller and the device, including a noise margin 0.2V_{CC}.

$V_{CC} - IL R_{PU} - 0.2\,V_{CC} \geqq V_{IH}$

$$\therefore \quad R_{PU} \leqq \frac{0.8V_{CC} - V_{IH}}{IL}$$

Examples: When V_{CC}=3V IL=10μA VIH=0.7V_{CC}

According to ②

$$R_{PU} \leqq \frac{0.8\times3 - 0.7\times3}{10\times10^{-6}}$$

$$\leqq 300\ [k\Omega]$$

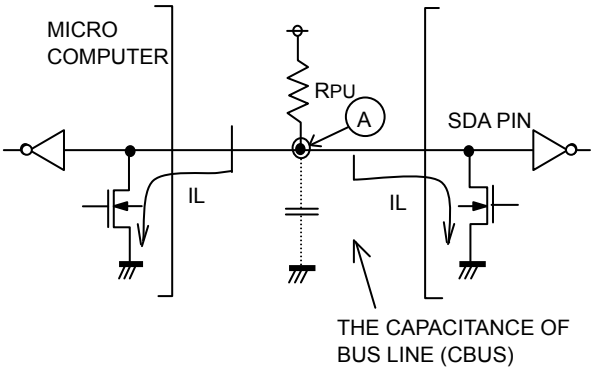


Fig.32 I/O Circuits

○Minimum R_{PU}

The minimum value of R_{PU} is determined by following factors:

①Meets the condition that V_{OLMAX}=0.4V, I_{OLMAX}=3mA when the output is Low.

$$\frac{V_{CC} - V_{OL}}{R_{PU}} \leqq I_{OL}$$

$$\therefore \quad R_{PU} \geqq \frac{V_{CC} - V_{OL}}{I_{OL}}$$

② V_{OLMAX}=0.4V must be lower than the input Low level of the microcontroller and the EEPROM including the recommended noise margin of 0.1V_{CC}.

VOLMAX ≦ VIL-0.1 V_{CC}

Examples: V_{CC}=3V, VOL=0.4V, IOL=3mA, the VIL of the controller and the EEPROM is VIL=0.3V_{CC},

According to ① $R_{PU} \geqq \frac{3-0.4}{3\times10^{-3}}$

$$\geqq 867\ [\Omega]$$

and VOL=0.4 [V]

VIL=0.3×3

=0.9 [V]

so that condition② is met

○SCL Pin Pull-up Resister

When SCL is controlled by the CMOS output the pull-up resistor at SCL is not required.
However, should SCL be set to Hi-Z, connection of a pull-up resistor between SCL and V_{CC} is recommended.
Several kΩ are recommended for the pull-up resistor in order to drive the output port of the microcontroller.

●Notes For Power Supply

VCC rises through the low voltage region in which the internal circuit of the IC and the controller are unstable. Therefore, the device may not work properly due to an incomplete reset of the internal circuit. To prevent this, the device has a P.O.R. and LVCC feature. At power up, maintain the following conditions to ensure functions of P.O.R and LVCC.

1. "SDA='H'" and "SCL='L' or 'H'".
2. Follow the recommended conditions of tR, tOFF, Vbot for the P.O.R. function during power up.

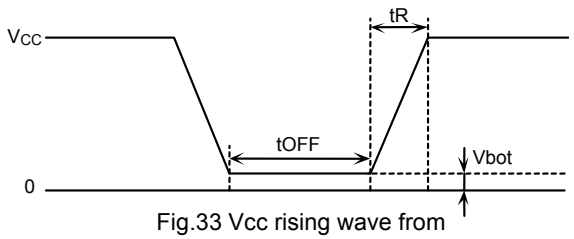


Fig.33 Vcc rising wave from

Recommended conditions of tR, tOFF, Vbot

tR	tOFF	Vbot
Below 10ms	Above 10ms	Below 0.3V
Below 100ms	Above 10ms	Below 0.2V

3. Prevent SDA and SCL from being "Hi-Z".
   In case conditions 1 and/or 2 cannot be met, take following actions:
   A) If unable to keep condition 1 (SDA is "Low" during power up):
   →Control SDA ,SCL to be "High" as shown in figure below.

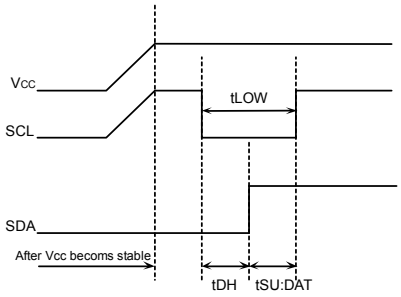


Fig.34 SCL="H" and SDA="L"

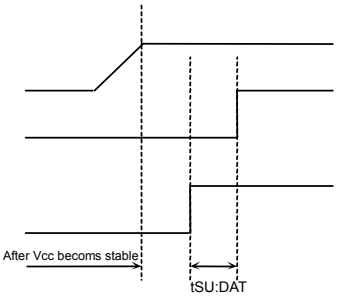


Fig.35 SCL="L" and SDA="L"

   B) If unable to keep condition 2.
   →After power becomes stable, execute software reset. (See Fig.29)
   C) If unable to keep both conditions 1 and 2.
   →Follow the instruction A first, then the instruction B.

●LVcc Circuit

LVCC circuit inhibits write operation at low voltage, and prevents an inadvertent write. Write operation is inhibited below the LVCC voltage (Typ.=1.2V).

●Vcc NOISE

○Bypass Condenser

Noise and surges on power line may cause abnormal function. It is recommended that the bypass condensers (0.1μF) are attached on the Vcc and GND line beside the device. It is also recommended to attach bypass condensers on the board close to the connector.

●Caution On Use

1) Described numeric values and data are design representative values, and the values are not guaranteed.
2) We believe that application circuit examples are recommendable, however, in actual use, confirm characteristics further sufficiently. In the case of use by changing the fixed number of external parts, make your decision with sufficient margin in consideration of static characteristics and transition characteristics and fluctuations of external parts and our LSI.
3) Absolute maximum ratings
   If the absolute maximum ratings such as impressed voltage and operating temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.
4) GND electric potential
   Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltages is lower than that of GND terminal.
5) Heat design
   In consideration of permissible dissipation in actual use condition, carry out heat design with sufficient margin.
6) Terminal to terminal shortcircuit and wrong packaging
   When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of shortcircuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.
7) Use in a strong electromagnetic field may cause malfunction, therefore, evaluated design sufficiently.

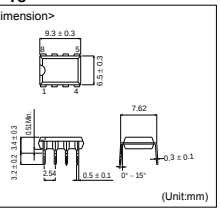
●Selection of order type

BR	24	C	21	/F/FJ/FV	—	E2
ROHM type name	BUS type 24:I²C	Product type C:2.5V Version	Capacity 21=1k	Package type Blank:DIP-T8 F:SOP8 FJ:SOP-J8 FV:SSOP-B8		Package specifications Blank:Tube(only for DIP) E2:Embossed carrier tape

BU	9882	/F/FV	—	W	E2
ROHM type name	Product No	Package type Blank:DIP14 F:SOP14 FV:SSOP-B14		Double cell	Package specifications Blank:Tube(only for DIP) E2:Embossed carrier tape

DIP-T8

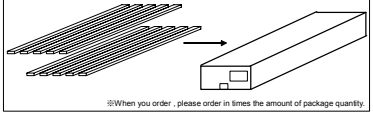
<Dimension>



(Unit:mm)

<Packing information>

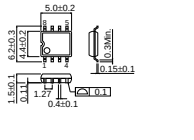
Container	Tube
Quantity	2000pcs
Direction of feed	Direction of products is fixed in a container tube.



※When you order , please order in times the amount of package quantity.

SOP8

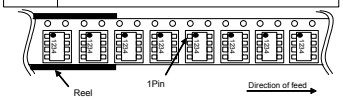
<Dimension>



(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

SOP-J8

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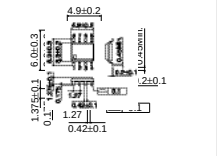
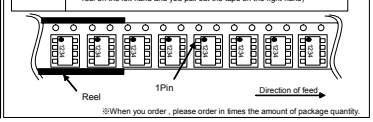


(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

SSOP-B8

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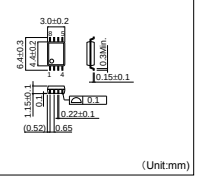

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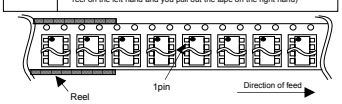
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

DIP14

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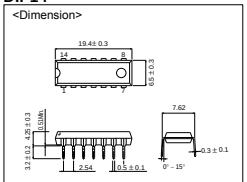
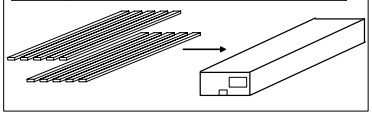


(Unit:mm)

<Packing information>

Container	Tube
Quantity	1000pcs
Direction of feed	Direction of products is fixed in a container tube.



SOP14

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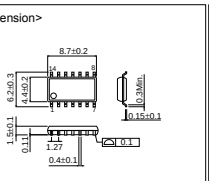
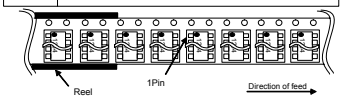


(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

SSOP-B14

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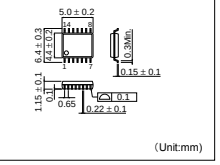

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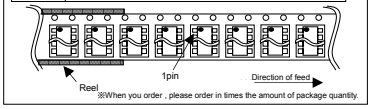
Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



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