TECHNICAL NOTE

Single-chip built-in FET type Switching Regulator Series

High Efficiency Step-down Switching Regulator

BD9141MUV

●Description

ROHM's high efficiency step-down switching regulator BD9141MUV is a power supply designed to produce a low voltage including 5.0/3.3 volts from 2 lithium cell power supply line. Offers high efficiency with our original pulse skip control technology and synchronous rectifier. Employs a current mode control system to provide faster transient response to sudden change in load.

●Features

1) Offers fast transient response with current mode PWM control system.
2) Offers highly efficiency for all load range with synchronous rectifier (Nch/Pch FET) and SLLM (Simple Light Load Mode)
3) Incorporates soft-start function.
4) Incorporates thermal protection and ULVO functions.
5) Incorporates short-current protection circuit with time delay function.
6) Incorporates shutdown function
7) Employs small surface mount package : VQFN020V4040

●Use

Power supply for LSI including DSP, Micro computer and ASIC

●Line up

Parameter	Symbol	Limits	Unit
		BD9141MUV	
VCC Voltage	VCC	-0.3～+15 [*1]	V
PVCC Voltage	PVCC	-0.3～+15 [*1]	V
EN Voltage	VEN	-0.3～+15	V
SW,ITH Voltage,VREG	VSW,VITH, VREG	-0.3～+15	V
Power Dissipation 1	Pd1	0.34[*2]	W
Power Dissipation 2	Pd2	0.70[*3]	W
Power Dissipation 3	Pd3	2.21 [*4]	W
Power Dissipation 4	Pd4	3.56 [*5]	W
Operating temperature range	Topr	-40～+105	℃
Storage temperature range	Tstg	-55～+150	℃
Maximum junction temperature	Tjmax	+150	℃

[*1] Pd should not be exceeded.
[*2] IC only.
[*3] 1 layer, mounted on a board 74.2mm×74.2mm×1.6mm Glass-epoxy PCB (Copper foil area : 10.29mm^2)
[*4] 4 layers, mounted on a board 74.2mm×74.2mm×1.6mm Glass-epoxy PCB
(1st ,4th Copper foil area : 10.29mm^2 2nd ,3rd Copper foil area : 5505mm^2) ,.
[*5] 4 layers, mounted on a board 74.2mm×74.2mm×1.6mm Glass-epoxy PCB (Copper foil area : 5505mm^2) , copper foil in each layers.

●Operating Conditions (Ta=-40～+105℃)

Parameter	Symbol	BD9141MUV			Unit
		Min.	Typ.	Max.	
VCC Voltage	VCC [*6]	4.5[*7]	8.0	13.2	V
PVCC Voltage	PVCC [*6]	4.5[*7]	8.0	13.2	V
EN Voltage	VEN	0	-	VCC	V
SW average output current	Isw [*6]	-	-	2.0	A
Output voltage Setting Range	VOUT[*7]	2.5	-	6.0	V

[*6] Pd should not be exceeded.
[*7] VccMin. = Vout + 1.3V.

★ This product is under development. Any information is possible to be changed.

Jul.2008

●Electrical Characteristics

◎BD9141MUV (Ta=25℃, V_{CC}=PV_{CC}=8.0V, EN=V_{CC}, R_1=8.2kΩ, R_2=43kΩ, unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Standby current	I_{STB}	-	0	10	μA	EN=GND
Bias current	I_{CC}	-	300	500	μA	
EN Low voltage	V_{ENL}	-	GND	0.8	V	Standby mode
EN High voltage	V_{ENH}	2.0	V_{CC}	-	V	Active mode
EN input current	I_{EN}	-	1.6	10	μA	V_{EN}=8V
Oscillation frequency	F_{OSC}	400	500	600	KHz	
Pch FET ON resistance	R_{ONP}	-	150	300	mΩ	PV_{CC}=8V
Nch FET ON resistance	R_{ONN}	-	80	160	mΩ	PV_{CC}=8V
ADJ Voltage	V_{ADJ}	0.788	0.800	0.812	V	
ITH sink current	I_{THSI}	10	20	-	μA	V_{ADJ}=1.0V
ITH source current	I_{THSO}	10	20	-	μA	V_{ADJ}=0.6V
UVLO threshold voltage	V_{UVLO1}	3.90	4.10	4.30	V	V_{CC}=8V→0V
UVLO release voltage	V_{UVLO2}	3.95	4.20	4.50	V	V_{CC}=0V→8V
Soft start time	T_{SS}	0.5	1	2	ms	
Timer latch time	T_{LATCH}	1	2	3	ms	SCP/TSD operated
Output Short circuit Threshold Voltage	V_{SCP}	-	0.4	0.56	V	V_{ADJ}=0.8V→0V

●Block Diagram, Application Circuit

【BD9141MUV】

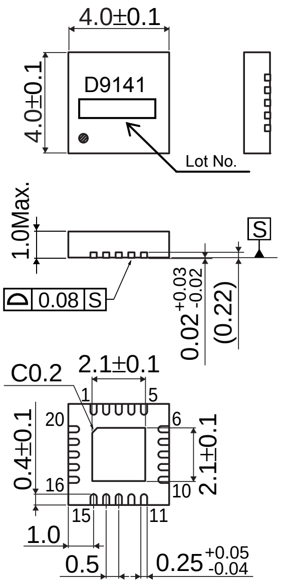


Fig.1 BD9141MUV View

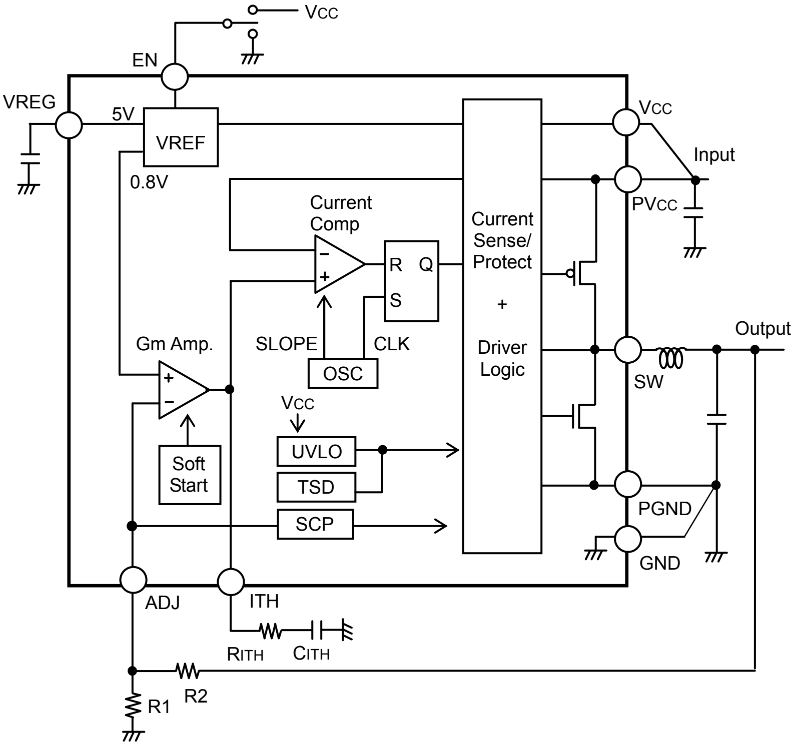


Fig.2 BD9141MUV Block Diagram

●Pin No. & function table

Pin No.	BD9141MUV	
	Pin Name	Pin Function
1,2,3,4,5	SW	Pch/Nch FET drain output pin
6,7,8	PV_{CC}	Pch FET source pin
9	N.C.	Non connection
10	Vcc	VCC power supply input pin
11	GND	Ground
12	ADJ	Output voltage detect pin
13	ITH	GmAmp output pin/Connected phase compensation capacitor
14	VREG	Reference Voltage
15,16	N.C.	Non connection
17	EN	Enable pin(Active High)
18,19,20	PGND	Nch FET source pin

●Characteristics data【BD9141MUV】

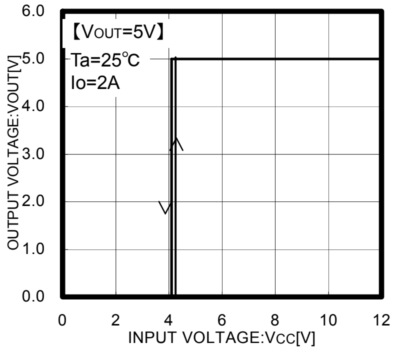


Fig.3 VCC-VOUT

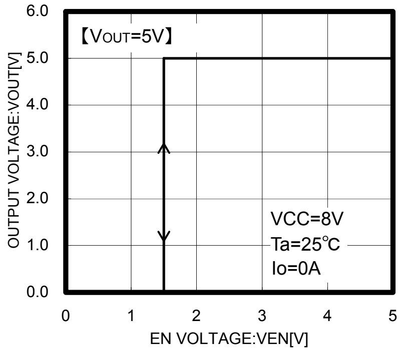


Fig.4 VEN-VOUT

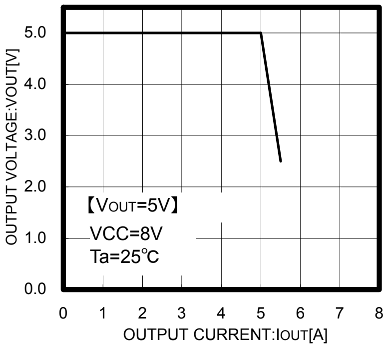


Fig.5 IOUT-VOUT

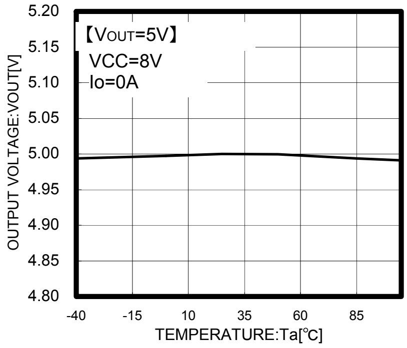


Fig. 6 Ta-VOUT

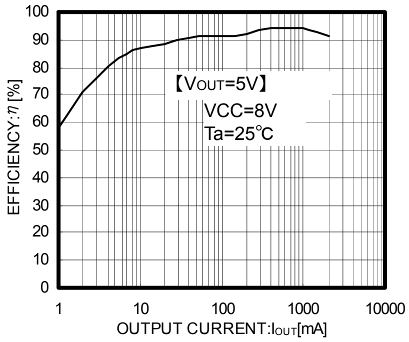


Fig.7 Efficiency

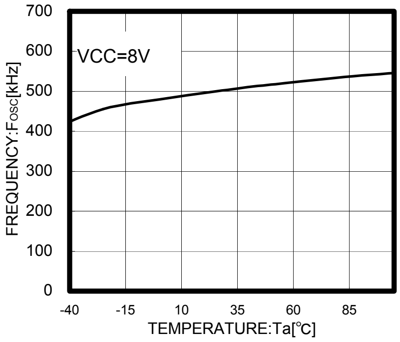


Fig.8 Ta-FOSC

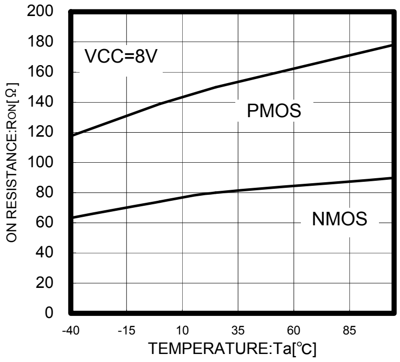


Fig.9 Ta-RONN, RONP

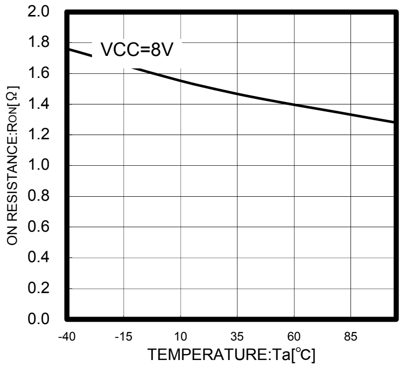


Fig.10 Ta-VEN

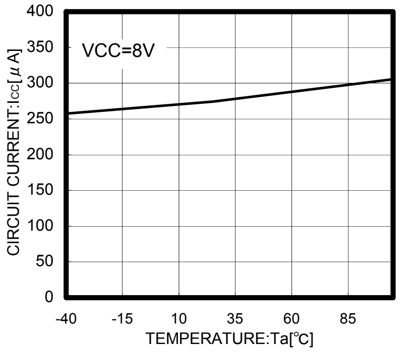


Fig.11 Ta-Icc

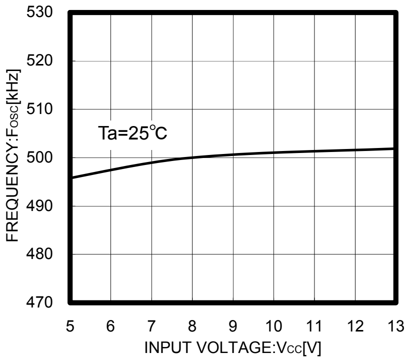


Fig.12 VCC-FOSC

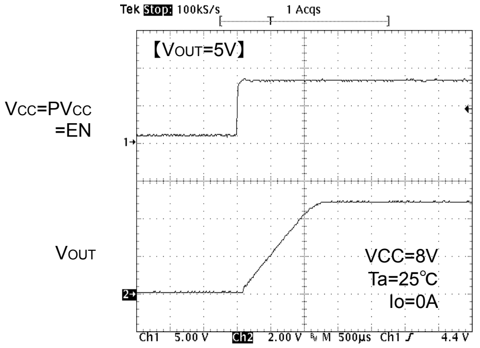


Fig.13 Soft start waveform

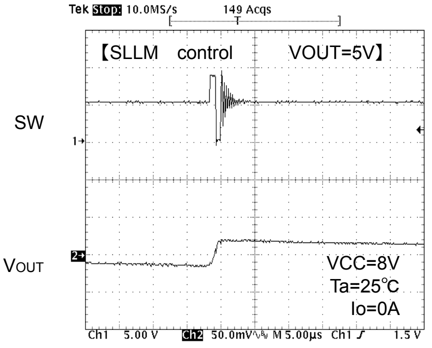


Fig.14 SW waveform Io=10mA

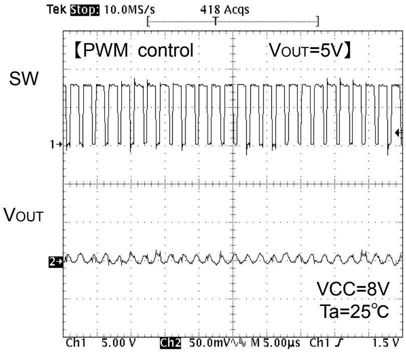


Fig.15 SW waveform Io=2000mA

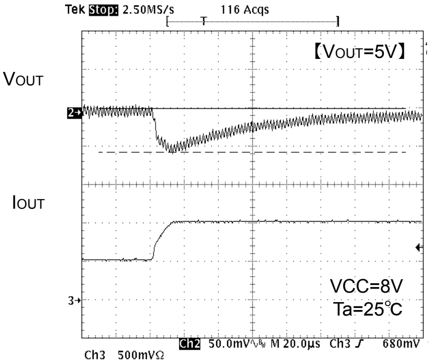


Fig. 16Transient response
Io=0.5A→1A(10μs)

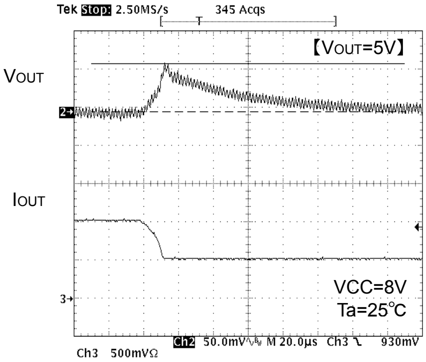
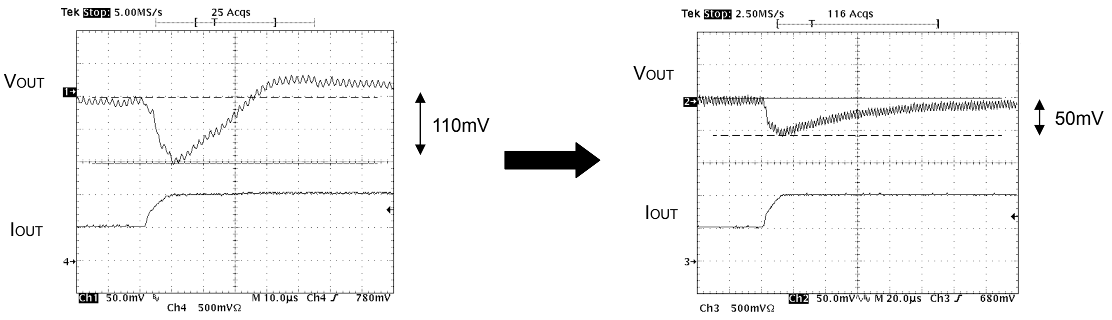


Fig.17 Transient response
Io=1A→0.5A(10μs)

●Information on advantages

Advantage 1 : Offers fast transient response with current mode control system.



Conventional product (Load response Io=0.5A→1A)

BD9141MUV (Load response Io=0.5A→1A)

Voltage drop due to sudden change in load was reduced by about 50%.

Fig.18 Comparison of transient response

Advantage 2 : Offers high efficiency for all load range.

- For lighter load:
  Utilizes the current mode control mode called SLLM for lighter load, which reduces various dissipation such as switching dissipation (P_{SW}), gate charge/discharge dissipation, ESR dissipation of output capacitor (P_{ESR}) and on-resistance dissipation (P_{RON}) that may otherwise cause degradation in efficiency for lighter load.

Achieves efficiency improvement for lighter load.

- For heavier load:
  Utilizes the synchronous rectifying mode and the low on-resistance MOS FETs incorporated as power transistor.

ON resistance of P-channel MOS FET : 150mΩ(Typ.)
ON resistance of N-channel MOS FET : 80mΩ(Typ.)

Achieves efficiency improvement for heavier load.

Offers high efficiency for all load range with the improvements mentioned above.

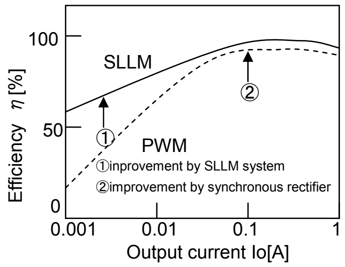


Fig.19 Efficiency

Advantage 3 : ・Supplied in smaller package due to small-sized power MOS FET incorporated.

- Output capacitor Co required for current mode control: 22µF ceramic capacitor
- Inductance L required for the operating frequency of 1MHz: 2.2µH inductor

(BD9141MUV:Co=22µF, L=4.7µH)

Reduces a mounting area required.

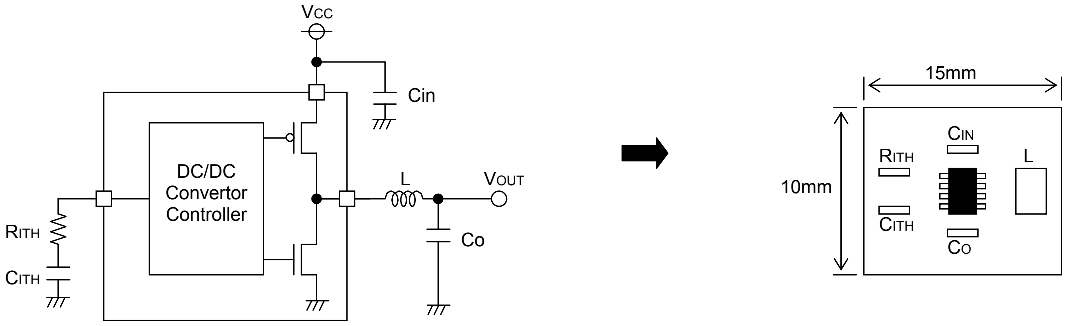


Fig.20 Example application

●Operation

BD9141MUV is a synchronous rectifying step-down switching regulator that achieves faster transient response by employing current mode PWM control system. It utilizes switching operation in PWM (Pulse Width Modulation) mode for heavier load, while it utilizes SLLM (Simple Light Load Mode) operation for lighter load to improve efficiency.

○Synchronous rectifier

It does not require the power to be dissipated by a rectifier externally connected to a conventional DC/DC converter IC, and its P.N junction shoot-through protection circuit limits the shoot-through current during operation, by which the power dissipation of the set is reduced.

○Current mode PWM control

Synthesizes a PWM control signal with a inductor current feedback loop added to the voltage feedback.

・PWM (Pulse Width Modulation) control

The oscillation frequency for PWM is 500kHz. SET signal form OSC turns ON a P-channel MOS FET (while a N-channel MOS FET is turned OFF), and an inductor current I_L increases. The current comparator (Current Comp) receives two signals, a current feedback control signal (SENSE: Voltage converted from I_L) and a voltage feedback control signal (FB), and issues a RESET signal if both input signals are identical to each other, and turns OFF the P-channel MOS FET (while a N-channel MOS FET is turned ON) for the rest of the fixed period. The PWM control repeat this operation.

・SLLM (Simple Light Load Mode) control

When the control mode is shifted from PWM for heavier load to the one for lighter load or vise versa, the switching pulse is designed to turn OFF with the device held operated in normal PWM control loop, which allows linear operation without voltage drop or deterioration in transient response during the mode switching from light load to heavy load or vise versa.

Although the PWM control loop continues to operate with a SET signal from OSC and a RESET signal from Current Comp, it is so designed that the RESET signal is held issued if shifted to the light load mode, with which the switching is tuned OFF and the switching pulses are thinned out under control. Activating the switching intermittently reduces the switching dissipation and improves the efficiency.

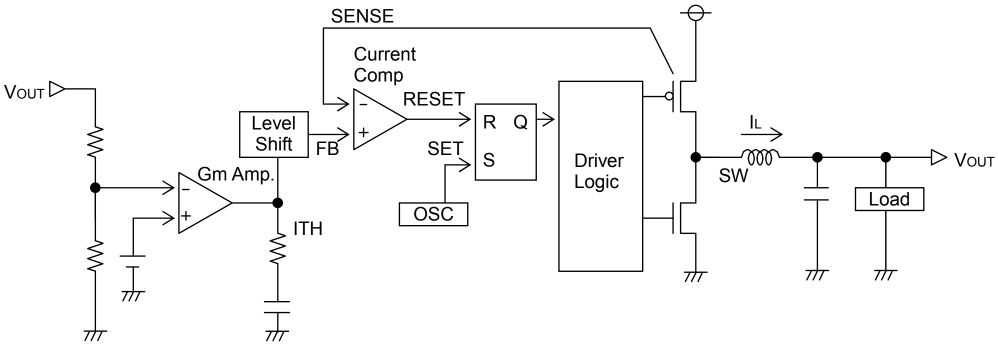


Fig.21 Diagram of current mode PWM control

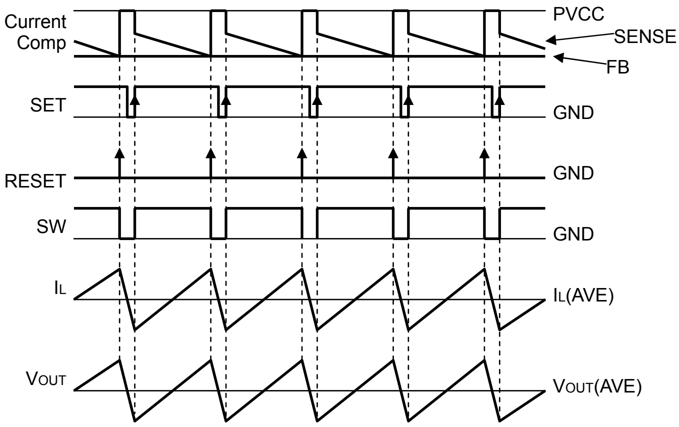


Fig.22 PWM switching timing chart

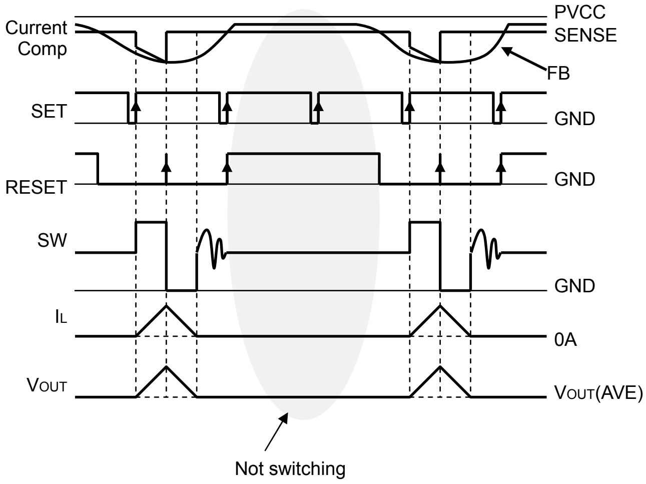


Fig.23 SLLM^{TM} switching timing chart

●Description of operations

・Soft-start function

EN terminal shifted to “High” activates a soft-starter to gradually establish the output voltage with the current limited during startup, by which it is possible to prevent an overshoot of output voltage and an inrush current.

・Shutdown function

With EN terminal shifted to “Low”, the device turns to Standby Mode, and all the function blocks including reference voltage circuit, internal oscillator and drivers are turned to OFF. Circuit current during standby is 0μA (Typ.).

・UVLO function

Detects whether the input voltage sufficient to secure the output voltage of this IC is supplied. And the hysteresis width of 100mV (Typ.) is provided to prevent output chattering.

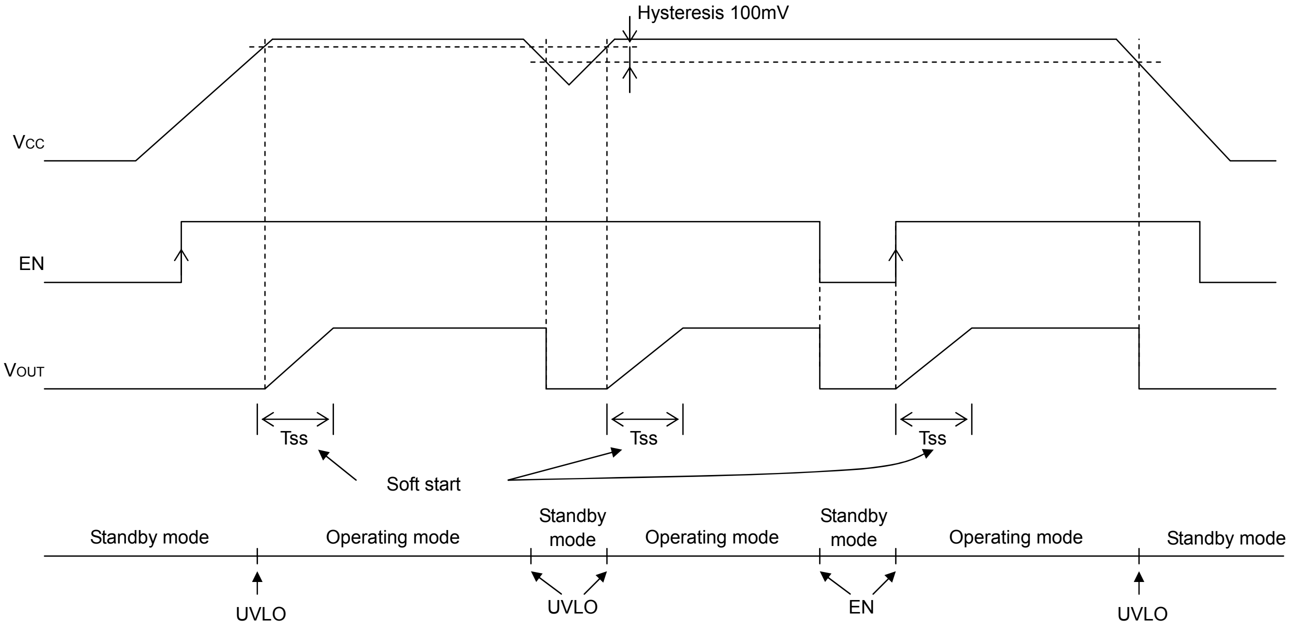


Fig.24 Soft start, Shutdown, UVLO timing chart

・Short-current protection circuit with time delay function

Turns OFF the output to protect the IC from breakdown when the incorporated current limiter is activated continuously for the fixed time(T_{LATCH}) or more.　The output thus held tuned OFF may be recovered by restarting EN or by re-unlocking UVLO.

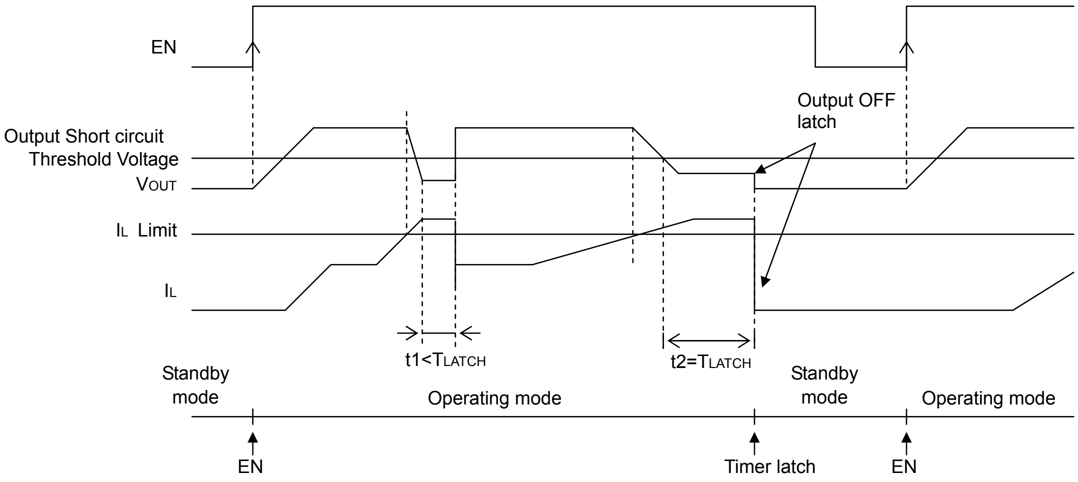


Fig.25 Short-current protection circuit with time delay timing chart

●Switching regulator efficiency

Efficiency η may be expressed by the equation shown below:

$$\eta = \frac{V_{OUT} \times I_{OUT}}{Vin \times Iin} \times 100[\%] = \frac{P_{OUT}}{Pin} \times 100[\%] = \frac{P_{OUT}}{P_{OUT}+P_D\alpha} \times 100[\%]$$

Efficiency may be improved by reducing the switching regulator power dissipation factors $P_D\alpha$ as follows:

Dissipation factors:

1) ON resistance dissipation of inductor and FET：PD(I^2R)
2) Gate charge/discharge dissipation：PD(Gate)
3) Switching dissipation：PD(SW)
4) ESR dissipation of capacitor：PD(ESR)
5) Operating current dissipation of IC：PD(IC)

1)$PD(I^2R)=I_{OUT}^2 \times (R_{COIL}+R_{ON})$　(R_{COIL}[Ω]：DC resistance of inductor, R_{ON}[Ω]：ON resistance of FET, I_{OUT}[A]：Output current.)

2)$PD(Gate)=Cgs \times f \times V$　(Cgs[F]：Gate capacitance of FET、f[H]：Switching frequency、V[V]：Gate driving voltage of FET)

3)$PD(SW)= \frac{Vin^2 \times C_{RSS} \times I_{OUT} \times f}{I_{DRIVE}}$　(C_{RSS}[F]：Reverse transfer capacitance of FET、I_{DRIVE}[A]：Peak current of gate.)

4)$PD(ESR)=I_{RMS}^2 \times ESR$　(I_{RMS}[A]：Ripple current of capacitor、ESR[Ω]：Equivalent series resistance.)

5)$PD(IC)=Vin \times I_{CC}$　(I_{CC}[A]：Circuit current.)

●Consideration on permissible dissipation and heat generation

As this IC functions with high efficiency without significant heat generation in most applications, no special consideration is needed on permissible dissipation or heat generation. In case of extreme conditions, however, including lower input voltage, higher output voltage, heavier load, and/or higher temperature, the permissible dissipation and/or heat generation must be carefully considered.

For dissipation, only conduction losses due to DC resistance of inductor and ON resistance of FET are considered. Because the conduction losses are considered to play the leading role among other dissipation mentioned above including gate charge/discharge dissipation and switching dissipation.

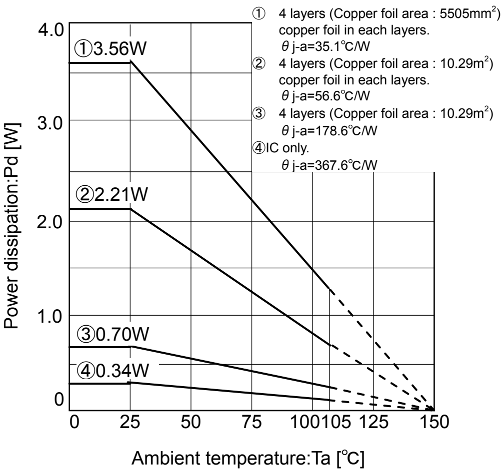


Fig.26 Thermal derating curve
(VQFN020V4040)

$P = I_{OUT}^2 \times R_{ON}$

$R_{ON} = D \times R_{ONP} + (1-D) R_{ONN}$

D : ON duty ($= V_{OUT}/V_{CC}$)

R_{COIL} : DC resistance of coil

R_{ONP} : ON resistance of P-channel MOS FET

R_{ONN} : ON resistance of N-channel MOS FET

I_{OUT} : Output current

If $V_{CC}=8V$, $V_{OUT}=5V$, $R_{ONP}=0.15\Omega$, $R_{ONN}=0.08\Omega$
$I_{OUT}=2A$, for example,

$$D = V_{OUT}/V_{CC} = 5/8 = 0.625$$

$$R_{ON} = 0.625 \times 0.15 + (1-0.625) \times 0.08 = 0.09375 + 0.03 = 0.12375[\Omega]$$

$$P = 2^2 \times 0.12375 = 0.495[W]$$

As R_{ONP} is greater than R_{ONN} in this IC, the dissipation increases as the ON duty becomes greater. With the consideration on the dissipation as above, thermal design must be carried out with sufficient margin allowed.

●Selection of components externally connected

1. Selection of inductor (L)

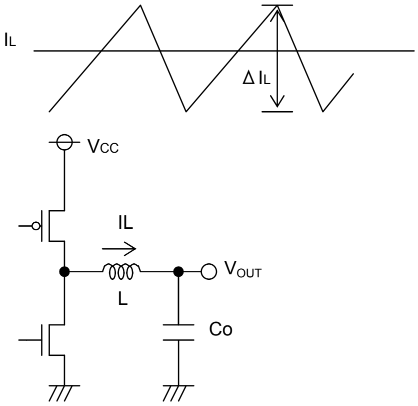


Fig.27 Output ripple current

The inductance significantly depends on output ripple current. As seen in the equation (1), the ripple current decreases as the inductor and/or switching frequency increases.

$$\Delta I_L = \frac{(V_{CC}-V_{OUT})\times V_{OUT}}{L\times V_{CC}\times f}\ [A]\ \cdot\cdot\cdot\ (1)$$

Appropriate ripple current at output should be 20% more or less of the maximum output current.

$$\Delta I_L = 0.2\times I_{OUT}max.\ [A]\ \cdot\cdot\cdot\ (2)$$

$$L = \frac{(V_{CC}-V_{OUT})\times V_{OUT}}{\Delta I_L\times V_{CC}\times f}\ [H]\ \cdot\cdot\cdot\ (3)$$

(ΔI_L: Output ripple current, and f: Switching frequency)

*Current exceeding the current rating of the inductor results in magnetic saturation of the inductor, which decreases efficiency. The inductor must be selected allowing sufficient margin with which the peak current may not exceed its current rating.

If V_{CC}=3.3V, V_{OUT}=1.8V, f=1MHz, ΔI_L=0.2×2A=0.4A, for example,(BD9141MUV)

$$L = \frac{(8-5)\times 5}{0.6\times 8\times 500k} = 6.25\mu \ \rightarrow\ 6.3[\mu H]$$

*Select the inductor of low resistance component (such as DCR and ACR) to minimize dissipation in the inductor for better efficiency.

2. Selection of output capacitor (C_O)

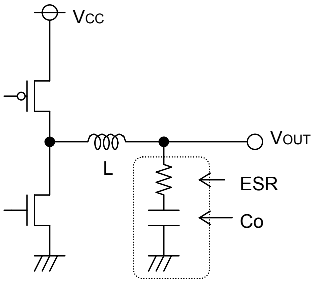


Fig.28 Output capacitor

Output capacitor should be selected with the consideration on the stability region and the equivalent series resistance required to smooth ripple voltage.

Output ripple voltage is determined by the equation (4) :

$$\Delta V_{OUT} = \Delta I_L\times ESR\ [V]\ \cdot\cdot\cdot\ (4)$$

(ΔI_L: Output ripple current, ESR: Equivalent series resistance of output capacitor)

*Rating of the capacitor should be determined allowing sufficient margin against output voltage. A 22μF to 100μF ceramic capacitor is recommended.
Less ESR allows reduction in output ripple voltage.

3. Selection of input capacitor (Cin)

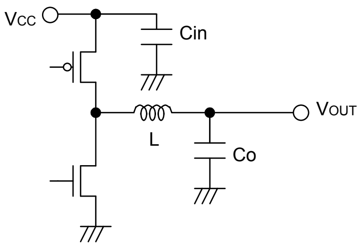


Fig.29 Input capacitor

Input capacitor to select must be a low ESR capacitor of the capacitance sufficient to cope with high ripple current to prevent high transient voltage. The ripple current IRMS is given by the equation (5):

$$I_{RMS}=I_{OUT}\times\frac{\sqrt{V_{OUT}(V_{CC}-V_{OUT})}}{V_{CC}}\ [A]\ \cdot\cdot\cdot(5)$$

< Worst case > $I_{RMS(max.)}$

When Vcc is twice the V_{OUT}, $I_{RMS}=\frac{I_{OUT}}{2}$

If V_{CC}=8V, V_{OUT}=5V, and $I_{OUTmax.}$=2A, (BD9140MUV)

$$I_{RMS}=2\times\frac{\sqrt{5(8-5)}}{3.3}=0.97[A_{RMS}]$$

A low ESR 22μF/25V ceramic capacitor is recommended to reduce ESR dissipation of input capacitor for better efficiency.

4. Determination of RITH, CITH that works as a phase compensator

As the Current Mode Control is designed to limit a inductor current, a pole (phase lag) appears in the low frequency area due to a CR filter consisting of a output capacitor and a load resistance, while a zero (phase lead) appears in the high frequency area due to the output capacitor and its ESR. So, the phases are easily compensated by adding a zero to the power amplifier output with C and R as described below to cancel a pole at the power amplifier.

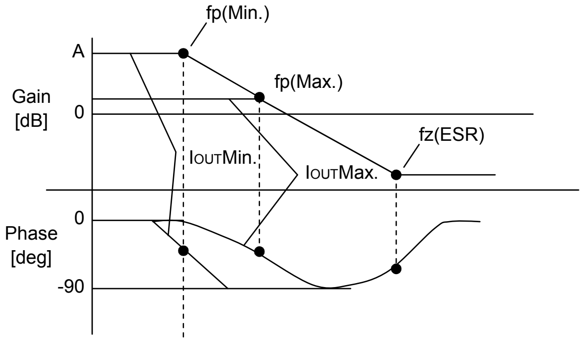


Fig.30 Open loop gain characteristics

$$fp=\frac{1}{2\pi\times R_O\times C_O}$$

$$fz_{(ESR)}=\frac{1}{2\pi\times E_{SR}\times C_O}$$

Pole at power amplifier

When the output current decreases, the load resistance Ro increases and the pole frequency lowers.

$$fp_{(Min.)}=\frac{1}{2\pi\times R_{OMax.}\times C_O}\ [Hz]\leftarrow\text{with lighter load}$$

$$fp_{(Max.)}=\frac{1}{2\pi\times R_{OMin.}\times C_O}\ [Hz]\leftarrow\text{with heavier load}$$

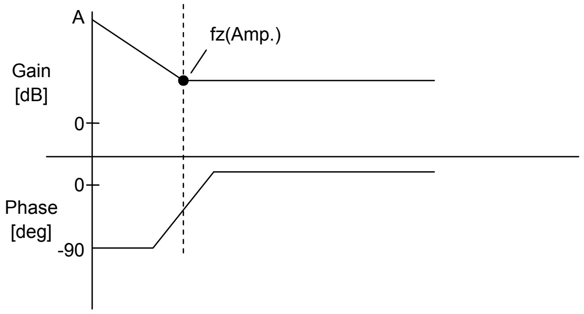


Fig.31 Error amp phase compensation characteristics

Zero at power amplifier

Increasing capacitance of the output capacitor lowers the pole frequency while the zero frequency does not change. (This is because when the capacitance is doubled, the capacitor ESR reduces to half.)

$$fz_{(Amp.)}=\frac{1}{2\pi\times R_{ITH}\times C_{ITH}}$$

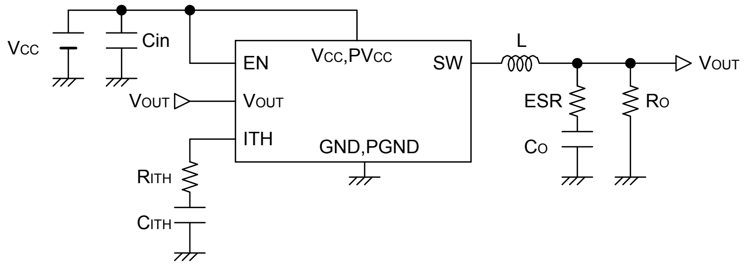


Fig.32 Typical application

Stable feedback loop may be achieved by canceling the pole fp (Min.) produced by the output capacitor and the load resistance with CR zero correction by the error amplifier.

$$f_{z(\mathrm{Amp.})} = f_{p(\mathrm{Min.})}$$

$$\longrightarrow \frac{1}{2\pi \times R_{ITH} \times C_{ITH}} = \frac{1}{2\pi \times R_{O\mathrm{Max.}} \times C_O}$$

5. Determination of output voltage

The output voltage VOUT is determined by the equation (6):
$V_{OUT}=(R2/R1+1) \times V_{ADJ}$ ・・・(6)　V_{ADJ}: Voltage at ADJ terminal (0.8V Typ.)
With R1 and R2 adjusted, the output voltage may be determined as required.

(Adjustable output voltage range : 2.5V～6.0V)

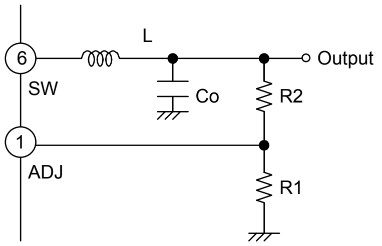


Fig.33 Determination of output voltage

Use 1 kΩ～100 kΩ resistor for R1.　if you can use the resistance more than 100kΩ or they have a big range between the setting value of output voltage and input voltage.

The minimum input voltage depends on the setting output voltage.
Basically, it is recommended to use in the condition :
　　VCCmin = VOUT+1.3V.
It is shown the necessary output current value at the minimum input voltage. (DCR of inductor : 0.1Ω)See Fig.34.
This data is the characteristic value, so it doesn't guarantee the operation range.

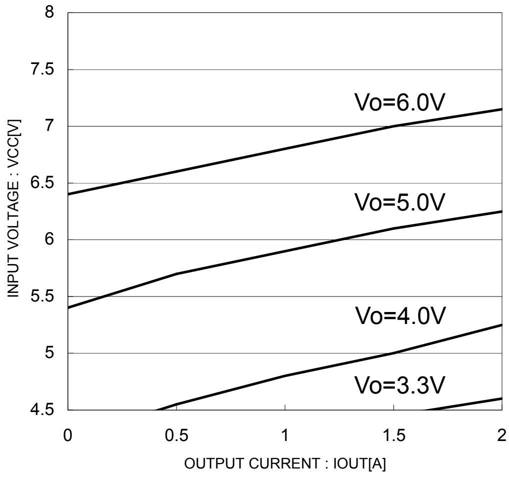


Fig.34 minimum input voltage in each output voltage

6.Selection of the reference voltage capacitor (CVREG)

VREG voltage is the reference voltage created by Input voltage (Vcc Voltage). CVREG capacitor should be selected 0.1uF or more.

●BD9141MUV　Cautions on PC Board layout

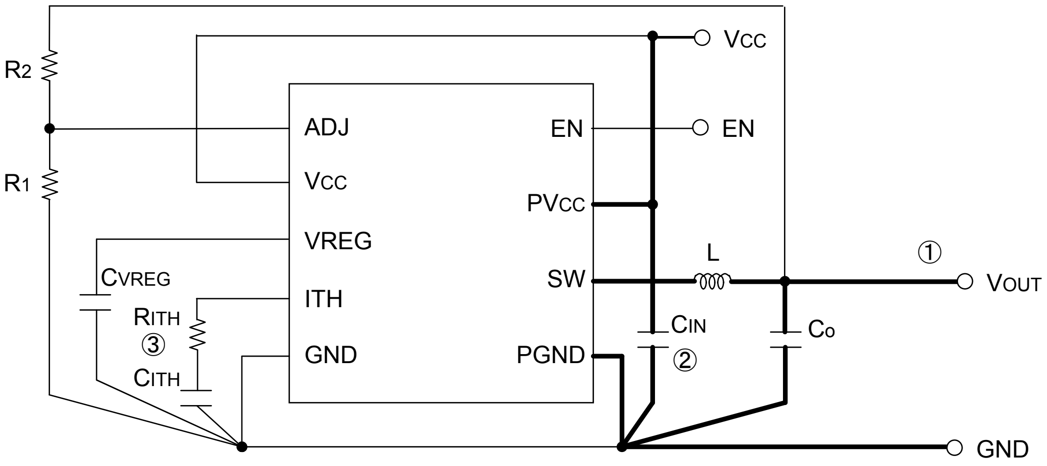


Fig.34 Layout diagram

① For the sections drawn with heavy line, use thick conductor pattern as short as possible.
② Lay out the input ceramic capacitor CIN closer to the pins PVCC and PGND, and the output capacitor Co closer to the pin PGND.
③ Lay out CITH and RITH between the pins ITH and GND as neat as possible with least necessary wiring.

※ VQFN020V4040 (BD9141MUV) has thermal FIN on the reverse of the package.
The package thermal performance may be enhanced by bonding the FIN to GND plane which take a large area of PCB.

●Recommended components Lists on above application

Symbol	Part	Value		Manufacturer	Series
L	Coil	4.7uH		TDK	RLF7030T-4R7M3R4
CIN	Ceramic capacitor	22uF		kyocera	CM32X5R226M25A
CO	Ceramic capacitor	22uF		kyocera	CM32X5R226M10A
CVREG	Ceramic capacitor	0.1uF		murata	GRM188B11H102KA01
CITH	Ceramic capacitor	Vo=3.3V	1000pF	murata	CM05B104K10A
		Vo=5V	1000pF	murata	CM05B104K10A
RITH	Resistance	Vo=3.3V	20kΩ	Rohm	MCR03 Serise
		Vo=5V	47kΩ	Rohm	MCR03 Serise

*The parts list presented above is an example of recommended parts. Although the parts are sound, actual circuit characteristics should be checked on your application carefully before use. Be sure to allow sufficient margins to accommodate variations between external devices and this IC when employing the depicted circuit with other circuit constants modified. Both static and transient characteristics should be considered in establishing these margins. When switching noise is substantial and may impact the system, a low pass filter should be inserted between the VCC and PVCC pins, and a schottky barrier diode established between the SW and PGND pins.

●I/O equivalence circuit

【BD9141MUV】

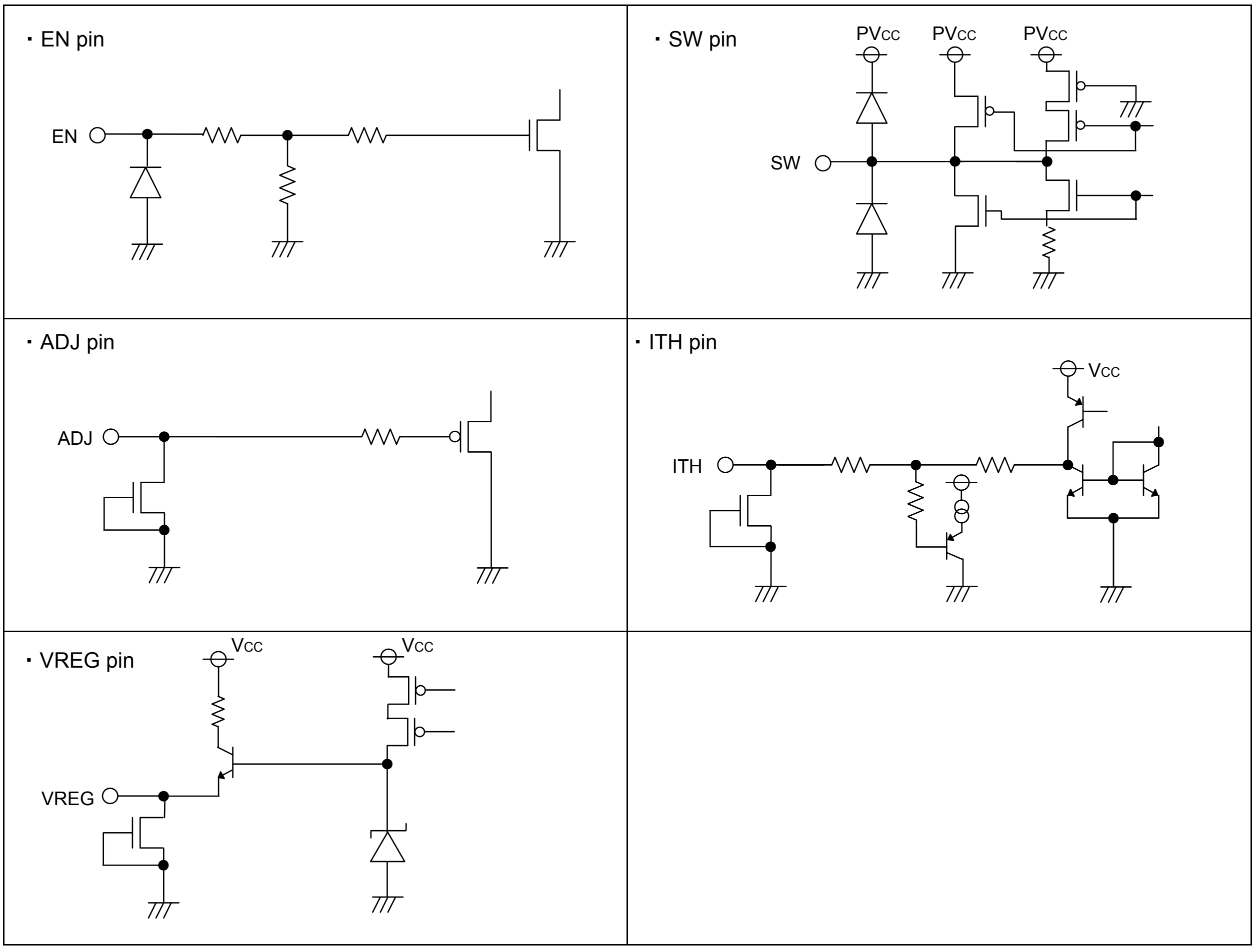


Fig.35 I/O equivalence circuit

●Cautions on use

1. Absolute Maximum Ratings

While utmost care is taken to quality control of this product, any application that may exceed some of the absolute maximum ratings including the voltage applied and the operating temperature range may result in breakage. If broken, short-mode or open-mode may not be identified. So if it is expected to encounter with special mode that may exceed the absolute maximum ratings, it is requested to take necessary safety measures physically including insertion of fuses.

2. Electrical potential at GND

GND must be designed to have the lowest electrical potential In any operating conditions.

3. Short-circuiting between terminals, and mismounting

When mounting to pc board, care must be taken to avoid mistake in its orientation and alignment. Failure to do so may result in IC breakdown. Short-circuiting due to foreign matters entered between output terminals, or between output and power supply or GND may also cause breakdown.

4.Operation in Strong electromagnetic field

Be noted that using the IC in the strong electromagnetic radiation can cause operation failures.

5. Thermal shutdown protection circuit

Thermal shutdown protection circuit is the circuit designed to isolate the IC from thermal runaway, and not intended to protect and guarantee the IC. So, the IC the thermal shutdown protection circuit of which is once activated should not be used thereafter for any operation originally intended.

6. Inspection with the IC set to a pc board

If a capacitor must be connected to the pin of lower impedance during inspection with the IC set to a pc board, the capacitor must be discharged after each process to avoid stress to the IC. For electrostatic protection, provide proper grounding to assembling processes with special care taken in handling and storage. When connecting to jigs in the inspection process, be sure to turn OFF the power supply before it is connected and removed.

7. Input to IC terminals

This is a monolithic IC with P^+ isolation between P-substrate and each element as illustrated below. This P-layer and the N-layer of each element form a P-N junction, and various parasitic element are formed.

If a resistor is joined to a transistor terminal as shown in Fig 37.

○P-N junction works as a parasitic diode if the following relationship is satisfied; GND>Terminal A (at resistor side), or GND>Terminal B (at transistor side); and

○if GND>Terminal B (at NPN transistor side),

a parasitic NPN transistor is activated by N-layer of other element adjacent to the above-mentioned parasitic diode.

The structure of the IC inevitably forms parasitic elements, the activation of which may cause interference among circuits, and/or malfunctions contributing to breakdown. It is therefore requested to take care not to use the device in such manner that the voltage lower than GND (at P-substrate) may be applied to the input terminal, which may result in activation of parasitic elements.

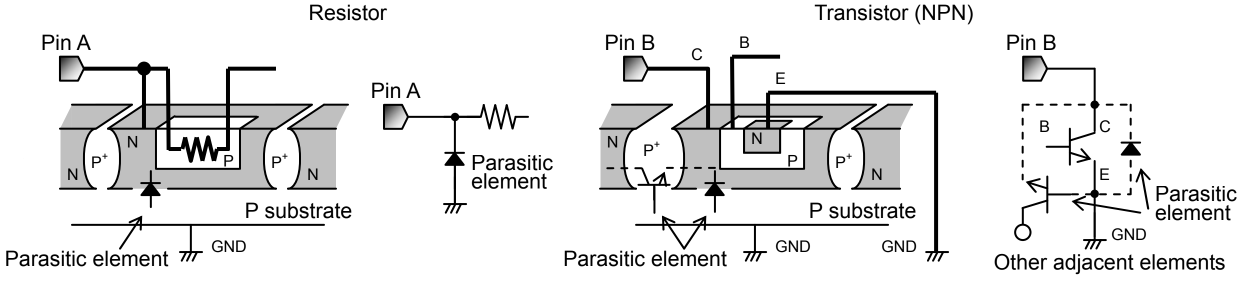


Fig.36 Simplified structure of monorisic IC

8. Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

9 . Selection of inductor

It is recommended to use an inductor with a series resistance element (DCR) 0.1Ω or less. When using an inductor over 0.1Ω, be careful to ensure adequate margins for variation between external devices and this IC, including transient as well as static characteristics. Furthermore, in any case, it is recommended to start up the output with EN after supply voltage is within operation range.

●Ordering part number

B D 9 1 4 1 M U V – E 2

ROHM part number

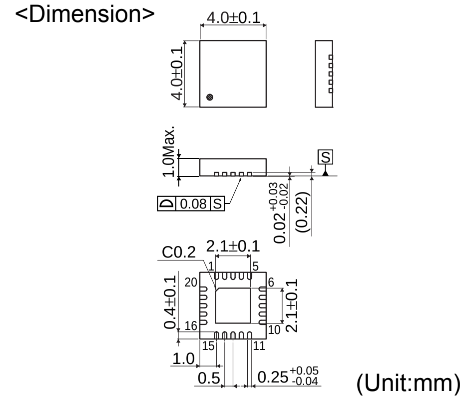
Type
41 : Adjustable (2.5～6V)

Package
MUV : VQFN020V4040

Package specification
E2 : Embossed taping

VQFN020V4040

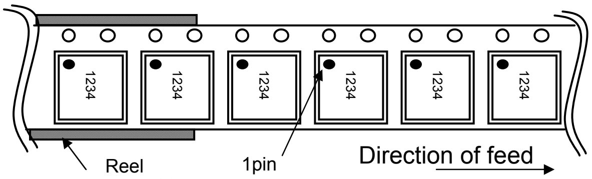
<Dimension>



(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

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