

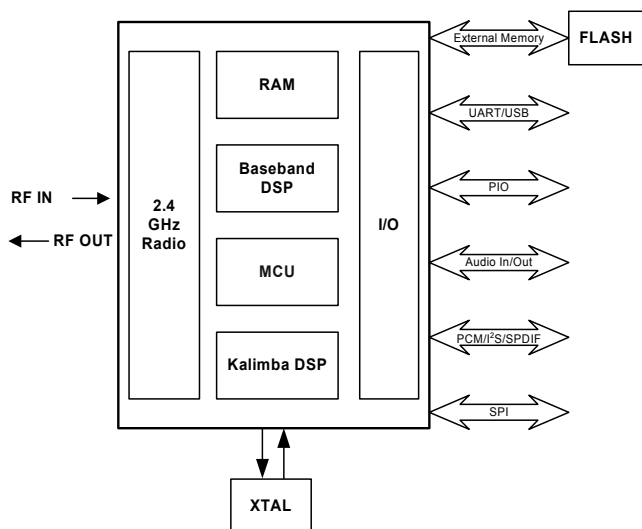
Features

- Fully Qualified Bluetooth v2.1 + EDR Specification System
- Best in Class Bluetooth Radio with 8dBm Transmit Power and -90dBm Receive Sensitivity
- 64MIPS Kalimba DSP Co-processor
- 16-bit Internal Stereo CODEC 95dB SNR for DAC
- Low-power 1.5V Operation, 1.8V to 3.6V I/O
- Integrated 1.5V and 1.8V Linear Regulators
- Integrated Switched-mode Regulator
- Integrated Battery Charger
- USB, I²C and UART with Dual-port Bypass Mode to 4Mbits/s
- Supports up to 32Mbit of External Flash Memory (8Mbit Typical Requirement)
- Multi-configurable I²S, PCM or SPDIF Interface
- Enhanced Audibility and Noise Cancellation
- 8 x 8 x 1.2mm, 0.5mm pitch 169-ball TFBGA
- Support for 802.11 Co-existence
- RoHS Compliant

General Description

The BlueCore[®]5-Multimedia External is a single-chip radio and baseband IC for Bluetooth 2.4GHz systems.

BlueCore5-Multimedia External interfaces up to 32Mbit of external Flash memory. When used with the CSR Bluetooth stack, it provides a fully compliant Bluetooth v2.1 + EDR specification system for data and voice.



BlueCore[®]5-Multimedia External

Single Chip Bluetooth[®] v2.1 + EDR System

Production Information

BC57E687B

Issue 2

Applications

- High-quality Stereo Wireless Headsets
- High-quality Mono Headsets
- Hands-free Car Kits
- Wireless Speakers
- VoIP Handsets
- Analogue and USB Multimedia Dongles
- Bluetooth-enabled Automotive Wireless Gateways

BlueCore5-Multimedia External contains the Kalimba DSP co-processor with double the MIPS of BlueCore3-Multimedia External, supporting enhanced audio applications.

BlueCore5-Multimedia External is designed to reduce the number of external components required which ensures production costs are minimised. The device incorporates auto-calibration and *built-in self-test* (BIST) routines to simplify development, type approval and production test.

To improve the performance of both Bluetooth and 802.11b/g co-located systems a wide range of co-existence features are available including a variety of hardware signalling: basic activity signalling, Intel WCS activity and channel signalling.

For additional performance information refer to the *BlueCore5-Multimedia External Product Data Sheet*.

1 Device Details

Radio

- Common TX/RX terminal simplifies external matching; eliminates external antenna switch
- BIST minimises production test time
- Bluetooth v2.1 + EDR specification compliant

Transmitter

- 8dBm RF transmit power with level control from on-chip 6-bit DAC over a dynamic range >30dB
- Class 2 and Class 3 support without the need for an external power amplifier or TX/RX switch

Receiver

- Receiver sensitivity of -90dBm
- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real-time digitised RSSI available on HCI interface
- Fast AGC for enhanced dynamic range

Synthesiser

- Fully integrated synthesiser requires no external VCO, varactor diode, resonator or loop filter
- Compatible with crystals 16MHz to 26MHz or an external clock 12MHz to 52MHz
- Accepts 14.40, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz TCXO frequencies for GSM and CDMA devices with sinusoidal or logic level signals

Baseband and Software

- 32Mbit of external Flash
- 48Kbyte of internal RAM, allows full-speed data transfer, mixed voice/data and full piconet support
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping
- Transcoders for A-law, μ -law and linear voice from host and A-law, μ -law and CVSD voice over air

Physical Interfaces

- SPI with clock speeds up to 64MHz in Master mode⁽¹⁾ and 32MHz in Slave mode
- I²C master compatible interface
- UART interface with programmable data rate up to 3Mbits/s with an optional bypass mode
- Full speed USB v1.1 interface
- Bi-directional serial programmable audio interface supporting PCM, I²S and SPDIF formats
- Two LED drivers with faders

⁽¹⁾ Requires firmware support

Kalimba DSP

- Very low power Kalimba DSP co-processor, 64MIPS, 24-bit fixed point core
- SBC decode takes approximately 4mW power consumption while streaming music
- Single-cycle MAC; 24 x 24-bit multiply and 56-bit accumulator
- 32-bit instruction word, dual 24-bit data memory
- 24-Kbyte (6-Kword) program RAM, 36-Kbyte + 48-Kbyte (16-Kword + 12-Kword) data RAM
- 64-word x 32-bit program memory cache when executing from Flash

Stereo Audio CODEC

- 16-bit internal stereo CODEC
- Dual ADC and DAC for stereo audio
- Integrated amplifiers for driving 16 Ω speakers; no need for external components
- Support for single-ended speaker termination and line output
- Integrated low-noise microphone bias
- ADC sample rates are 8, 11.025, 16, 22.05, 32 and 44.1kHz
- DAC sample rates are 8, 11.025, 12, 16, 22.05, 24, 32, 44.1 and 48kHz

Auxiliary Features

- User space on processor for customer applications
- Crystal oscillator with built-in digital trimming
- Power management includes digital shutdown and wake-up commands with an integrated low-power oscillator for ultra-low power Park/Sniff/Hold mode
- Clock request output to control external clock
- On-chip regulators: 1.5V output from 1.8V to 2.7V input and 1.8V output from 2.7V to 4.5V input
- On-chip high-efficiency switched-mode regulator; 1.8V output from 2.7V to 4.4V input
- Power-on-reset cell detects low supply voltage
- 10-bit ADC and 8-bit DAC available to applications
- On-chip charger for lithium ion/polymer batteries

Bluetooth Stack

CSR's Bluetooth Protocol Stack runs on the on-chip MCU in a variety of configurations:

- Standard HCI (UART or USB)
- Audio CODEC and echo-noise suppression or customer-specific algorithms running on the DSP

Package Option

- TFBGA 169-ball, 8 x 8 x 1.2mm, 0.5mm pitch

2 Ordering Information

Interface Version	Package			Order Number
	Type	Size	Shipment Method	
UART and USB	TFBGA 169-ball (Pb free)	8 x 8 x 1.2mm, 0.5mm pitch	Tape and reel	BC57E687B-ITB-E4

Note:

At **Production** status **Minimum Order Quantity** is 2kpcs taped and reeled.

To contact a CSR representative, email sales@csr.com or go to www.csr.com/contacts

Document History

Revision	Date	Change Reason
Issue 1	10 AUG 07	Original Publication of this document. (Replaces CS-101610-PBP3)
Issue 2	10 JUL 08	Order code update. Temperature range moved to -40°C to 85°C. If you have any comments about this document, email comments@csr.com giving the number, title and section with your feedback.

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