OVERVIEW DATA SHEET: BT2084A

DUAL-BAND GSM & DCS SINGLE CHIP RF TRANSCEIVER

Features

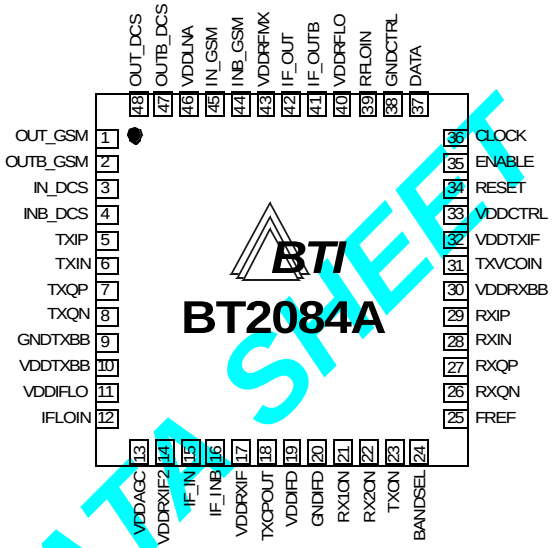
- Highly integrated complete dual-band GSM900 and DCS1800 / PCS1900 RF Transceiver
- Low noise and wide dynamic range receiver
- Greater than 35dB on-chip image rejection in receive mode
- Over 90dB overall gain control in 2dB steps in receive mode
- Offset PLL transmitter architecture
- Operating supply voltage from 2.7V to 3.3V
- Ambient temperature range (-40°C to +85°C)
- Low power BiCMOS silicon technology
- 48L QLP package with exposed ground pad

Functions

- **Receiver:**
  - Dual Low Noise Amplifier (LNA) w/ Gain Control
  - Dual Image Reject RxRF Mixer
  - IF Output Buffer
  - IF Input Buffer w/ Gain Control
  - RxIF Mixer
  - Automatic Gain Control (AGC)
  - I/Q Demodulator
  - Baseband Channel Select Filter with tuning
  - Baseband I/Q Buffer
  - DC Offset Calibration
- **Transmitter:**
  - I/Q Modulator
  - Offset PLL
    - Downconversion Mixer
    - Phase Detector
- **IFLO Buffer**
- **RFLO Buffer**

Applications

- GSM/DCS Handsets & Communication Systems
- RF Wireless Modems
- RF Wireless Communications Products



General Description

The BT2084A is a highly integrated low power silicon BiCMOS RF transceiver designed for dual-band GSM900 and DCS1800/PCS1900 handset applications. The BT2084A consists of a receiver, transmitter, and both IF and RFLO buffer sections.

The receiver can be divided into two sections. The first section is the receiver front-end which consists of a low noise amplifier (LNA), image-reject downconversion mixers and an IF output buffer. This section provides amplification for the incoming signal with low noise and high linearity. It also provides more than 35dB image suppression and 20dB gain control. The second section consists of an IF input buffer, IF downconversion mixer, automatic gain control (AGC), I/Q demodulator, baseband channel select filter, and a baseband buffer. This section provides second downconversion and I/Q demodulation to the channel-selected signal and an additional on-chip channel selection. The IF input buffer and AGC perform over 90dB gain control in 2dB steps.

GRT™ RFICs for GSM cellular

Ordering Information

BT2084A GSM/DCS/PCS Dual-Band RF Transceiver

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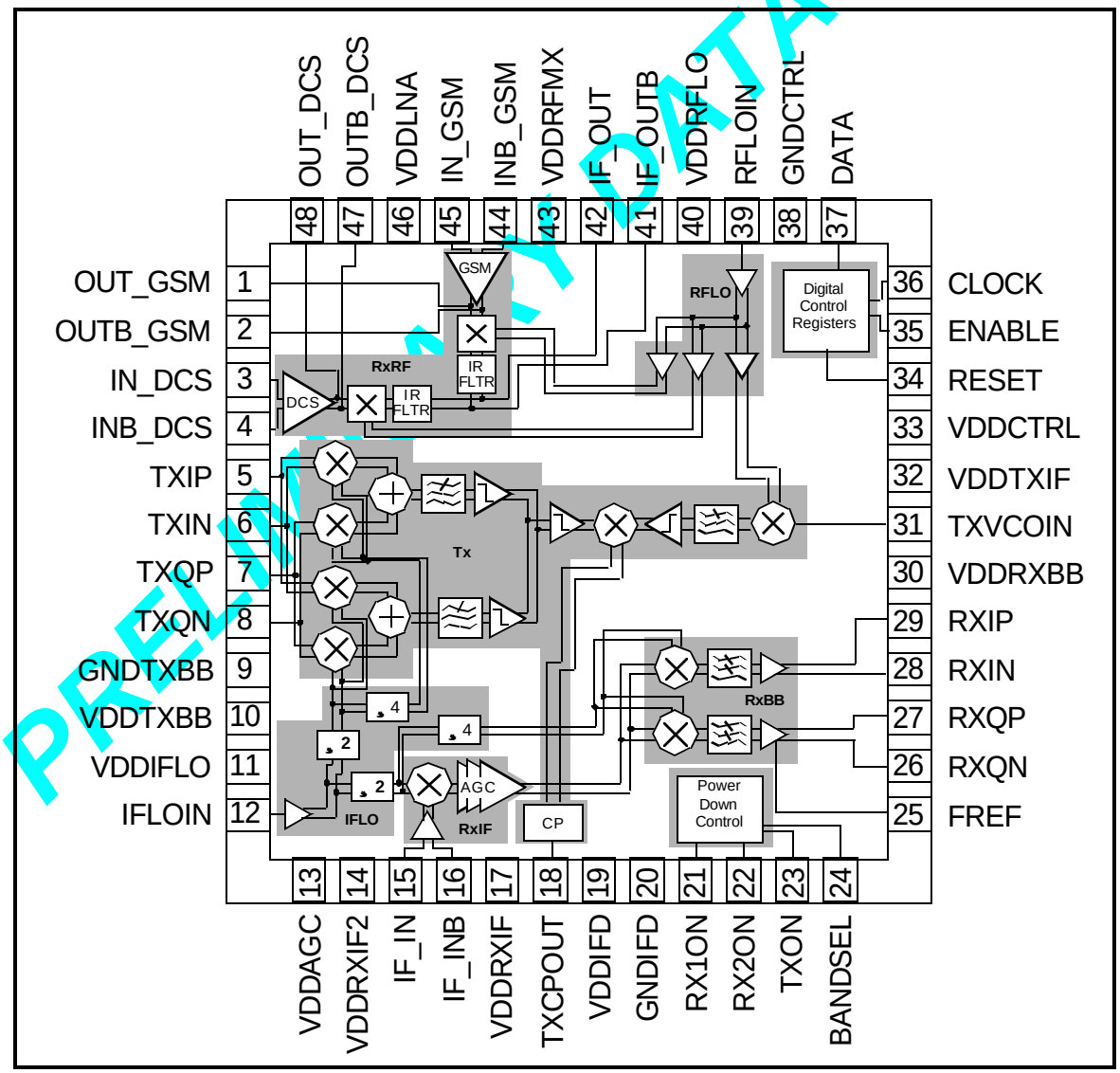
The transmitter employs an offset PLL architecture and also consists of two sections. The first section is the I/Q modulator which upconverts the incoming baseband signal to the common IF frequency. The second section is the offset PLL, which consists of a downconversion mixer and a phase detector. The phase detector compares the downconverted external Tx VCO output and the upconverted baseband input at the common IF frequency. The output of the phase detector controls the off-chip Tx VCO to generate the RF transmit signal.

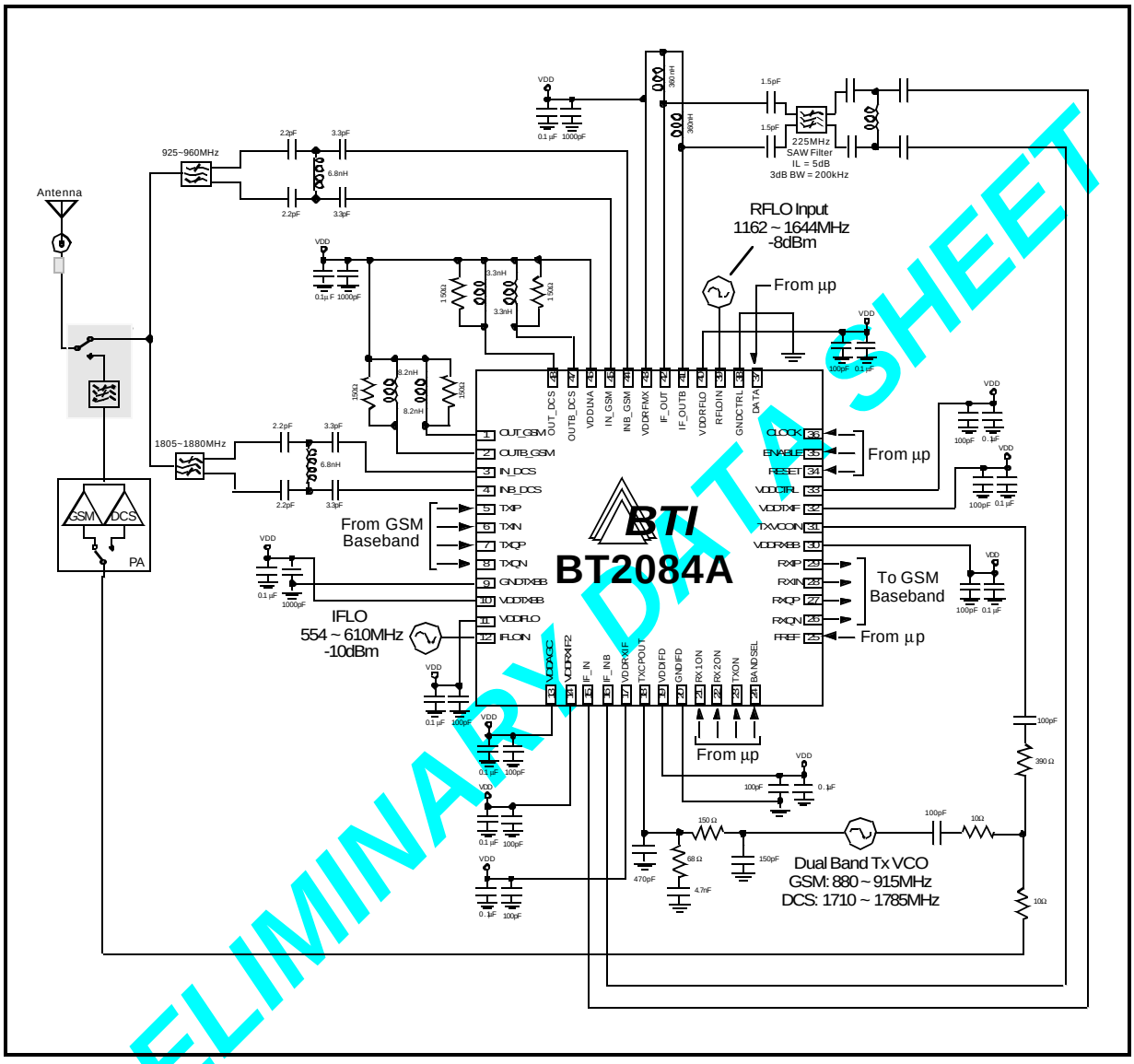
The IFLO section includes buffers and dividers that provide LO signals for both receiver and transmitter sections. The input to the IFLO section is generated from an off-chip VCO. The RFLO section includes buffers that provide LO signals for both the receiver and transmitter. The input to the RFLO section is also generated from an off-chip VCO.

The operation of the transceiver in different modes is controlled using combinations of the RX1ON, RX2ON, TXON, and BANDSEL pins (*Table #2*). The other operation set-ups such as gain control in the LNA, IF buffer, and the AGC are provided digitally through a 3-wire interface with a microcontroller or baseband processor (*Table #3*).

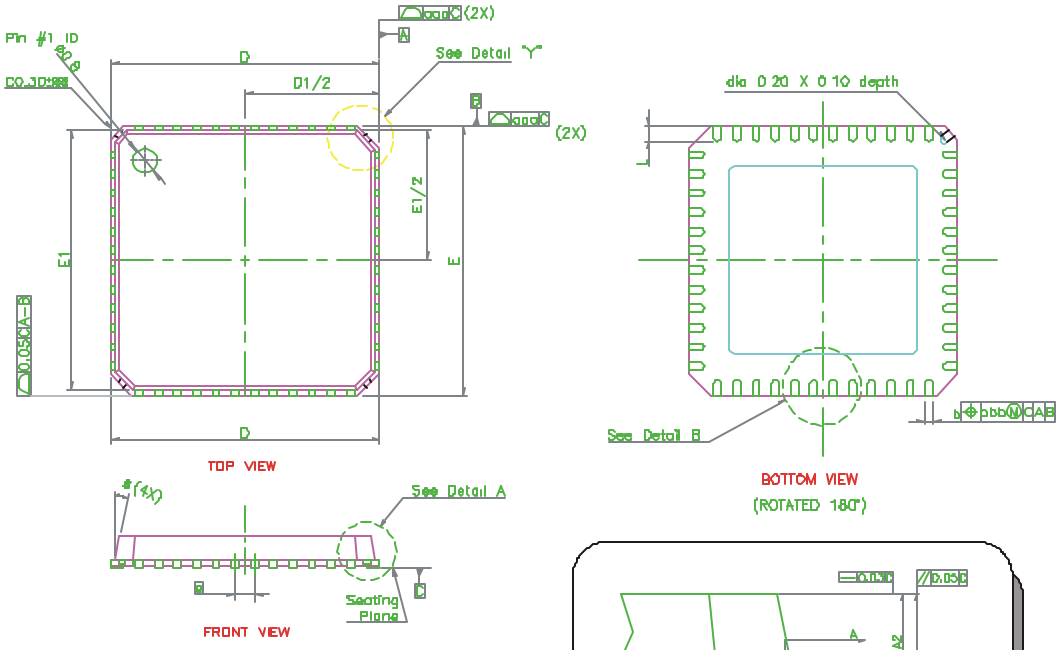
Functional Block Diagram



Application Circuit

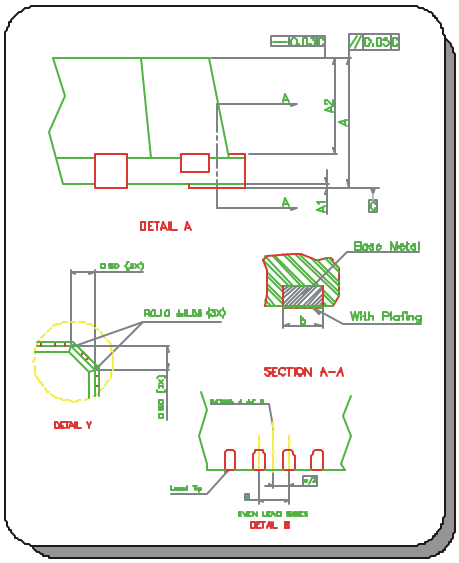


Package Information



DIMENSION TABLE
(48L QLP 7X7 BODY)

SYMBOL	SPECIFICATION	DESCRIPTION
A	1.0 MAX.	Package Seated Height
A1	5µm ~ 20µm	Stand-off
A2	0.70±0.08	Mold Cap Thickness
D	7.00 ±0.10	Terminal dimension "D"
D1	6.75 ±0.10	Package length
E	7.00 ±0.10	Terminal Dimension "E"
E1	6.75 ±0.10	Package width
b	0.23 ±0.04	Lead width (after plate)
b1	0.20 BSC	Lead width (before plate)
e	0.50 BSC	Lead pitch
N	48	Lead count
L	0.40 ±0.10	Lead foot length
θ	11°±1	Package draft angle
aaa	0.05	Package body side alignment
bbb	0.05	Ld foot length alignment



1. Controlling dimension are in millimeter (mm).
2. Top package body corner radius to be 0.15±0.08
3. Microgap visible by 45X shall not be allowed.
4. Lead tip burr shall be 0.03 maximum (Horizontal burr)
5. Vertical burr shall be not allowed
6. Interlead (window) flash remain after trim shall be at 0.125 maximum. Intrusion on package body is not allowed.
7. Gate residue shall not exceed 0.10 from the package body.
8. Pin #1 count orientation shall be at counterclockwise direction as viewed in live-bug position.
9. Package surface roughness at 0.9µm ±0.30
10. Gate burr remain after singulation shall be at 0.20 maximum.