

FEATURES

Operation: 2.3 GHz to 4.0 GHz
Gain of 14 dB at 2.6 GHz
OIP3 of 41 dBm at 2.6 GHz
P1dB of 25.7 dBm at 2.6 GHz
Noise figure: 4.0 dB at 2.6 GHz
Power supply: 5 V
Power supply current: 90 mA typical
Internal active biasing
Thermally efficient SOT-89 package
ESD rating of ± 2 kV (Class 3A)

GENERAL DESCRIPTION

The ADL5321 is a broadband, linear driver RF amplifier that operates at frequencies from 2.3 GHz to 4.0 GHz. The device can be used in a wide variety of wired and wireless applications, including ISM, WLL, PCS, GSM, CDMA, and W-CDMA.

The ADL5321 operates with a 5 V supply voltage and a supply current of 90 mA.

FUNCTIONAL BLOCK DIAGRAM

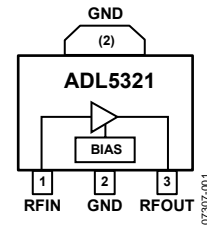


Figure 1.

The ADL5321 is fabricated on the GaAs HBT process. The device is packaged in a low cost SOT-89 that uses an exposed paddle for excellent thermal impedance. It operates from -40°C to $+85^{\circ}\text{C}$, and a fully populated evaluation board is available.

The [ADL5320](#) is a companion part to the ADL5321 that operates at similar performance from 400 MHz to 2700 MHz.

Rev. 0

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REVISION HISTORY

5/08—Revision 0: Initial Version

SPECIFICATIONS

VCC = 5 V and T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		2.3		4.0	GHz
FREQUENCY = 2.6 GHz					
Gain ¹		13.2	14.0	14.6	dB
vs. Frequency	±100 MHz		±0.4		dB
vs. Temperature	−40°C ≤ T _A ≤ +85°C		±0.7		dB
vs. Supply	4.75 V to 5.25 V		±0.07		dB
Output 1 dB Compression Point, P1dB			25.7		dBm
Output Third-Order Intercept, OIP3	Δf = 1 MHz, P _{OUT} = 5 dBm per tone		41		dBm
Noise Figure			4.0		dB
FREQUENCY = 3.5 GHz					
Gain ¹		11.1	12.0	12.9	dB
vs. Frequency	±100 MHz		±0.05		dB
vs. Temperature	−40°C ≤ T _A ≤ +85°C		±0.8		dB
vs. Supply	4.75 V to 5.25 V		±0.07		dB
Output 1 dB Compression Point, P1dB			25.7		dBm
Output Third-Order Intercept, OIP3	Δf = 1 MHz, P _{OUT} = 5 dBm per tone		38		dBm
Noise Figure			4.9		dB
POWER INTERFACE	Pin RFOUT				
Supply Voltage		4.5	5	5.5	V
Supply Current			90	100	mA
vs. Temperature	−40°C ≤ T _A ≤ +85°C		±6.0		mA
Power Dissipation	VCC = 5 V		520		mW

¹ Guaranteed maximum and minimum specified limits on this parameter are based on six sigma calculations.

ADL5321

TYPICAL SCATTERING PARAMETERS

VCC = 5 V and T_A = 25°C; the effects of the test fixture have been de-embedded up to the pins of the device.

Table 2.

Frequency (MHz)	S11		S21		S12		S22	
	Magnitude (dB)	Angle (°)	Magnitude (dB)	Angle (°)	Magnitude (dB)	Angle (°)	Magnitude (dB)	Angle (°)
2400	−4.47	−176.78	12.04	+74.69	−26.63	+16.98	−7.98	−111.37
2450	−4.57	−179.08	12.04	+71.96	−26.53	+15.09	−8.12	−113.06
2500	−4.62	+178.53	12.03	+69.02	−26.44	+12.94	−8.22	−115.61
2550	−4.70	+176.46	12.01	+66.20	−26.38	+10.91	−8.33	−118.13
2600	−4.78	+174.30	11.99	+63.23	−26.30	+8.56	−8.37	−121.11
2650	−4.88	+172.49	11.97	+60.32	−26.25	+6.38	−8.36	−124.14
2700	−4.97	+170.84	11.93	+57.28	−26.20	+3.90	−8.25	−127.48
2750	−5.07	+169.41	11.93	+54.11	−26.15	+1.38	−8.05	−130.84
2800	−5.23	+168.34	11.86	+51.18	−26.14	−1.15	−7.88	−133.91
2850	−5.44	+167.48	11.80	+47.81	−26.16	−3.88	−7.59	−137.02
2900	−5.72	+167.06	11.74	+44.61	−26.18	−6.79	−7.25	−139.88
2950	−6.00	+167.08	11.69	+41.14	−26.18	−9.78	−6.83	−142.37
3000	−6.40	+167.66	11.62	+37.73	−26.22	−13.00	−6.37	−144.60
3050	−6.84	+169.10	11.51	+34.13	−26.31	−16.32	−5.90	−146.58
3100	−7.32	+171.08	11.44	+30.41	−26.37	−19.95	−5.38	−148.25
3150	−7.93	+174.69	11.28	+26.53	−26.51	−23.60	−4.92	−149.46
3200	−8.52	+179.46	11.14	+22.45	−26.66	−27.66	−4.40	−150.81
3250	−9.06	−173.89	10.95	+18.23	−26.86	−31.92	−3.91	−151.83
3300	−9.46	−165.62	10.71	+13.94	−27.11	−36.45	−3.45	−152.90
3350	−9.48	−156.10	10.39	+9.45	−27.45	−41.18	−3.05	−153.80
3400	−9.18	−146.31	10.03	+5.06	−27.85	−45.96	−2.67	−154.63
3450	−8.56	−138.10	9.65	+0.71	−28.28	−50.83	−2.33	−155.41
3500	−7.74	−131.09	9.20	−3.47	−28.76	−55.67	−2.04	−156.03
3550	−6.90	−126.03	8.70	−7.62	−29.33	−60.52	−1.80	−156.44
3600	−6.08	−122.27	8.14	−11.37	−29.96	−65.27	−1.60	−156.77
3650	−5.35	−119.50	7.55	−14.86	−30.62	−69.78	−1.47	−156.90
3700	−4.73	−117.43	6.93	−18.10	−31.32	−74.35	−1.38	−156.85
3750	−4.15	−115.94	6.34	−21.07	−31.98	−78.77	−1.29	−156.62
3790	−3.78	−114.89	5.81	−23.21	−32.56	−82.30	−1.27	−156.36
3800	−3.68	−114.66	5.69	−23.67	−32.68	−83.17	−1.24	−156.19
3850	−3.29	−113.41	5.09	−25.99	−33.35	−87.33	−1.20	−155.59
3900	−2.97	−112.48	4.45	−27.94	−34.03	−91.70	−1.22	−154.96
3950	−2.67	−111.68	3.86	−29.95	−34.65	−96.22	−1.23	−154.01
4000	−2.41	−110.79	3.30	−31.52	−35.23	−100.84	−1.23	−153.20

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage, VCC	6.5 V
Input Power, 50 Ω Impedance	20 dBm
Internal Power Dissipation, Paddle Soldered	683 mW
θ_{JC} , Junction to Paddle	28.5°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ADL5321

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

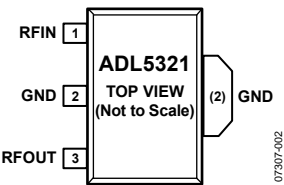


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RFIN	RF Input. This pin requires a dc blocking capacitor.
2	GND	Ground. Connect this pin to a low impedance ground plane.
3	RFOUT	RF Output and Supply Voltage. DC bias is provided to this pin through an inductor that is connected to the external power supply. RF path requires a dc blocking capacitor.
Exposed Paddle		Expose Paddle. Internally connected to GND. Solder to a low impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

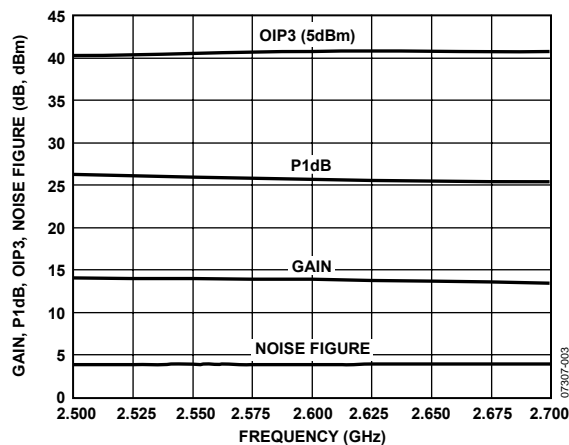


Figure 3. Gain, P1dB, OIP3, and Noise Figure vs. Frequency, 2.5 GHz to 2.7 GHz

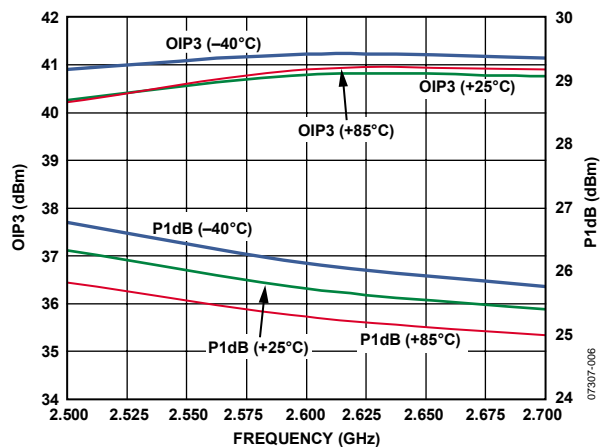


Figure 6. OIP3 and P1dB vs. Frequency and Temperature, 2.5 GHz to 2.7 GHz

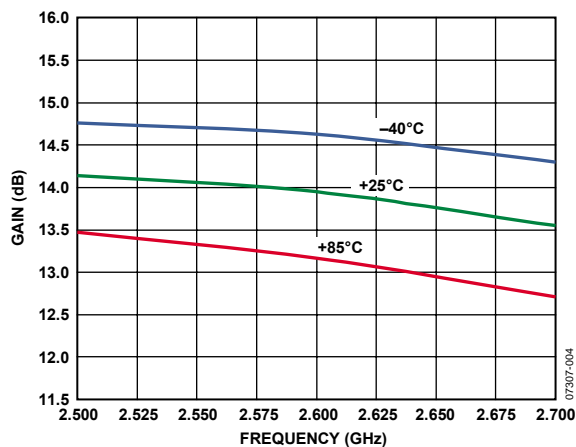


Figure 4. Gain vs. Frequency and Temperature, 2.5 GHz to 2.7 GHz

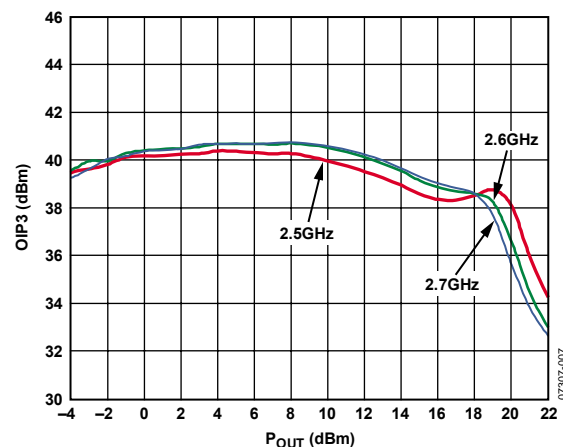


Figure 7. OIP3 vs. P_{OUT} and Frequency, 2.5 GHz to 2.7 GHz

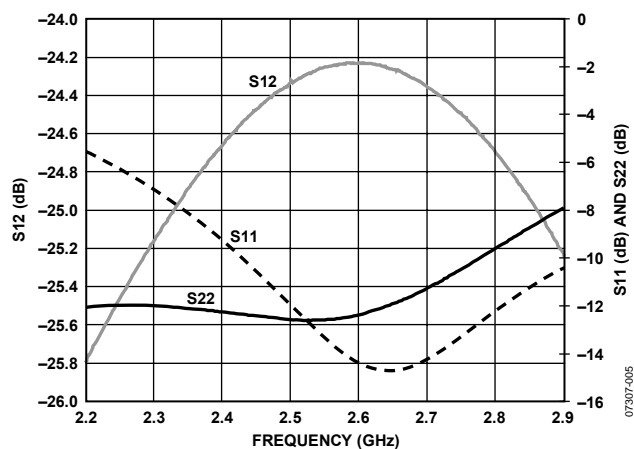


Figure 5. Reverse Isolation (S_{12}), Input Return Loss (S_{11}), and Output Return Loss (S_{22}) vs. Frequency, 2.2 GHz to 2.9 GHz

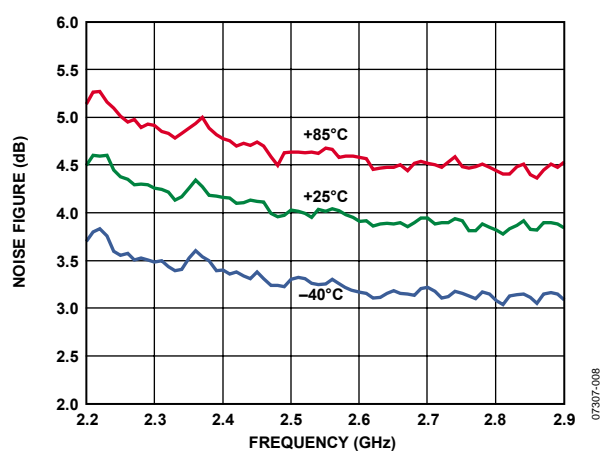


Figure 8. Noise Figure vs. Frequency and Temperature, 2.2 GHz to 2.9 GHz

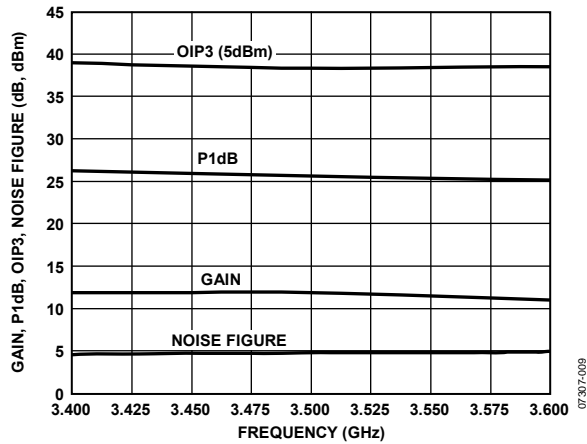


Figure 9. Gain, P1dB, OIP3, and Noise Figure vs. Frequency, 3.4 GHz to 3.6 GHz

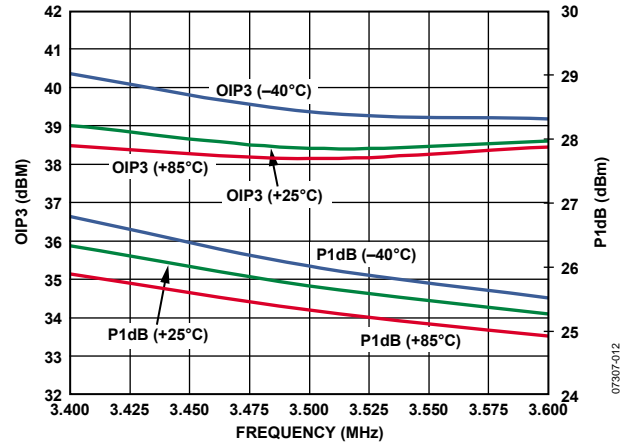


Figure 12. OIP3 and P1dB vs. Frequency and Temperature, 3.4 GHz to 3.6 GHz

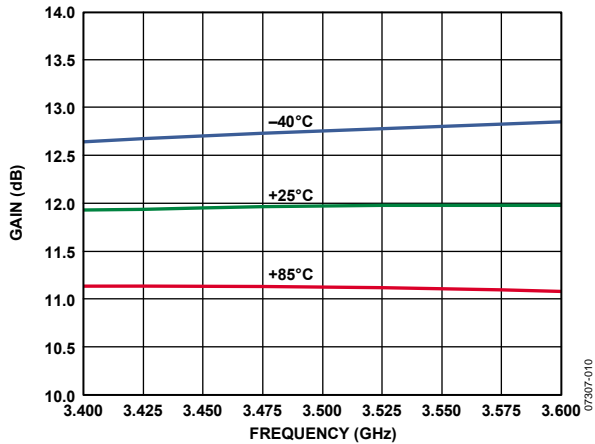


Figure 10. Gain vs. Frequency and Temperature, 3.4 GHz to 3.6 GHz

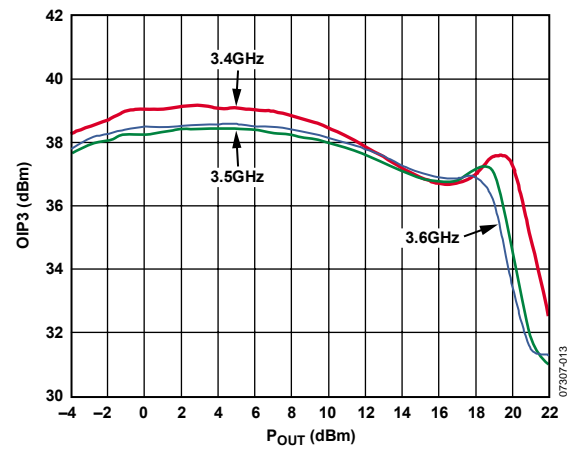


Figure 13. OIP3 vs. P_{OUT} and Frequency, 3.4 GHz to 3.6 GHz

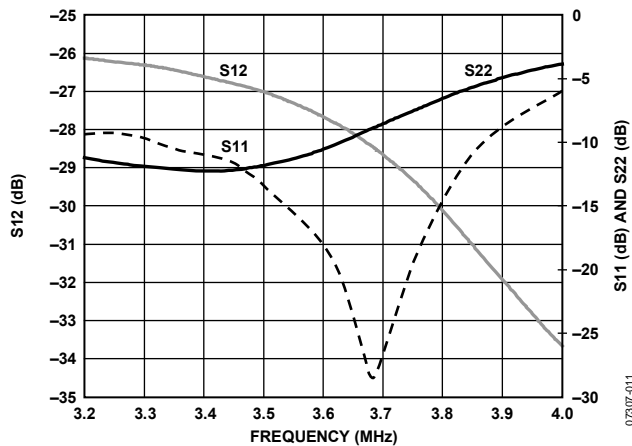


Figure 11. Reverse Isolation (S12), Input Return Loss (S11), and Output Return Loss (S22) vs. Frequency, 3.2 GHz to 4.0 GHz

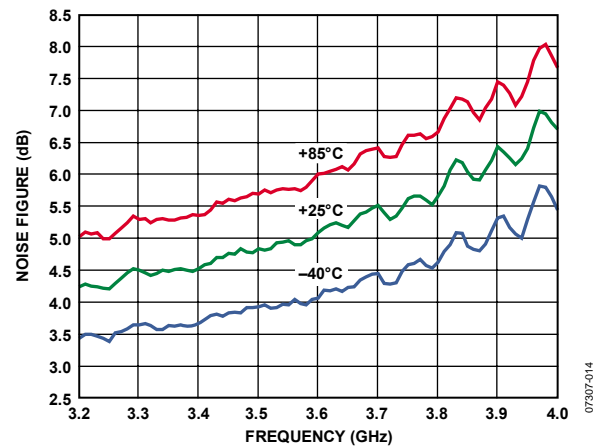


Figure 14. Noise Figure vs. Frequency and Temperature, 3.2 GHz to 4.0 GHz

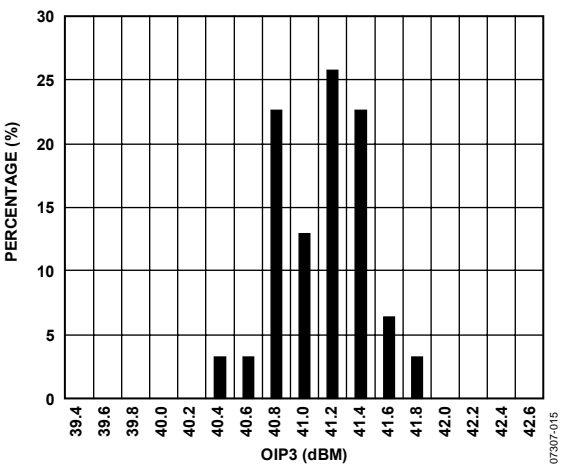


Figure 15. OIP3 Distribution at 2.6 GHz

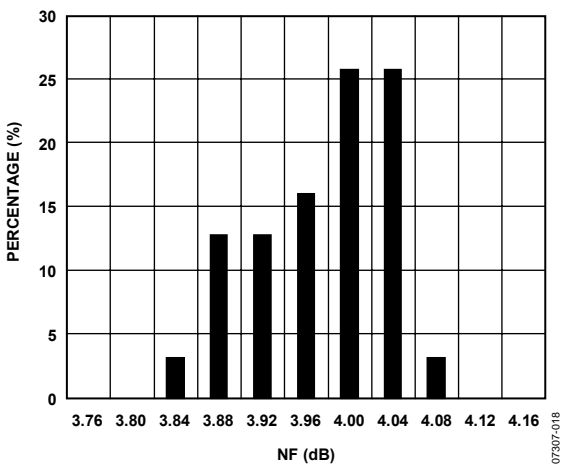


Figure 18. Noise Figure (NF) Distribution at 2.6 GHz

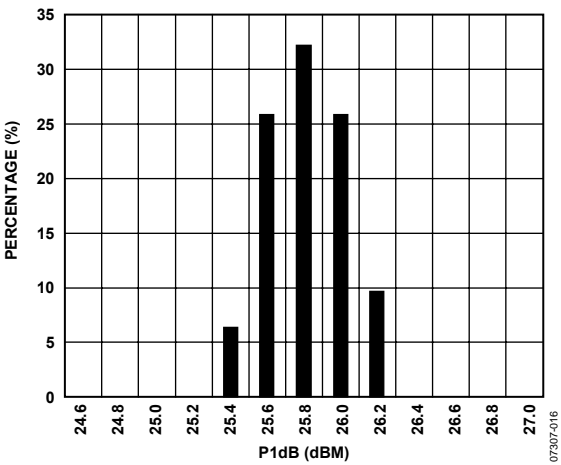


Figure 16. P1dB Distribution at 2.6 GHz

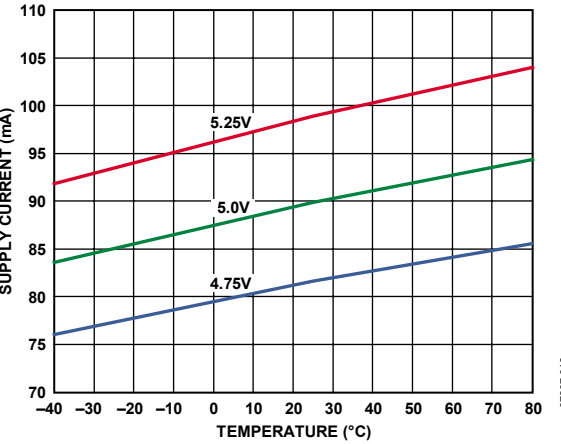


Figure 19. Supply Current vs. Temperature and Supply Voltage (Using 2.6 GHz Matching Components)

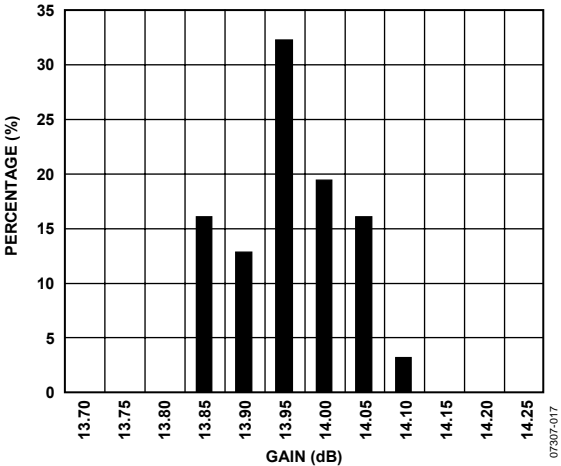


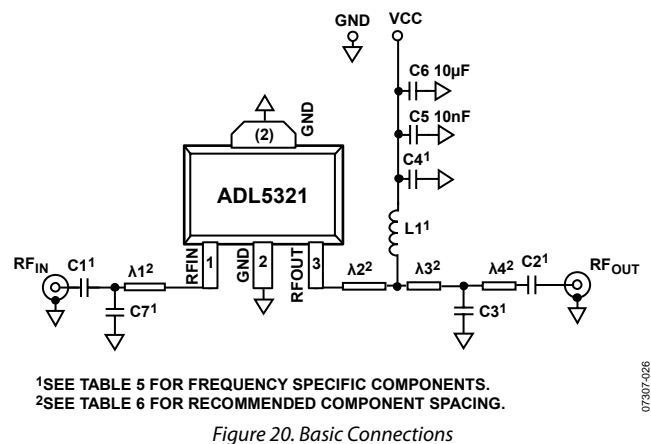
Figure 17. Gain Distribution at 2.6 GHz

BASIC LAYOUT CONNECTIONS

The basic connections for operating the ADL5321 are shown in Figure 20.

Table 5 lists the required matching components. Capacitors C1, C2, C3, C4, and C7 are Murata GRM155 series (0402 size) and Inductor L1 is a Coilcraft 0603CS series (0603 size). For all frequency bands, the placement of C3 and C7 is critical. From 2500 MHz to 2700 MHz, the placement of C1 is also important. Table 6 lists the recommended component placement for various frequencies.

A 5 V dc bias is supplied through L1 that is connected to RFOUT (Pin 3). In addition to C4, 10 nF and 10 μ F power supply decoupling capacitors are also required. The typical current consumption for the ADL5321 is 90 mA.



SOLDERING INFORMATION AND RECOMMENDED PCB LAND PATTERN

Figure 21 shows the recommended land pattern for the ADL5321. To minimize thermal impedance, the exposed paddle on the SOT-89 package underside is soldered down to a ground plane along with (GND) Pin 2. If multiple ground layers exist, they should be stitched together using vias. For more information on land pattern design and layout, refer to the AN-772 application note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

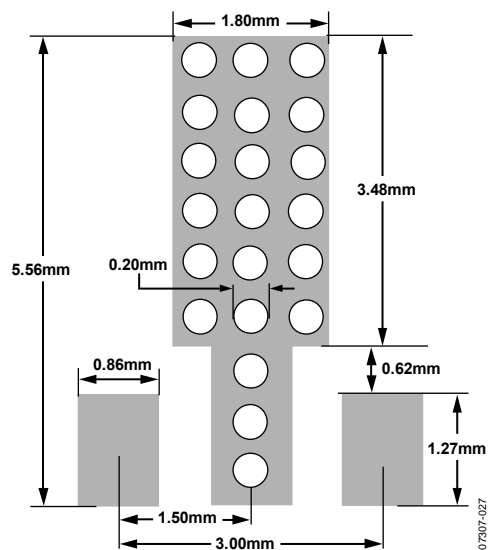


Table 5. Recommended Components for Basic Connections

Frequency (MHz)	C1 (pF)	C2 (pF)	C3 (pF)	C4 (pF)	C7 (pF)	L1 (nH)
2500 to 2700	1.0	10	1.2	10	Open	9.5
3400 to 3850	10	10	1.2	10	1.0	9.5

Table 6. Matching Component Spacing

Frequency (MHz)	λ 1 (mils)	λ 2 (mils)	λ 3 (mils)	λ 4 (mils)
2500 to 2700	240	75	89	325
3400 to 3850	90	35	40	416

MATCHING PROCEDURE

The ADL5321 is designed to achieve excellent gain and IP3 performance. To achieve this, both input and output matching networks must present specific impedance to the device. The matching components listed in Table 5 were chosen to provide –14 dB input return loss while maximizing OIP3. The load-pull plots (see Figure 22, Figure 23, and Figure 24) show the load impedance points on the Smith chart where optimum OIP3, gain, and output power can be achieved. These load impedance values (that is, the impedance that the device sees when looking into the output matching network) are listed in Table 7 and Table 8 for maximum gain and maximum OIP3, respectively. The contours show how each parameter degrades as it is moved away from the optimum point.

From the data shown in Table 7 and Table 8, it becomes clear that maximum gain and maximum OIP3 do not occur at the same impedance. This can also be seen on the load-pull contours in Figure 22 through Figure 24. Therefore, output matching generally involves compromising between gain and OIP3. In addition, the load-pull plots demonstrate that the quality of the output impedance match must be compromised to optimize gain and/or OIP3. In most applications where line lengths are short and where the next device in the signal chain presents a low input return loss, compromising on the output match is acceptable.

To adjust the output match for operation at a different frequency or if a different trade-off between OIP3, gain, and output impedance is desired, the following procedure is recommended.

For example, to optimize the ADL5321 for optimum OIP3 and gain at 2300 MHz, use the following steps:

1. Install the recommended tuning components for a 2500 MHz to 2700 MHz tuning band, but do not install C3 and C7.
2. Connect the evaluation board to a vector network analyzer so that input and output return loss can be viewed simultaneously.
3. Starting with the recommended values and positions for C3 and C7, adjust the positions of these capacitors along the transmission line until the return loss and gain are acceptable. Push-down capacitors that are mounted on small sticks can be used in this case as an alternative to soldering. If moving the component positions does not yield satisfactory results, then the values of C3 and C7 should be increased or decreased (most likely increased in this case because the user is tuning for a lower frequency). Repeat the process.
4. Once the desired gain and return loss are realized, OIP3 should be measured. It may be necessary to go back and forth between return loss/gain and OIP3 measurements (probably compromising most on output return loss) until an acceptable compromise is achieved.

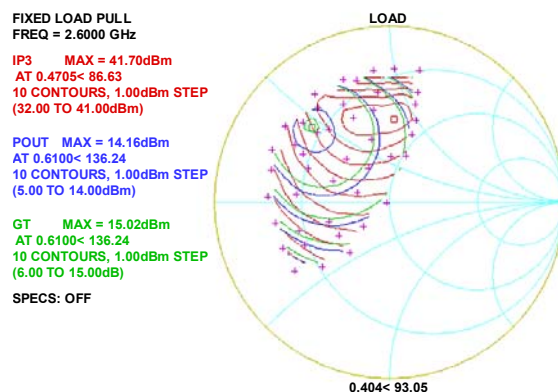


Figure 22. Load-Pull Contours, 2600 MHz

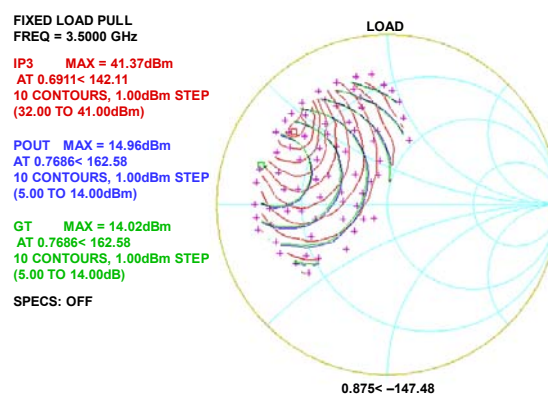


Figure 23. Load-Pull Contours, 3500 MHz

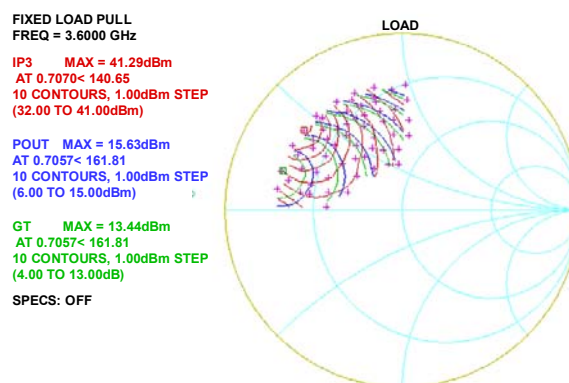


Figure 24. Load-Pull Contours, 3600 MHz

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Table 7. Load Conditions for Gain_{MAX}

Frequency (MHz)	Γ_{Load} (Magnitude)	Γ_{Load} (°)	Gain _{MAX} (dB)
2600	0.6100	136.24	15.02
3500	0.7686	162.58	14.02
3600	0.7057	161.81	13.44

Table 8. Load Conditions for OIP₃_{MAX}

Frequency (MHz)	Γ_{Load} (Magnitude)	Γ_{Load} (°)	IP ₃ _{MAX} (dBm)
2600	0.4705	86.63	41.7
3500	0.6911	142.11	41.37
3600	0.7070	140.65	41.29

WiMAX OPERATION

Figure 25 shows a plot of adjacent channel leakage ratio (ACLR) vs. P_{OUT} for the ADL5321. The signal type used is a WiMAX, 64 QAM, single carrier with a 10 MHz channel bandwidth. This signal is generated by a WiMAX-enabled source and followed with suitable band-pass filtering. The band-pass filter helps reduce the adjacent and alternate channel noise and distortion out of the signal generator down to -63 dB in the adjacent channels and -76 dB in the alternate channels at 2.6 GHz and -60 dB at 3.5 GHz.

Below an output power of 7 dBm, measured ADL5321 output spectral performance is limited by the signal quality from the signal source used (-63 dB at 2.6 GHz and -60 dB at 3.5 GHz). At high power operation, input power to the ADL5321 is 1 dBm for 15 dBm output power and the source ACLR is -60.2 dB. It is expected that with a better signal source, the ADL5321 output spectral quality improves further, especially at output power levels ≤10 dBm. For instance, the ADL5373 quadrature modulator measured ACLR is -69 dB for an output power of -10 dBm.

For output powers up to 10 dBm rms, the ADL5321 adds very little distortion to the output spectrum. At 2.6 GHz, the ACLR is -59 dB and a relative constellation error of -46.6 dB (<0.5% EVM) at an output power of 10 dBm rms.

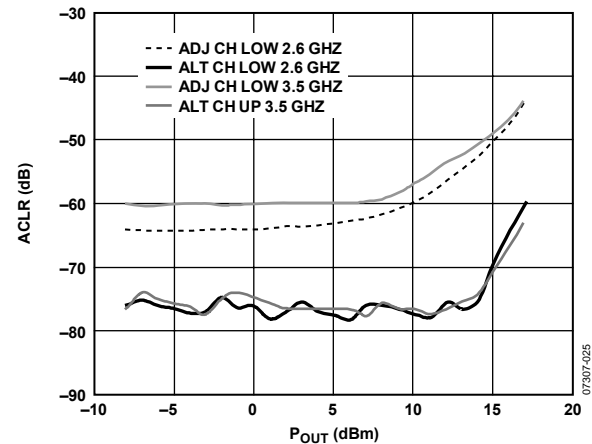


Figure 25. ACLR vs. P_{OUT}, WiMAX 64 QAM, 10 MHz Bandwidth, Single Carrier

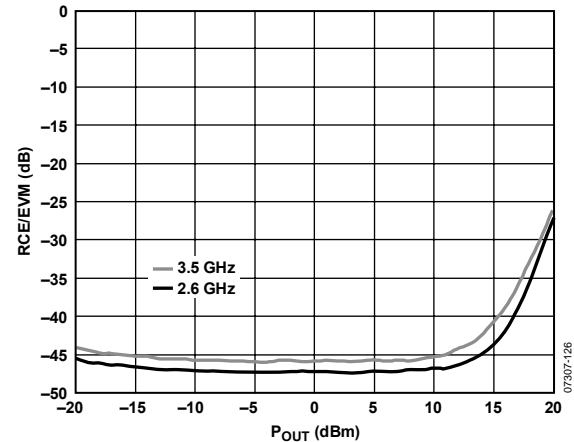


Figure 26. RCE/EVM vs. P_{OUT}, WiMAX 64 QAM, 10 MHz Bandwidth, Single Carrier

EVALUATION BOARD

The schematic of the ADL5321 evaluation board is shown in Figure 27. This evaluation board uses 25 mil wide traces and is made from IS410 material (lead-free version of FR4). The evaluation board comes tuned for operation in the 2500 MHz to 2700 MHz tuning band. Tuning options for other frequency bands

are also provided in Table 9. The recommended placement for these components is provided in Table 10. The inputs and outputs should be ac-coupled with appropriately sized capacitors. DC bias is provided to the amplifier via an inductor connected to the RFOUT pin. A bias voltage of 5 V is recommended.

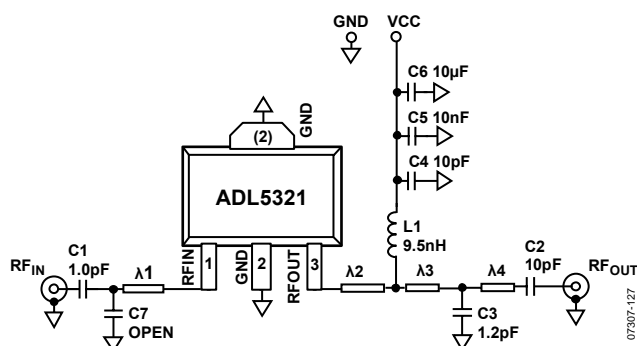


Figure 27. Evaluation Board, 2500 MHz to 2700 MHz

Table 9. Evaluation Board Configuration Options

Component	Function	2500 MHz to 2700 MHz	3400 MHz to 3850 MHz
C1, C2	AC coupling capacitors	C1 = 0402, 1.0 pF C2 = 0402, 10 pF	C1 = 0402, 10 pF C2 = 0402, 10 pF
C4, C5, C6	Power supply bypassing capacitors	C4 = 0603, 10 pF C5 = 0603, 10 nF C6 = 1206, 10 μF	C4 = 0603, 10 pF C5 = 0603, 10 nF C6 = 1206, 10 μF
L1	DC bias inductor	0603, 9.5 nH	0603, 9.5 nH
C3, C7	Tuning capacitors	C3 = 0402, 1.2 pF C7 = 0402, open	C3 = 0402, 1.2 pF C7 = 0402, 1.0 pF
VCC, GND	Power supply connections	VCC, red test loop GND, black test loop	VCC, red test loop GND, black test loop

Table 10. Recommended Component Spacing on Evaluation Board

Frequency (MHz)	λ1 (mils)	λ2 (mils)	λ3 (mils)	λ4 (mils)
2500 to 2700	240	75	89	325
3400 to 3850	90	35	40	416

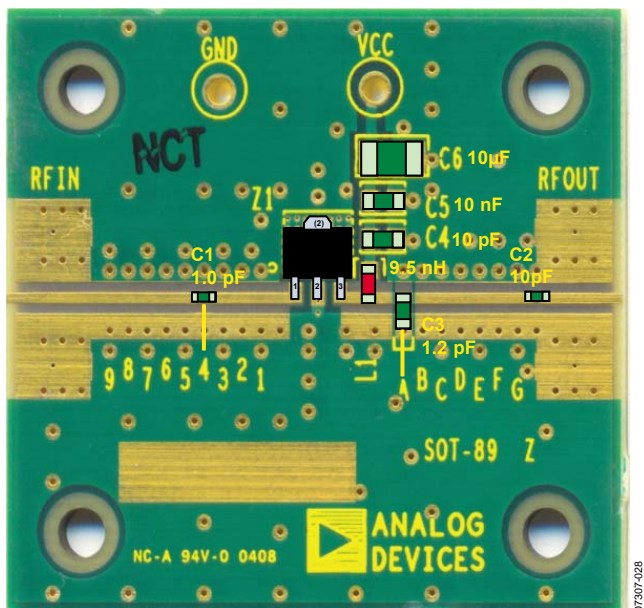


Figure 28. Evaluation Board Layout and Default Component Placement for Operation from 2500 MHz to 2700 MHz (Note: C7 Is Not Placed)

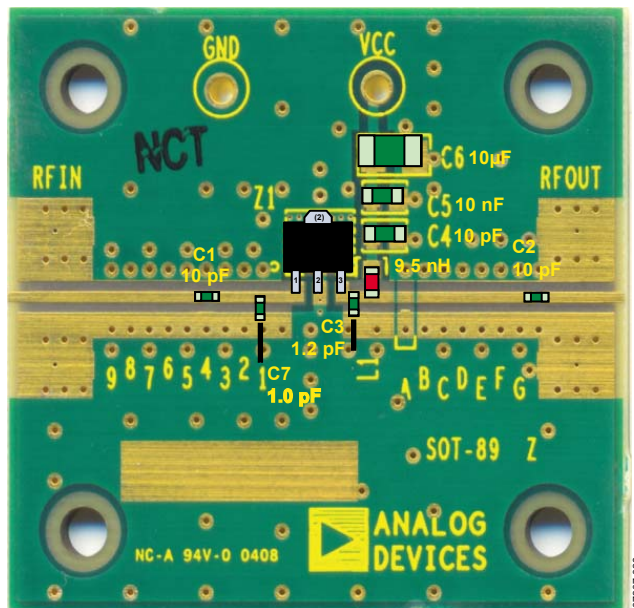


Figure 29. Evaluation Board Layout and Component Placement for Operation from 3400 MHz to 3850 MHz

OUTLINE DIMENSIONS

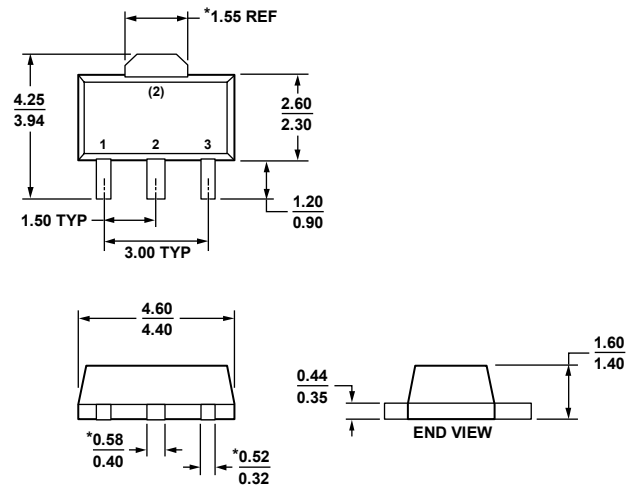


Figure 30. 3-Lead Small Outline Transistor Package [SOT-89]
(RK-3)
Dimensions shown in millimeters

040407-A

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADL5321ARKZ-R7 ¹	-40°C to +85°C	3-Lead SOT-89, 7" Tape and Reel	RK-3	Q0P
ADL5321-EVALZ ¹		Evaluation Board		

¹ Z = RoHS Compliant Part.

ADL5321

NOTES