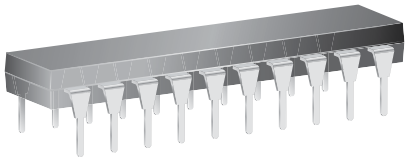
8-Bit Serial Input DMOS Power Driver

Features and Benefits

- 50 V minimum output clamp voltage
- 250 mA output current (all outputs simultaneously)
- 1.3 Ω typical $r_{DS(on)}$
- Low power consumption
- Replacements for TPIC6595N and TPIC6595DW

Package: 20-pin DIP (suffix A)



Not to scale

Description

The A6595 combines an 8-bit CMOS shift register and accompanying data latches, control circuitry, and DMOS power driver outputs. Power driver applications include relays, solenoids, and other medium-current or high-voltage peripheral power loads.

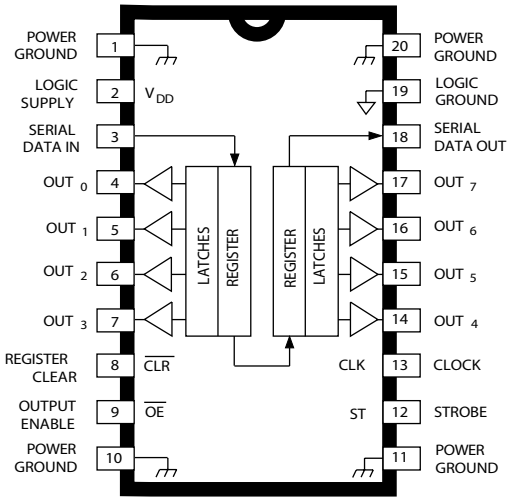
The serial-data input, CMOS shift register and latches allow direct interfacing with microprocessor-based systems. Serial-data input rates are over 5 MHz. Use with TTL may require appropriate pull-up resistors to ensure an input logic high.

A CMOS serial-data output enables cascade connections in applications requiring additional drive lines.

The A6595 DMOS open-drain outputs are capable of sinking up to 750 mA. All of the output drivers are disabled (the DMOS sink drivers turned off) by the OUTPUT ENABLE input high.

The A6595 is furnished in a 20-pin dual in-line plastic package that is lead (Pb) free, with 100% matte tin leadframe plating. Copper leadframe base material, reduced supply current requirements, and low on-state resistance allow the device to sink 150 mA from all outputs continuously, to ambient temperatures to 125°C.

Pin-out Diagram



Selection Guide

Part Number	Packing
A6595KA-T	18 pieces per tube

Absolute Maximum Ratings*

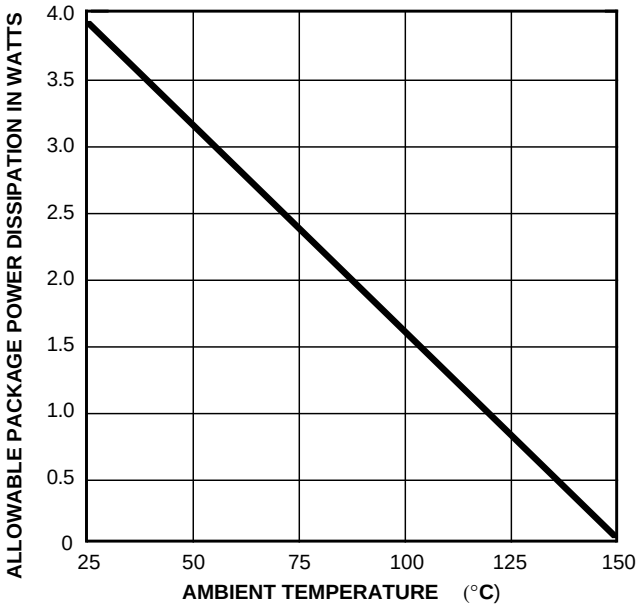
Characteristic	Symbol	Notes	Rating	Units
Logic Supply Voltage	V_{DD}		7.0	V
Input Voltage Range	V_I		–0.3 to 7.0	V
Output Voltage	V_O		50	V
Output Drain Current	I_O	Continuous, each output, all outputs on	250	mA
	I_{OM}	Pulsed t_w ≤100 µs, duty cycle ≤ 2%; each output, all outputs on	750	mA
		Pulsed t_w ≤100 µs, duty cycle ≤ 2%;	2.0	A
Single-Pulse Avalanche Energy	E_{AS}		75	mJ
Operating Ambient Temperature	T_A	Range K	–40 to 125	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

*These CMOS devices have input static protection (Class 3) but are still susceptible to damage if exposed to extremely high static electrical charges.

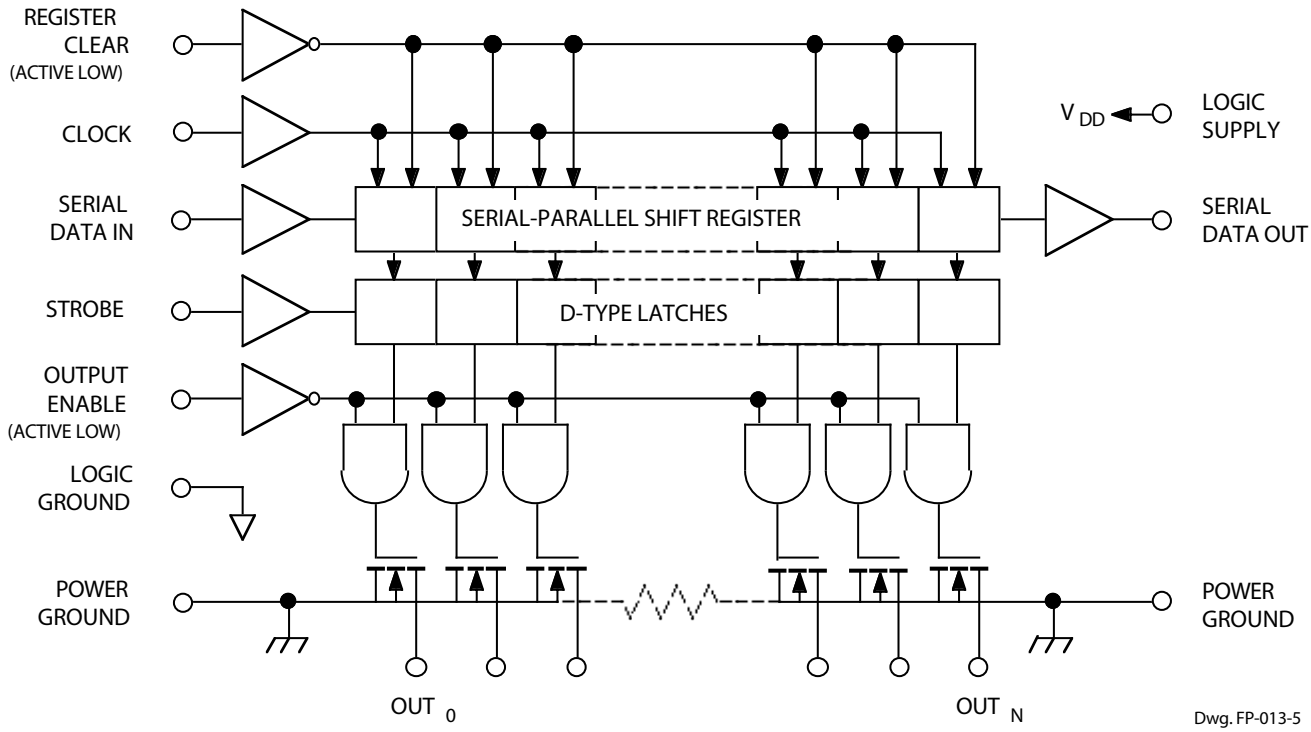
Thermal Characteristics may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	32	ºC/W

*Additional thermal information available on the Allegro website.

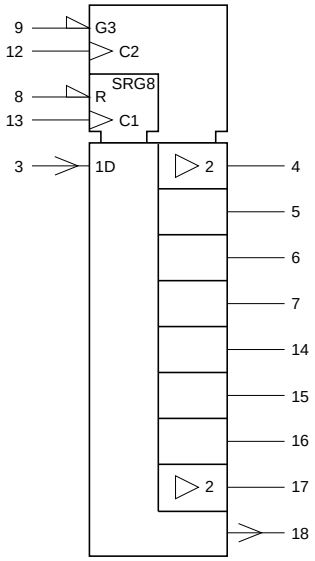


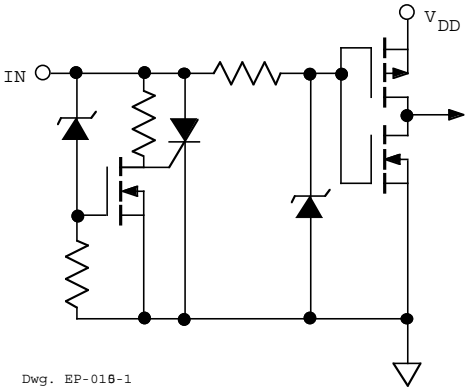
Functional Block Diagram



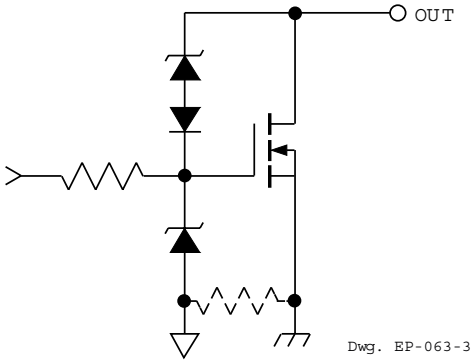
Grounds (terminals 1, 10, 11, 19, and 20) must be connected together externally.

Device Logic Diagram





LOGIC INPUTS

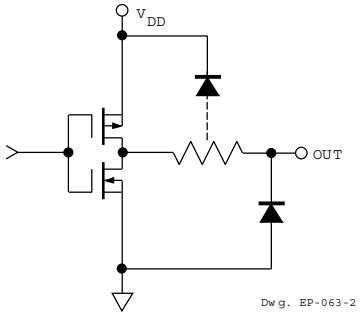


DMOS POWER DRIVER OUTPUT

RECOMMENDED OPERATING CONDITIONS

over operating temperature range

Logic Supply Voltage Range, V_{DD} ..... 4.5 V to 5.5 V
High-Level Input Voltage, V_{IH} ..... $\geq 0.85V_{DD}$
Low-level input voltage, V_{IL} ..... $\leq 0.15V_{DD}$



SERIAL DATA OUT

TRUTH TABLE

Data Input	Clock Input	Shift Register Contents						Serial Data Output	Strobe	Latch Contents						Output Enable	Output Contents					
		I_0	I_1	I_2	...	I_6	I_7			I_0	I_1	I_2	...	I_6	I_7		I_0	I_1	I_2	...	I_6	I_7
H	⌐	H	R_0	R_1	...	R_5	R_6	R_6														
L	⌐	L	R_0	R_1	...	R_5	R_6	R_6														
X	⌐	R_0	R_1	R_2	...	R_6	R_7	R_7														
		X	X	X	...	X	X	X	—	R_0	R_1	R_2	...	R_6	R_7							
		P_0	P_1	P_2	...	P_6	P_7	P_7	⌐	P_0	P_1	P_2	...	P_6	P_7	L	P_0	P_1	P_2	...	P_6	P_7
										X	X	X	...	X	X	H	H	H	H	...	H	H

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous Stat e

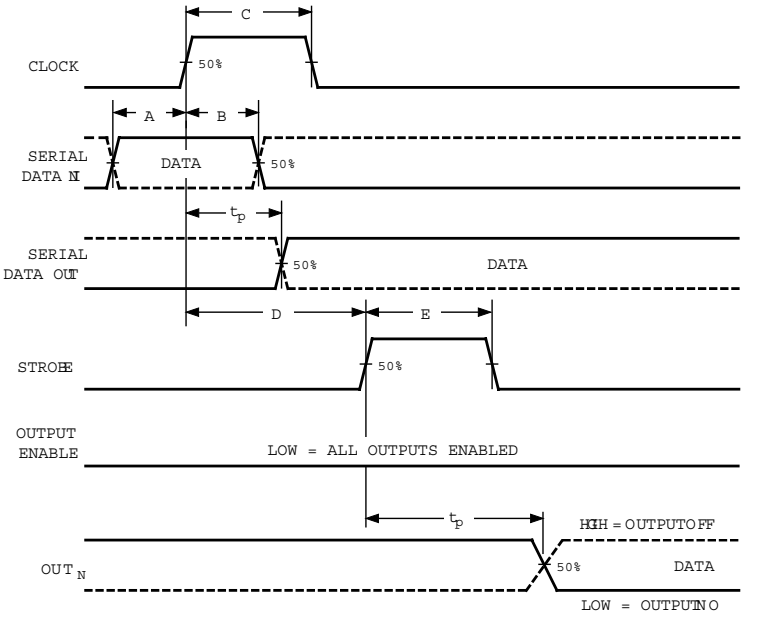
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V, $t_{ir} = t_{if} \leq 10$ ns (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Breakdown Voltage	$V_{(BR)DSX}$	I_O = 1 mA	50	—	—	V
Off-State Output Current	I_{DSX}	V_O = 40 V	—	0.05	1.0	µA
		V_O = 40 V, T_A = 125°C	—	0.15	5.0	µA
Static Drain-Source On-State Resistance	$r_{DS(on)}$	I_O = 250 mA, V_{DD} = 4.5 V	—	1.3	2.0	Ω
		I_O = 250 mA, V_{DD} = 4.5 V, T_A = 125°C	—	2.0	3.2	Ω
		I_O = 500 mA, V_{DD} = 4.5 V (see note)	—	1.3	2.0	Ω
Nominal Output Current	I_{ON}	$V_{DS(on)}$ = 0.5 V, T_A = 85°C	—	250	—	mA
Logic Input Current	I_{IH}	$V_I = V_{DD}$ = 5.5 V	—	—	1.0	µA
	I_{IL}	V_I = 0, V_{DD} = 5.5 V	—	—	-1.0	µA
Logic Input Hysteresis	$V_{I(hys)}$		—	1.3	—	V
SERIAL-DATA Output Voltage	V_{OH}	I_{OH} = -20 µA, V_{DD} = 4.5 V	4.4	4.49	—	V
		I_{OH} = -4 mA, V_{DD} = 4.5 V	4.1	4.3	—	V
	V_{OL}	I_{OL} = 20 µA, V_{DD} = 4.5 V	—	0.002	0.1	V
		I_{OL} = 4 mA, V_{DD} = 4.5 V	—	0.2	0.4	V
Prop. Delay Time	t_{PLH}	I_O = 250 mA, C_L = 30 pF	—	650	—	ns
	t_{PHL}	I_O = 250 mA, C_L = 30 pF	—	150	—	ns
Output Rise Time	t_r	I_O = 250 mA, C_L = 30 pF	—	7500	—	ns
Output Fall Time	t_f	I_O = 250 mA, C_L = 30 pF	—	425	—	ns
Supply Current	$I_{DD(OFF)}$	All inputs low	—	15	100	µA
	$I_{DD(ON)}$	V_{DD} = 5.5 V, Outputs on	—	150	300	µA
	$I_{DD(fclk)}$	f_{clk} = 5 MHz, C_L = 30 pF, Outputs off	—	0.6	5.0	mA

Typical Data is at VDD = 5 V and is for design information only.
NOTE — Pulse test, duration ≤100 µs, duty cycle ≤2%.

TIMING REQUIREMENTS and SPECIFICATIONS

(Logic Levels are V_{DD} and Ground)



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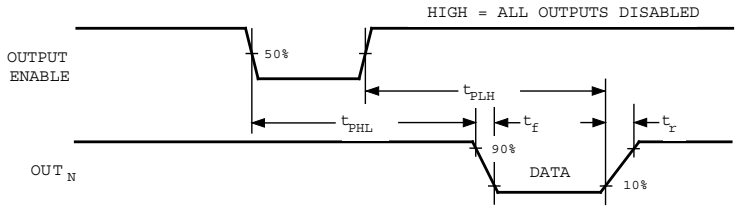


Dwg. WP-030-2

A. Data Active Time Before Clock Pulse (Data Set-Up Time), $t_{su(D)}$ ..... **10 ns**

B. Data Active Time After Clock Pulse (Data Hold Time), $t_{h(D)}$ ..... **10 ns**

C. Clock Pulse Width, $t_{w(CLK)}$ ..... **20 ns**

D. Time Between Clock Activation and Strobe, $t_{su(ST)}$ ..... **50 ns**

E. Strobe Pulse Width, $t_{w(ST)}$ ..... **50 ns**

F. Output Enable Pulse Width, $t_{w(OE)}$ ..... **4.5 µs**

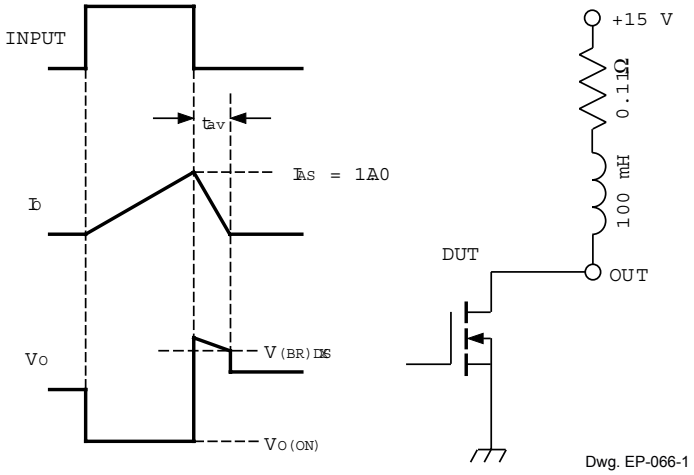
NOTE – Timing is representative of a 12.5 MHz clock. Higher speeds are attainable.

Serial data present at the input is transferred to the shift register on the rising edge of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT.

Information present at any register is transferred to the respective latch on the rising edge of the STROBE input pulse (serial-to-parallel conversion).

When the OUTPUT ENABLE input is high, the output source drivers are disabled (OFF). The information stored in the latches is not affected by the OUTPUT ENABLE input. With the OUTPUT ENABLE input low, the outputs are controlled by the state of their respective latches.

TEST CIRCUITS



$$E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{AV}/2$$

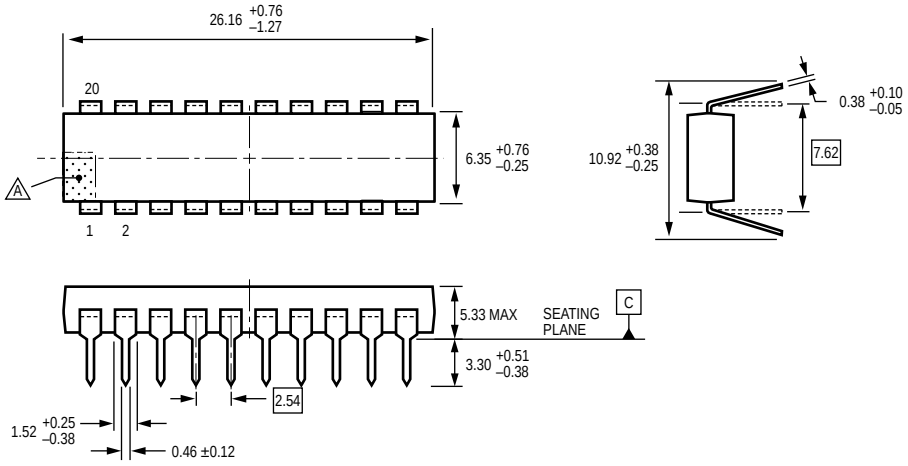
Single-Pulse Avalanche Energy Test Circuit and Waveforms

TERMINAL DESCRIPTIONS

Terminal No.	Terminal Name	Function
1	POWER GROUND	Reference terminal for output voltage measurements (OUT_{0-3}).
2	LOGIC SUPPLY	(V_{DD}) The logic supply voltage (typically 5 V).
3	SERIAL DATA IN	Serial-data input to the shift-register.
4-7	OUT_{0-3}	Current-sinking, open-drain DMOS output terminals.
8	CLEAR	When (active) low, the registers are cleared (set low).
9	OUTPUT ENABLE	When (active) low, the output drivers are enabled; when high, all output drivers are turned OFF (blanked).
10	POWER GROUND	Reference terminal for output voltage measurements (OUT_{0-3}).
11	POWER GROUND	Reference terminal for output voltage measurements (OUT_{0-7}).
12	STROBE	Data strobe input terminal; shift register data is latched on rising edge.
13	CLOCK	Clock input terminal for data shift on rising edge.
14-17	OUT_{4-7}	Current-sinking, open-drain DMOS output terminals.
18	SERIAL DATA OUT	CMOS serial-data output to the following shift register.
19	LOGIC GROUND	Reference terminal for input voltage measurements.
20	POWER GROUND	Reference terminal for output voltage measurements (OUT_{4-7}).

NOTE — Grounds (terminals 1, 10, 11, 19, and 20) must be connected together externally.

Package A, 20-Pin DIP



Preliminary dimensions, for reference only
Dimensions in inches
Metric dimensions (mm) in brackets, for reference only
(reference JEDEC MS-001 AD)
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown
A Terminal #1 mark area

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