Valley Current Mode Control Buck Converter

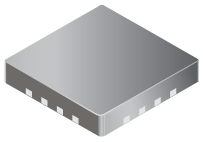
Features and Benefits

- Extremely fast load-transient response with minimal output voltage delta
- Achieves high step-down ratios with on-times < 50 ns
- User-configurable on-time, achieving switching frequencies up to 2 MHz
- Minimal external components required
- Optimized for low value filter capacitors and inductors
- Wide input voltage range: 9 to 46 V
- Output Current: 3 A
- Low standby current <100 µA
- Supplied in thermally-enhanced QFN package

Applications:

- Printers, scanners
- Cable, DSL modems/routers
- Network and telecom
- Industrial control
- Distributed power systems
- Set top box
- High power LED supply
- Battery chargers
- GPS/ Infotainment

Package 16-contact QFN (suffix EU):



4 mm × 4 mm × 0.75 mm

Description

The A4403 is a buck converter that uses valley current-mode control. This control scheme allows very short switch on-times to be achieved, making it ideal for applications that require high switching frequencies combined with high input voltages and low output voltages.

Low cost is accomplished through high switching frequencies of up to 2 MHz, allowing smaller and lower value inductors and capacitors. In addition, minimal external components are required through high levels of integration. Optimal drive circuits are utilized to minimize switching losses.

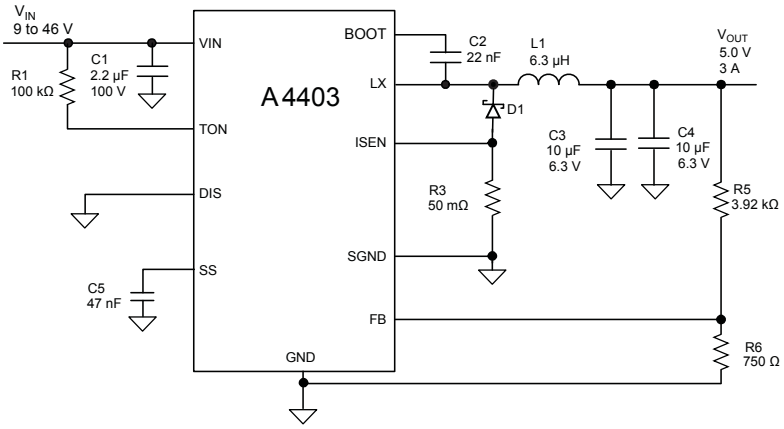
The switching frequency is maintained constant, as the on-time is modulated by the input voltage. This feed-forward control ensures excellent line correction. The on-time is set by an external resistor pulled-up to the input supply.

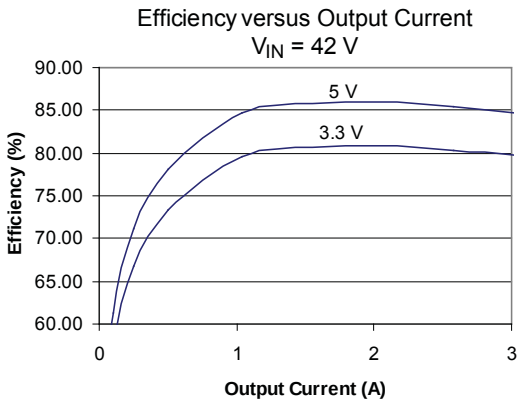
When power is initially applied and the device is enabled, a user-configurable soft-start function occurs to minimize inrush current and to prevent output overshoot. Internal housekeeping and bootstrap supplies are provided which only require the addition of one small ceramic capacitor. A top-off charge pump is also provide to ensure correct operation at light loads.

Internal diagnostics provide comprehensive protection against overcurrents, input undervoltages, and overtemperatures.

The device package is a 16-contact, 4 mm × 4 mm, 0.75 mm nominal overall height QFN, with exposed pad for enhanced thermal dissipation. It is lead (Pb) free, with 100% matte tin leadframe plating.

Typical Application Diagram





All capacitors are X5R or X7R ceramic
Resistors R3 and R4 should be surface mount, low inductance type, rated at 250 mW at 70°C

Selection Guide

Part Number	Packing	Package
A4403GEU-T	92 pieces per tube	16-contact 4 mm × 4 mm QFN with exposed thermal pad
A4403GEUTR-T	1500 pieces per 7-in. reel	

Absolute Maximum Ratings (reference to GND)

Characteristic	Symbol	Notes	Rating	Units
VIN Pin Supply Voltage	V_{IN}		–0.3 to 50	V
LX Pin Switching Node Voltage	V_{LX}		–1 to 50	V
ISEN Pin Current Sense Voltage	V_{ISEN}		–1.0 to 0.5	V
DIS Pin Disable Voltage	V_{DIS}		–0.3 to 7	V
TON Pin On-Time Voltage	V_{TON}		–0.3 to 50	V
Operating Ambient Temperature	T_A	Range G	–40 to 105	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

Recommended Operating Conditions

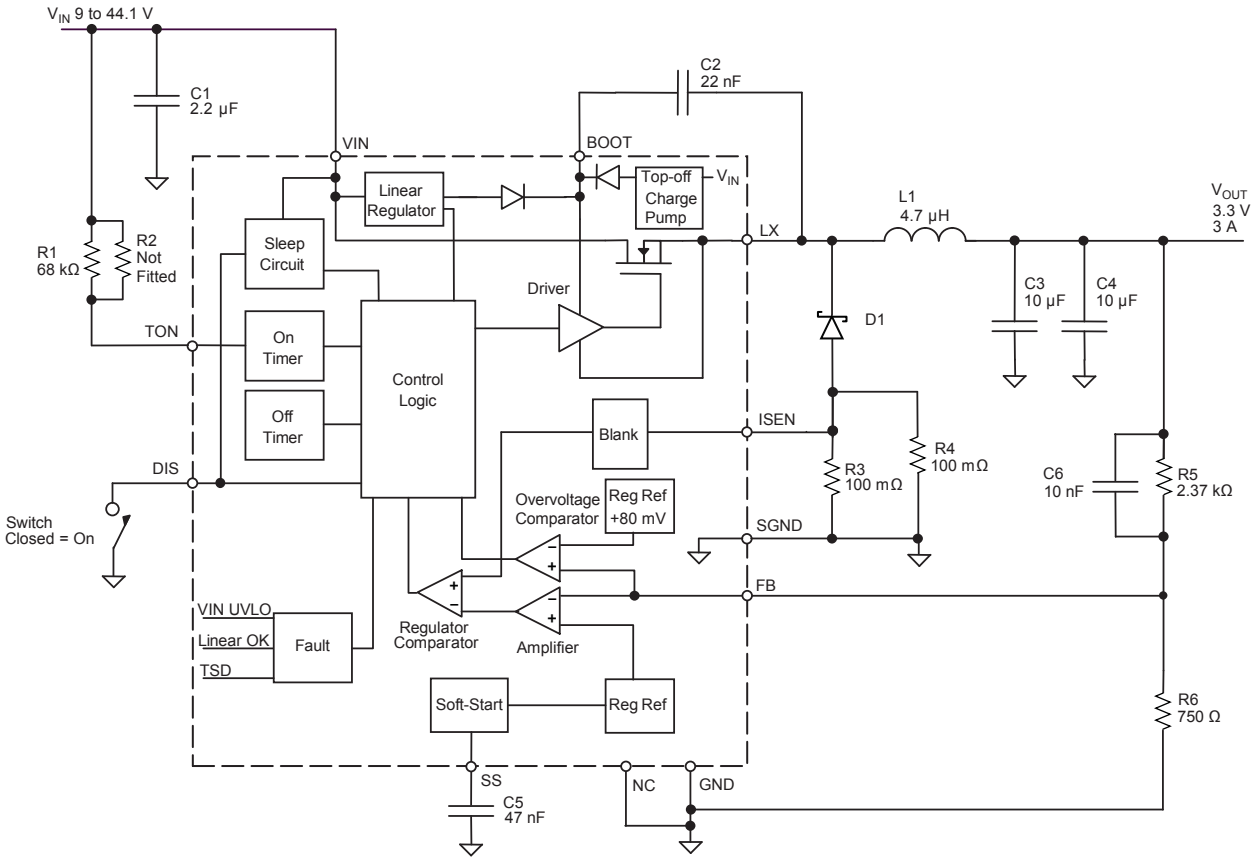
Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{IN}		9	–	46	V
Switching Node	V_{LX}		–0.7	–	46	V
Switching Frequency Range	f_{SW}	Continuous conduction mode	0.45	–	2	MHz
Operating Ambient Temperature	T_A		–40	–	105	ºC
Junction Temperature	T_J		–40	–	125	ºC

Thermal Characteristics may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	36	ºC/W
Package Thermal Resistance, Junction to Pad	$R_{\theta JP}$	On 4-layer PCB based on JEDEC standard	2	ºC/W

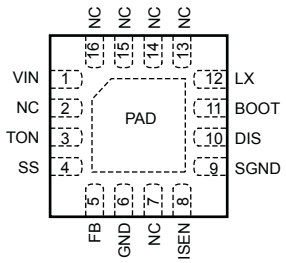
*Additional thermal information available on the Allegro website.

Functional Block Diagram



Switching Frequency = 1 MHz
All capacitors are X5R or X7R ceramic
Resistors R3 and R4 should be surface mount, low inductance type, rated at 250 mW at 70°C
C6 is an optional speed-up capacitor, to improve the transient response

Pin-out Diagram



(Top View)

Terminal List Table

Number	Name	Function
1	VIN	Input supply
2, 7, 13, 14, 15, 16	NC	No connection; tie to GND
3	TON	Terminal for on-time setting with external resistor
4	SS	Terminal for soft-start setting with external capacitor
5	FB	Feedback terminal
6	GND	Ground terminal
8	ISEN	Current sense input
9	SGND	Current sense ground reference
10	DIS	Disable logic input; active high
11	BOOT	Bootstrap supply node
12	LX	Switch node
–	PAD	Exposed thermal pad; connect to ground plane (GND) by through-hole vias

ELECTRICAL CHARACTERISTICS[1] valid at T_J = 25°C, V_{IN} = 9 to 46 V, unless otherwise noted

Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Units
General						
V_{IN} Quiescent Current	I_{VINOFF}	DIS = high, VIN = 46 V	–	–	100	µA
	I_{VINON}	DIS = low, VIN = 46 V, I_{LOAD}= 1 mA	–	4.3	5.5	mA
Feedback Voltage	V_{FB}	T_J = 25°C	0.792	0.8	0.808	V
Feedback Input Bias Current	I_{BIAS}		–400	–100	100	nA
Output Voltage Tolerance[2]	ΔV_{OUT}	I_{LOAD} = 1 mA to 3 A	–2.5	–	2.5	%
On-Time Tolerance	ΔT_{ON}	Based on selected value	–15	–	15	%
Minimum On-Time Period	$T_{on(min)}$		–	50	60	ns
Minimum Off-Time Period	$T_{off(min)}$		–	–	350	ns
Buck Switch On-Resistance	$R_{DS(on)}$	T_J = 25°C, I_{LOAD} = 3 A	–	350	–	mΩ
		T_J = 125°C, I_{LOAD} = 3 A	–	550	–	mΩ
Current Limit Threshold	I_{LIM}	Valley current in external sense resistors = 50 mΩ	3.0	3.6	4.2	A
Soft Start Current Source	I_{SS}		5	10	15	µA
Input						
DIS Input Voltage Threshold	V_{DIS}	Device enabled	–	–	1	V
DIS Open-Circuit Voltage	V_{DISOC}	Device disabled	2	–	7	V
DIS Input Current	I_{IN}	DIS = 0 V	–10	–	–1	µA
Protection						
FB Overvoltage Shutdown	V_{FBOV}		–	0.88	–	V
VIN Undervoltage Shutdown Threshold	V_{INUV}	Voltage rising	6.4	–	7.5	V
VIN Undervoltage Shutdown Hysteresis	$V_{INUV(hys)}$		0.7	–	1.1	V
Overtemperature Shutdown Threshold	T_{JTSD}	Temperature rising	–	165	–	°C
Overtemperature Shutdown Hysteresis	$T_{JTSD(hys)}$	Recovery = $T_{JTSD} - T_{JTSD(hys)}$	–	15	–	°C

[1]Specifications over the junction temperature range of –40°C to 125°C are assured by design and characterization.
[2]Average value of V_{OUT} relative to target voltage. Note that the tolerance effects of the feedback resistors are not taken into account. This figure does include the feedback voltage tolerance.

Functional Description

Basic Operation The A4403 is a buck converter that utilizes valley current-mode control. The on-time is set by the amount of current that flows into the TON pin. This is determined by the value of the TON resistors chosen (R1 and R2 in the Functional Block diagram) and the magnitude of the input voltage, V_{IN}. Under a specific set of conditions, an on-time can be set that then dictates the switching frequency. This switching frequency remains reasonably constant throughout load and line conditions as the on-time varies inversely with the input voltage. The Switch On-Time and Switching Frequency section provides more details on this subject.

At the beginning of the switching cycle, the buck switch is turned on for a fixed period that is determined by the current flowing into TON. Once the current comparator trips, a one-shot monostable, the On Timer, is reset, turning off the switch. The current through the inductor then decays. This current is sensed through the external sense resistors (R3 and R4), and then compared against the current-demand signal. The current-demand signal is generated by comparing the output voltage against an accurate bandgap reference. After the current through the sense resistors decreases to the valley of the current-demand signal, the On Timer is set to turn the buck switch back on again and the cycle is repeated.

Under light load conditions, the converter automatically operates in pulse frequency modulation (PFM) mode to maintain regulation. This mode of operation ensures optimum efficiency as switching losses are reduced.

Overcurrent Protection The converter utilizes pulse-by-pulse valley current limiting, which operates when the current through the sense resistors, R3 and R4 (set for 50 mΩ by two 100 mΩ resistors in parallel), increases above 3.6 A typical at the valley point. The corresponding sense voltage (at the ISEN pin) that creates a current limiting condition is 180 mV typical. It is possible, by careful selection of the sense resistors, to reduce the current limit for systems with maximum loads of less than 3 A.

During an overload condition, the switch is turned on for the period determined by the constant on-time circuitry. The switch off-time is extended until the current decays to the current limit value of 3.6 A typical (which corresponds to a sense voltage of 180 mV). The switch is then turned on again.

Because no slope compensation is required in this control scheme, the current limit is maintained at a reasonably constant level across the input voltage range.

Figure 1 illustrates how the current is limited during an overload condition. The current decay (period with switch off) is proportional to the output voltage. As the overload is increased, the output voltage tends to decrease and the switching period increases.

Output Voltage Selection The output voltage of the converter is set by selecting the appropriate feedback resistors, using the following formula:

$$R_5 = R_6 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \quad , \tag{1}$$

where (refering to the Functional Block diagram):
R_6 has a value between 1 and 12 kΩ (R6 connected between the GND and FB pins),
R_5 is the dependent value (R5 connected between the output rail and the FB pin),
V_{OUT} is the user-configured output regulator voltage, and
V_{FB} is the reference voltage.

The tolerance of the feedback resistors influences the voltage setpoint. It is therefore important to consider the tolerance selection when targeting an overall regulation figure.

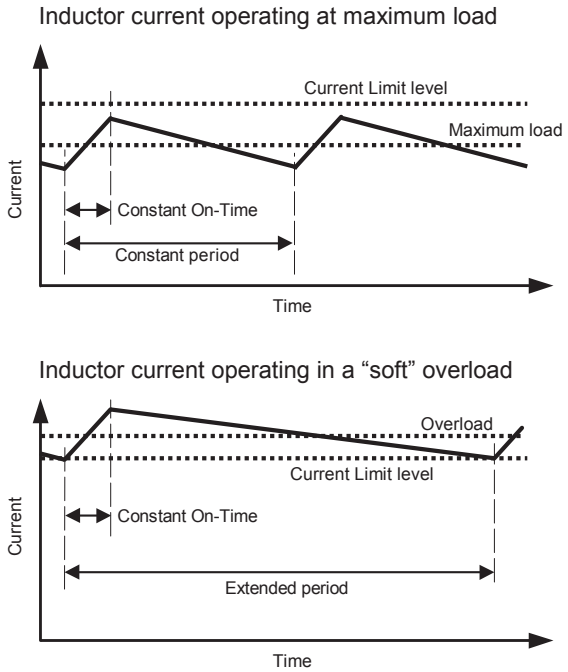


Figure 1. Current limiting during overload

In general, the feedback resistors should have the lowest resistance possible, to minimize any noise pick-up effects and to minimize voltage offsets on the output caused by the bias current, I_{BIAS}, flowing out of the FB node into R6. Reducing the feedback resistances does introduce another loading effect on the output, which has an effect on the standby current.

It should be noted that a minimum load of 1 mA is required (see the Light Load Operation section). This may be provided by the feedback resistors.

Disable The converter is enabled by pulling the DIS pin low. Once enabled, the output converter is started-up under the control of the soft-start routine.

To disable the converter, the DIS pin can simply be disconnected (open circuit).

Soft Start A soft-start routine is initiated when: DIS = 0, no thermal shutdown exists, and V_{IN} and the internal housekeeping supplies are above the minimum values. Note that an overcurrent event does not initiate a soft start, unless the converter is recovering from a thermal shutdown condition.

The soft-start routine controls the rate of rise of the reference voltage, which in turn controls the output voltage. This function minimizes the amount of inrush current drawn from VIN and potential voltage overshoot on the output rail, VOUT.

The soft-start period, T_{SS}, is set by an internal current source that charges the external capacitor (C5) connected to the SS pin. Control by the soft-start routine is completed when the SS pin reaches 0.8 V. The duration of T_{SS} is set by selecting the appropriate capacitance, according to the formula:

$$T_{SS} = \frac{C_5 \times 0.8}{10 \times 10^{-6}} \quad . \qquad (2)$$

Note: If the soft start function is not required for the application, a 220 kΩ resistor should be connected between the SS pin and GND. Without soft start, or with a soft start period that is too rapid, coupled with a high load that is present during start-up, the converter may operate in current limit, placing maximum stress on the input circuit.

Assuming no load is drawn until the start-up process is complete, the current drawn from the input supply is determined by how quickly the output capacitors (C3 and C4) are charged. The output capacitors are charged according to the following formula:

$$t_{CHARGE} = \frac{C_{OUT} \times V_{OUT}}{I_{VIN}} \quad , \qquad (3)$$

where I_{VIN} is the input supply current.

For example, if you limited I_{VIN} to 250 mA, and assumed V_{OUT} = 5 V and C_{OUT} = 20 µF, the soft start time could be determined as:

$$t_{CHARGE} = \frac{20\ \mu F \times 5\ V}{0.25\ A} = 400\ \mu s$$

This means a soft-start duration greater than 400 µs should be selected to ensure the inrush current is less than 250 mA.

Shutdown The converter is disabled in the event of either an overtemperature event, or an undervoltage on VIN (V_{INUVR}) or on an internal housekeeping supply.

As soon as any of the above faults have been removed and assuming DIS = 0, the output voltage, V_{OUT}, is brought-up under the control of the soft-start routine.

Output Overvoltage Protection In the event of an overvoltage condition appearing on the output rail, the FB terminal will also experience the overvoltage, scaled by the feedback resistors. If the FB terminal voltage rises above the nominal voltage by 10% (typical), the on-time of the buck switch will terminate and the switch will remain off until the FB voltage reduces to the correct V_{FB} range.

Switch On-Time and Switching Frequency The switch on-time effectively determines the operating frequency of the converter. The selection of the operating frequency is generally a trade-off between the size of the external passive components (inductor, and input and output capacitors) and switching losses. Another consideration in selecting the switching frequency is to ensure that none of the on- or off-time limits are reached under extreme conditions.

The minimum on-time occurs at maximum input voltage and minimum load. Consider the following example.

Given:

V_{IN} (max) = 46 V, V_{OUT} = 5 V, f_{SW} = 1 MHz, and:

$$T_{on}(min) = \left(\frac{V_{OUT} + V_f}{V_{IN} + V_f} \right) \times \frac{1}{f_{SW}} \quad , \qquad (4)$$

where V_f is the voltage drop of the recirculation diode (D1) and sense resistors (R3 and R4). Then, the minimum on-time is:

$$T_{on}(min) = \left(\frac{5 + 0.5}{46 + 0.5} \right) \times \frac{1}{1 \times 10^6} = 118\ ns$$

The specified minimum on-time, $T_{on(min)}$, is 60 ns maximum, so there is reasonable margin in this case.

The specified minimum off-time, $T_{off(min)}$, 350 ns maximum, also has to be considered. The minimum off-time occurs at minimum input voltage and maximum load. As was shown in the minimum on-time calculation (equation 4), you have to examine the extreme operating conditions to ensure adequate margin exists.

The switch on-time, T_{on}, is set by the current flowing into the TON pin. The current is determined by the input voltage, V_{IN}, and the resistor R1. The on-time can be found as:

$$T_{on} = \left(\frac{R_1}{V_{IN} \times 2.05 \times 10^{10}} \right) + 10 \times 10^{-9} \quad . \qquad (5)$$

The switching frequency may be slightly modulated by load changes. The on-time is always constant for a given input voltage and across the load range. To compensate for any losses in the circuitry (for example, in the series switch and inductor, or in the voltage drop across the recirculation diode), the off-time, hence the switching frequency, has to be adjusted. This effect is most noticeable at low input voltages and high output currents.

To calculate the actual switching frequency, the T_{on} of equation 5 can be used in conjunction with the transfer function of the converter:

$$f_{SW} = \left(\frac{V_{OUT} + V_f}{V_{IN} + V_f} \right) \times \frac{1}{T_{on}} \quad . \qquad (6)$$

An alternative approach to selecting the TON resistor (R1), to accomplish an approximate switching frequency is found in the following formula:

$$R_1 = \frac{V_{OUT} \times 2.05 \times 10^{10}}{f_{SW}} \quad . \qquad (7)$$

Figure 2 illustrates a range of switching frequencies that can be achieved with various TON resistances and output voltages.

Top-Off Charge Pump During light load operation, when operating in PFM mode, the top-off charge pump provides enough charge to drive the buck switch.

Light Load Operation To avoid the output voltage peak charging due to leakage effects from the buck switch and the charge pump recirculation current, a minimum load of 1 mA must be applied to the output.

The output feedback resistor network provides some loading. Depending on the values selected, this network may provide all, or at least some, of the minimum loading requirement.

Control Loop The process of closing the control loop for the A4403 has been greatly simplified through the integration of the compensation components into the device. The control loop bandwidth has been optimized for operation across the full input and output voltage range and for switching frequencies between 450 kHz and 2 MHz. Loop optimization is achieved with a 20 µF ceramic capacitor placed across the output (VOUT to GND) and a power inductor that achieves a peak to peak ripple current of around 720 mA. For example, for a 3.3 V output operating at a frequency of 1 MHz, the power inductor = 4.7 µH.

Larger output capacitors can be used; however, this tends to decrease the bandwidth of the control loop. Note that the output capacitance should not exceed 1000 µF or be less than 10 µF, as this may cause a loop instability to occur.

When the output voltage is set for 0.8 V, the typical bandwidth is 90 kHz with a phase margin of 45° at full load. As the load is

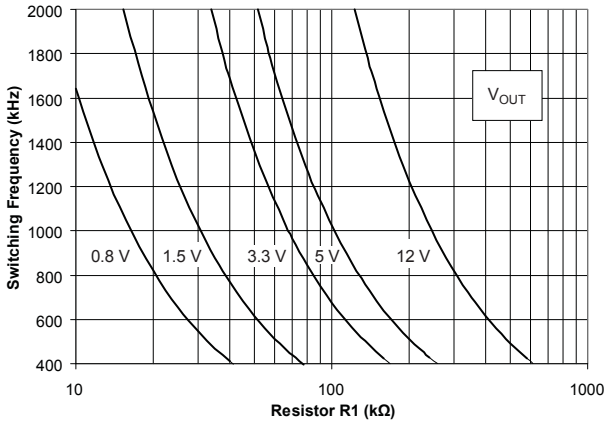


Figure 2. Switching frequencies versus TON resistor values, at various levels of V_{OUT}

reduced, the bandwidth remains largely constant; however, the phase margin tends to reduce slightly because the output power pole is shifted down in frequency, introducing the phase lag sooner. At light loads, before pulse frequency modulation occurs, the phase margin reduces to approximately 40°, which is reasonable given that it is the worst-case condition. Note that when pulse frequency modulation occurs, the system no longer operates as a linear system, therefore, the control laws do not apply.

When the output voltage is set for higher voltages, the DC gain is reduced by the resistor feedback network from the output. This effectively reduces the bandwidth of the control loop. An optional speed-up capacitor (C6) can be used in parallel with the feedback resistor (R5) to compensate for this effect. The addition of this capacitor introduces an additional zero which increases the gain and extends the bandwidth to maintain it in the region of 90 kHz. The position of the zero depends on the values of R5 and C6. The following time constants should be used for various output voltages:

Output Voltage (V)	Time Constant
5	3.6×10^{-5}
3.3	2.4×10^{-5}
2.5	1.8×10^{-5}
1.5	1.1×10^{-5}
0.8	Not required

For example, assume a target output voltage of 5 V, and an R5 of 16 kΩ to achieve that voltage. Then C6 = 2.28×10^{-8}. The nearest commonly available value is 2.2 nF.

Inductor The main factor in selecting the inductance value is the ripple current. The ripple current affects the output voltage ripple and also has an effect on the current limit. Because slope compensation is not used, the ripple current is not constrained by this factor.

A good starting point in selecting the inductance for a given application is to specify a maximum peak-to-peak ripple current of about 25% of the maximum load. The equates to a ripple current of approximately 750 mA for a maximum load of 3 A. This often gives a good compromise between size, cost, and performance.

The maximum peak to peak ripple current, I_{RIPP}, occurs at the maximum input voltage. Therefore the duty cycle, D, should be found under these conditions:

$$D\,(\min) = \frac{V_{OUT} + V_f}{V_{IN}(\max) + V_f} \quad , \tag{8}$$

where V_f is the forward voltage drop of the recirculation diode and the sense resistor.

The required inductance can be found:

$$L\,(\min) = \frac{V_{IN} - V_{OUT}}{I_{RIPP}} \times D\,(\min) \times \frac{1}{f_{SW}(\min)} \quad . \tag{9}$$

Note that the manufacturers inductance tolerance should also be taken into account. This value may be as high as ±20%.

In addition, because the control is dependant on the valley signal, it is important to consider the minimum peak to peak valley voltage that is developed across the sense resistor. The minimum peak to peak ripple current occurs at minimum input voltage. The peak to peak voltage is simply the peak to peak current multiplied by the sense resistor value. It is recommended that the peak to peak sense voltage should be greater than 25 mV.

It is recommended that gapped ferrite solutions be used as opposed to powdered iron solutions. The latter exhibit relatively high core losses that can have a large impact on long term reliability.

Inductors are typically specified at two current levels:

- rms current. It is important to understand how the rms current level is specified, in terms of ambient temperature. Some manufacturers quote an ambient only, whilst others quote a temperature that includes a self-temperature rise. For example, if an inductor is rated for 85°C and includes a self-temperature rise of 25°C at maximum load, then the inductor cannot be safely operated beyond an ambient temperature of 60°C at full load. The rms current can be assumed to be simply the maximum load current, with perhaps some margin to allow for overloads, and so forth.
- saturation current. The worst case maximum peak current should not exceed the saturation current and indeed some margin should be allowed. The maximum peak current can be found

to ensure the saturation current level of the chosen inductor is not exceeded:

$$I_{sat} = I_{LOAD} + \frac{I_{RIPPLE}}{2} \quad . \tag{10}$$

It is important to ensure that, under worst-case conditions (minimum input voltage, maximum load current, minimum inductance, and minimum switching frequency), that the minimum current limit is not exceeded and in fact has some margin. The current limit is measured at the valley level. The maximum current at the valley is found from:

$$I_{valley} = I_{LOAD} - \frac{I_{RIPPLE}}{2} \quad . \tag{11}$$

The minimum current limit threshold should be at least 20% above this level.

Recommended inductor manufacturers and ranges are:

• Tayo Yuden: NR6045 series

• Sumida: CDR7D43MN series

Output Capacitor In the interests of size, cost, and performance, this control architecture has been designed for ceramic capacitors. It is imperative that ceramic X5R or X7R capacitors are used. On no account should Y5V, Y5U, Z5U, or similar types be used.

When using ceramic capacitors, another important consideration is the E-field effects on the actual value of the capacitor. To minimize the effects of the capacitance being reduced with output voltage, it is recommended that the working voltage of the capacitor be considerably more than the set output voltage. Check with the vendor to obtain this information.

The output capacitor determines the output voltage ripple and is used to close the control loop. As outlined in the Control Loop section, the bandwidth has been optimized for an output capacitance of 20 µF.

If a particular application requires an extremely low output voltage, the output capacitor can be increased. Any increase will tend to reduce the bandwidth and therefore compromise the transient response performance.

In general the output capacitance should not exceed 1000 µF or be less than 10 µF, as this may cause a loop instability to occur.

The output ripple is largely determined by the output capacitance, and the effects of esr and esl can largely be ignored assuming good layout practice is observed. To help reduce the effects of esl it is a good idea to split the 20 µF capacitance into two separate 10 µF components.

The output voltage ripple can be approximated to:

$$V_{RIPPLE} \approx \frac{I_{RIPPLE}}{8 \times f_{SW} \times C_{OUT}} \quad , \tag{12}$$

where I_{RIPPLE} is as found in the Inductor section.

When using ceramic capacitors, due to the negligible heating effects of the esr, there is generally no need to consider the current carrying capability. Also, the rms current flowing into the output capacitor is extremely low.

Input Capacitor It is recommended that ceramic X5R or X7R capacitors be used, or at least that they be used in conjunction with some other capacitor technology; for example, aluminum electrolytic. Note that the self-resonance of electrolytics tend to occur in the 100s of kHz, therefore the effects of esl become apparent at switching frequencies in the region of 1 MHz.

The value of the input capacitance determines the amount of ripple voltage that appears at the source terminals. If a system is designed correctly, the input capacitor should supply the switching current minus the input average current during the on-time of the power switch. During the off-time of the power switch, the input capacitor is charged-up.

The rms current that flows in the input capacitor can be found from:

$$I_{rms} = \frac{I_{OUT} \times V_{OUT}}{V_{IN}} \times \left(\frac{V_{IN}}{V_{OUT}} - 1 \right)^{1/2} \quad , \tag{13}$$

The amount of ripple voltage that appears across the input terminals depends on: the amount of charge removed during the switch on-time and the actual capacitor value. If a capacitor technology such as an electrolytic is used, then the effects of esr also have to be considered.

The amount of capacitance required for a given ripple voltage can be found:

$$C_{IN} = \frac{I_{rms} \times T_{on}}{V_{RIPPLE}} \quad . \qquad (14)$$

As mentioned in the previous section, E-field biasing effects can reduce the actual capacitance and this should be taken into account when making the selection.

Again, there is generally no need to consider the heating effects of the rms current flowing through the esr of a ceramic capacitor. If an electrolytic device is used, then the ripple current rating should be considered. Note that most manufacturers only consider the rms current rating at 100 kHz.

Recirculation Diode This diode (D1) conducts during the switch off-time. A Schottky diode is recommended to minimize both the forward drop and switching losses. The worst-case dissipation occurs at maximum V_{IN}, when the duty cycle is at a minimum.

The average current through the diode can be found:

$$I_{DIODE(av)} = I_{LOAD} \times (1 - D\,(min)) \quad . \qquad (15)$$

The forward voltage drop, V_f, can be found from the diode characteristics by using the actual load current (not the average current).

The static power dissipation can be found:

$$P_{STAT} = I_{DIODE(av)} \times V_f \quad . \qquad (16)$$

It is also important to take into account the thermal rating of the package, $R_{\theta JA}$, and the ambient temperature, to ensure that enough heatsinking is provided to maintain the diode junction temperature within the safe operating area for the device.

To minimize the heating effects from the A4403 on the diode and vice-versa, it is recommended that the diode be mounted on the reverse side of the printed circuit board.

Sense Resistor The sense resistor should be a surface mount package, with low inductance. On no account should a wire-wound or through hole package be used. To prevent potential mistriggering problems from occurring in noisy systems, it is recommended that an R-C filter be applied across the sense resistor, as shown in figure 3.

The sense resistor value is selected depending on the maximum output load current. The typical sense voltage that causes a current limit is 180 mV. So, for example, a 50 mΩ value would be appropriate for a maximum load of 3 A, as it allows for margin between maximum load and the current limit. A tolerance of up to ±5% is acceptable.

The power rating of the resistor has to be considered. The current flowing in the resistor is essentially the same as the current flowing through the recirculation diode, although the power dissipation is worked out using the rms current.

To a first approximation, the sense resistor dissipation can be worked out as:

$$P_{SENSE} = I_{LOAD}^2 \times (1 - D\,(min)) \times R_{SENSE} \quad . \qquad (17)$$

For a converter working with a load of 3 A, a very narrow duty cycle, and a sense resistor of 50 mΩ, the power dissipation would be 450 mW.

The optimal solution from a cost perspective is to use two 100 mΩ, 1206-style resistors connected in parallel. Each resistor is generally rated at 250 mW at 70°C ambient. Check the vendor datasheet to verify the maximum ambient at full power.

When laying out the PCB, it is essential that the sense resistor connections, carrying the power current (see figure 3), are as short and wide as possible to minimize the effects of leakage inductance noise. In addition, the Kelvin sense circuit connections should be as close to the sense resistor pads as possible.

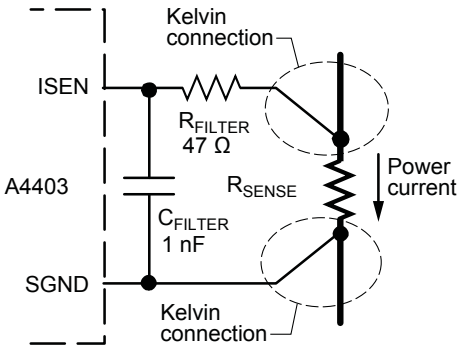


Figure 3. R-C filter added to the current sense circuit

R_{FILTER} and C_{FILTER} (R7 and C7 in the Typical Application diagram) should be placed close to the A4403 pins. The ground sense should connect directly to the SGND and not to the power ground.

Support Components The bootstrap capacitor (C2) and soft-start capacitor (C5) should be ceramic X5R or X7R.

Thermal Considerations To ensure the A4403 operates in the safe operating area, which effectively means restricting the junction temperature to less than 150°C, several checks should be made. The general approach is to work out what thermal impedance, $R_{\theta JA}$, is required to maintain the junction temperature at a given level, for a particular power dissipation. (Another factor worth considering is that other power dissipating components on the system PCB may influence the thermal performance of the A4403. For example, the power loss contribution from the recirculation diode and the sense resistor may cause the junction temperature of the A4403 to be higher than expected.) It should be noted that this process is usually an iterative one to achieve the optimum solution.

The following steps can be used as a guideline for determining the $R_{\theta JA}$ for a suitable thermal solution. :

1. Estimate the maximum ambient temperature, $T_A(max)$, of the application.

2. Define the maximum junction temperature, $T_J(max)$. Note that the absolute maximum is 150°C.

3. Determine the worst case power dissipation, $P_D(max)$. This will occur at maximum load and minimum V_{IN}. Contributors are:

(a) Switch static losses

Estimate the maximum duty cycle:

$$D\,(max) = \frac{V_{OUT} + V_f}{V_{IN}\,(min) + V_f} \quad , \qquad (18)$$

where V_f is the forward voltage drop of the Schottky diode (D1) and sense resistor (R2, R3) under the given load current.

Estimate the $R_{DS(on)}$ of the buck switch at the given junction temperature:

$$R_{DS(on)TJ} = R_{DS(on)25C}\left(1 + \frac{T_J - 25}{170}\right) \quad . \qquad (19)$$

The static loss for each switch can be determined:

$$P_{STAT} = I_{LOAD}{}^2 \times D\,(max) \times R_{DS(on)TJ} \quad , \qquad (20)$$

where I_{LOAD} is the load.

(b) Switch dynamic losses

Both the turn-on and the turn-off losses can be estimated:

$$P_{DYN} = V_{IN}(min) \times \frac{I_{LOAD}}{2} \times 5 \times 10^{-9} \times f_{SW} \times 1.6 \quad , \qquad (21)$$

where f_{SW} is the switching frequency.

(c) Diode capacitance turn-on loss

At turn-on, an additional current spike flows into the switch, causing a loss as follows:

$$P_{DIODECAP} = \frac{C_{DIODE} \times V_{IN}{}^2 \times f_{SW}}{2} \quad , \qquad (22)$$

where C_{DIODE} is the body capacitance of the Schottky diode (D1).

(d) Control losses

The control losses can be estimated as follows:

$$P_{CTRL} = I_{VINON} \times V_{IN} \quad , \qquad (23)$$

where I_{VINON} is the quiescent current with the converter enabled.

(e) Gate charge losses

Estimate the charge losses as follows:

$$P_{GATE} = Q \times f_{SW} \times V_{IN} \quad , \qquad (24)$$

where Q = 5 nC and is the charge that is required to turn on the buck switch.

(f) The total losses can now be estimated:

$$P_{TOTAL} = P_{STAT} + P_{DYN} + P_{DIODECAP} + P_{CTRL} + P_{GATE} \quad . \quad (25)$$

4. The thermal impedance required for the solution can now be determined:

$$R_{\theta JA} = \frac{T_J - T_A}{P_{TOTAL}} \quad . \quad (26)$$

Note that if a four-layer high thermal efficiency board is used, a thermal impedance of around 30°C/W can be achieved.

Example

Given selected parameters:

V_{IN}(min) = 42 V,

V_{OUT} = 3.3 V at 3 A,

f_{SW} = 1 MHz,

T_A = 70°C,

Target junction temperature, T_J = 115°C,

V_f = 0.55 V, and

C_{DIODE} = 150 pF, then:

(a) Switch static losses

Maximum duty cycle (equation 18):

$$D\ (max) = \frac{3.3 + 0.55}{42 + 0.55} = 0.09$$

$R_{DS(on)}$ of the buck switch (equation 19):

$$R_{DS(on)TJ} = 350 \times 10^{-3} \left(1 + \frac{115 - 25}{170}\right) = 0.535\ \Omega$$

Static loss for each switch (equation 20):

$$P_{STAT} = 3^2 \times 0.09 \times 0.535 = 0.433\ W$$

(b) Switch dynamic losses (equation 21):

$$P_{DYN} = 42 \times \frac{3}{2} \times 5 \times 10^{-9} \times 1000 \times 10^3 \times 1.6 = 0.504\ W$$

(c) Diode capacitance turn-on loss (equation 22):

$$P_{DIODECAP} = \frac{150 \times 10^{-12} \times 42^2 \times 1 \times 10^6}{2} = 0.132\ W$$

(d) Control losses (equation 23):

$$P_{CTRL} = 0.004 \times 42 = 0.168\ W$$

(e) Gate charge losses (equation 24):

$$P_{GATE} = 5 \times 10^{-9} \times 1 \times 10^6 \times 42 = 0.21\ W$$

(f) Total losses (equation 25):

$$P_{TOTAL} = 0.433 + 0.504 + 0.132 + 0.168 + 0.21 = 1.447\ W$$

Thermal impedance (equation 26):

$$R_{\theta JA} = \frac{115 - 70}{1.447} = 31°C/W$$

For this particular solution, a PCB with high thermal efficency is required to ensure the junction temperature is kept below 115°C. For maximum effectiveness, the PCB area underneath the thermal pad of the A4403 should be flooded with copper. Several thermal vias (say between 4 and 8) should be used to connect the thermal pad to the internal ground plane. If possible, a further thermal copper plane should be applied to the bottom side of the PCB and connected to the thermal pad of the A4403 through the vias.

This calculation assumes no thermal influence from other components. If possible, it is advisable to mount the recirculation diode (D1) on the reverse side of the printed circuit board. Ensure low impedance electrical connections are implemented between board layers.

PCB Layout Guidelines The ground plane is largely dictated by the thermal requirements of the previous section. The ground-referenced power components should be referenced to a star ground, located away from the A4403 to minimize ground bounce issues.

A small, local, relatively quiet ground plane near the A4403 should be used for the ground-referenced support components, to minimize interference effects of ground noise from the power circuitry. Figure 4 illustrates the recommended grounding architecture.

To avoid ground offset issues in the output voltage, it is highly recommended that the ground-referenced feedback resistor R6 should be connected directly to the GND connection of the A4403. In other words, the R6 ground return should avoid the use of the internal ground plane.

All ground-referenced support components (C5 and the DIS switch) should also be located as close to the GND connection as possible. A "local quiet" ground plane around these components can be implemented; however, this ground plane should have a high impedance connection to the star ground connection of the power stages, as referenced below.

The sense resistor connections should be connected in a Kelvin circuit (see figure 3) to the corresponding pins on the A4403 (ISEN and SGND). Note that it is imperative that the PCB traces between the sense resistor pads and the sense connections are as short as possible to minimize the effects of leakage inductance.

In noisy systems, it is highly recommended that an R-C filter be used to filter the signal produced across the ISEN pin. See the Sense Resistor section and the Typical Application schematic.

If an internal ground plane is used, it is recommended that it does not overlap the switching node, LX, to avoid the possibility of noise pick up. To minimize the possibility of noise injection issues, it is recommended to isolate the ground plane around the high impedance nodes, such as FB and SS.

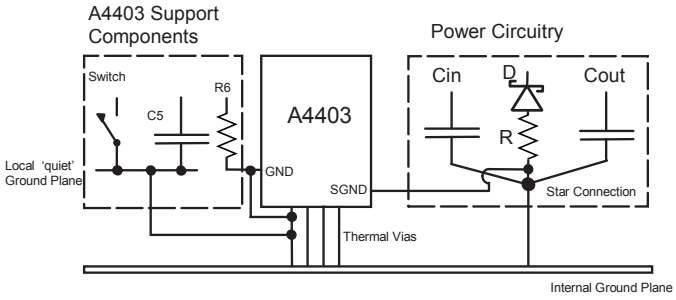


Figure 4. Ground plane configurations

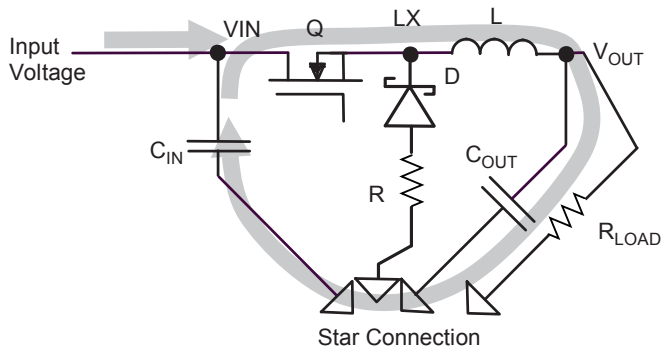


Figure 5. FET on-cycle current conduction paths

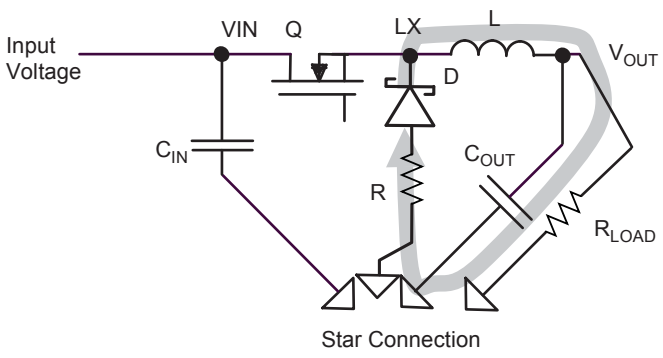


Figure 6. FET off-cycle current conduction paths

In terms of grounding the power components, a star connection should be made to minimize the ground loop impedances. Note that, although a ground plane may be required to meet the thermal characteristics of the solution, it is still imperative to implement a star ground connection for the power components.

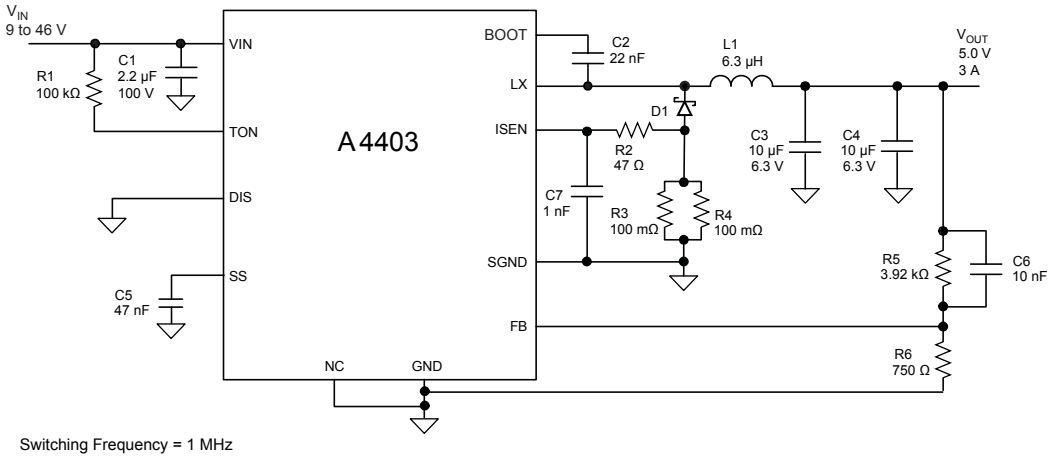
Figures 5 and 6 illustrate the importance of keeping the ground connections as short as possible and forming good star connections.

Figure 5 also illustrates the current conduction paths during the on-cycle of the switching FET. The following points should be noted:

- The capacitor C_{IN} should be placed as close as possible to the VIN terminal.
- The inductor L should placed as close as possible to the LX terminal and to the output capacitors C_{OUT}.
- Good separation should exist between the LX connection and any adjacent components or traces.

Figure 6 shows the current conduction path during the off-cycle of the switching FET. The following points should be noted:

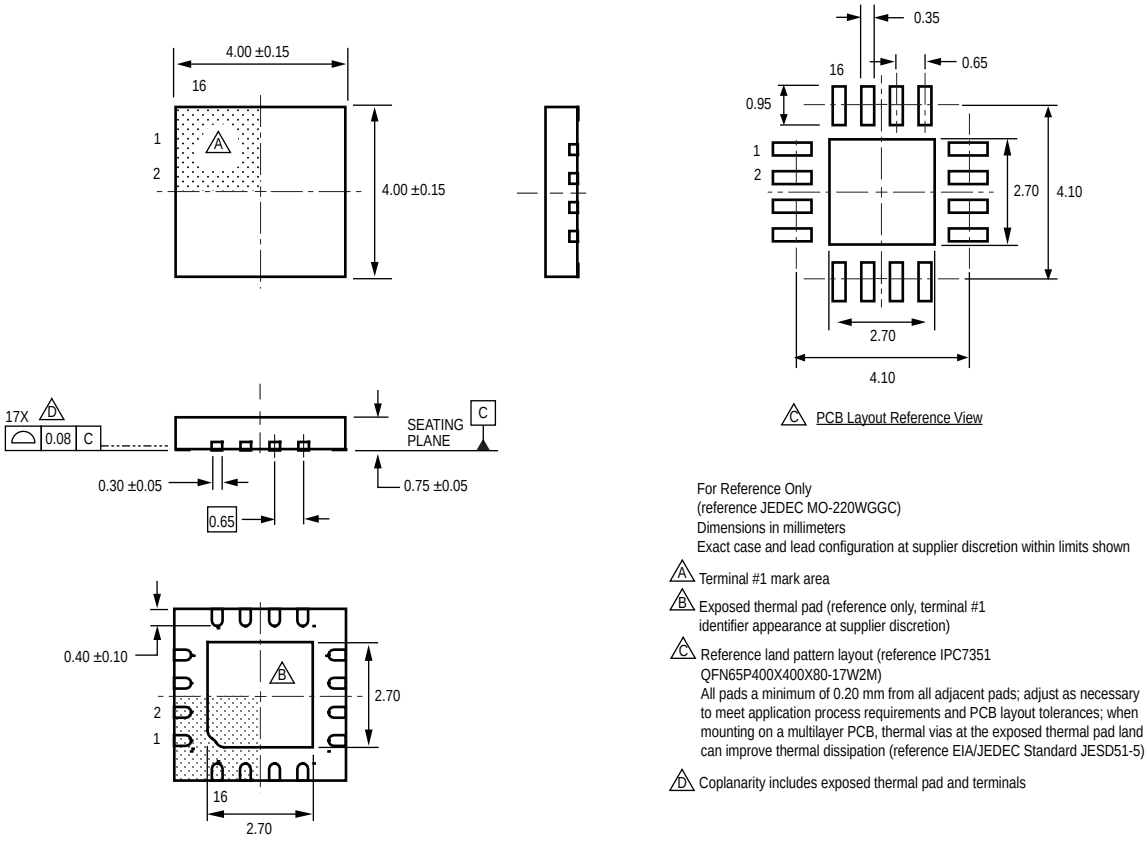
- The diode D should be placed as close as possible to both the switching FET and to the inductor. The resistor R should be placed as close as possible to the diode D.
- The boostrap capacitor, C2, and the soft start capacitor, C5, should be located as close as possible to their respective terminal connections. The ground reference of the soft start capacitor should be connected as close to the GND terminal as possible.



Switching Frequency = 1 MHz
All capacitors are X5R or X7R ceramic
Resistors R3 and R4 should be surface mount, low inductance type, rated at 250 mW at 70°C

Figure 7. Typical application

Package EU, 16-Contact QFN



For Reference Only
(reference JEDEC MO-220WGGC)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN65P400X400X80-17W2M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals