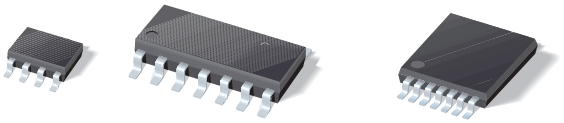


SLOS385A − SEPTEMBER 2001 − REVISED JANUARY 2009

# LOW-NOISE, HIGH-SPEED CURRENT FEEDBACK AMPLIFIERS

## FEATURES

- **Low Noise:**
  - **2.9 pA/√Hz Noninverting Current Noise**
  - **10.8 pA/√Hz Inverting Current Noise**
  - **2.2 nV/√Hz Voltage Noise**
- **Wide Supply Voltage Range: ±5 V to ±15 V**
- **Wide Output Swing:**
  - **25 $V_{PP}$ Output Voltage, $R_L$ = 100 Ω, ±15-V Supply**
- **High Output Current: 150 mA (Min)**
- **High Speed:**
  - **110 MHz (−3 dB, G=1, ±15 V)**
  - **1550 V/μs Slew Rate (G = 2, ±15 V)**
- **Low Distortion, G = 2:**
  - **−78 dBc (1 MHz, 2 $V_{PP}$, 100-Ω load)**
- **Low Power Shutdown (THS3115):**
  - **300-μA Shutdown Quiescent Current Per Channel**
- **Thermal Shutdown and Short Circuit Protection**
- **Standard SOIC, SOIC PowerPAD™, and TSSOP PowerPAD Package**
- **Evaluation Module Available**

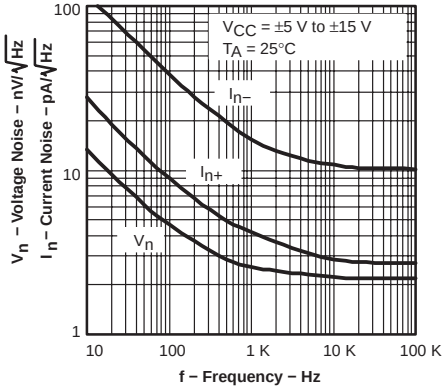
## APPLICATIONS

- **Communication Equipment**
- **Video Distribution**
- **Motor Drivers**
- **Piezo Drivers**

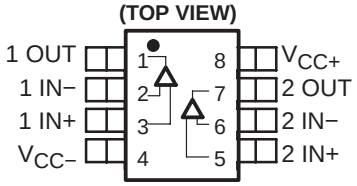
## DESCRIPTION

The THS3112/5 are low-noise, high-speed current feedback amplifiers, ideal for any application requiring high output current. The low noninverting current noise of 2.9 pA/√Hz and the low inverting current noise of 10.8 pA/√Hz increase signal to noise ratios for enhanced signal resolution. The THS3112/5 can operate from ±5-V to ±15-V supply voltages, while drawing as little as 4.5 mA of supply current per channel. It offers low –78-dBc total harmonic distortion driving 2 $V_{PP}$ into a 100-Ω load. The THS3115 features a low power shutdown mode, consuming only 300-μA shutdown quiescent current per channel. The THS3112/5 is packaged in a standard SOIC, SOIC PowerPAD, and TSSOP PowerPAD packages.

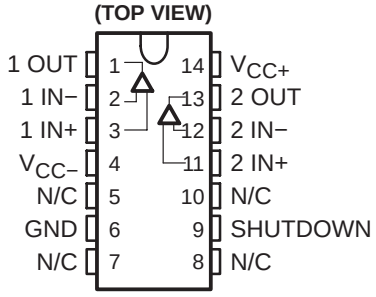
**VOLTAGE NOISE AND CURRENT NOISE vs FREQUENCY**




**THS3112 SOIC (D) AND SOIC PowerPAD™ (DDA) PACKAGE (TOP VIEW)**




**THS3115 SOIC (D) AND TSSOP PowerPAD™ (PWP) PACKAGE (TOP VIEW)**



**AVAILABLE OPTIONS(1)**

| $T_A$ | PACKAGED DEVICE | | | | EVALUATION MODULES |
|---|---|---|---|---|---|
| | SOIC-8 (D) | SOIC-8 PowerPAD (DDA) | SOIC-14 (D) | TSSOP-14 (PWP) | |
| 0°C to 70°C | THS3112CD | THS3112CDDA | THS3115CD | THS3115CPWP | THS3112EVM THS3115EVM |
| −40°C to 85°C | THS3112ID | THS3112IDDA | THS3115ID | THS3115IPWP | |

NOTE 1: For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, $V_{CC+}$ to $V_{CC-}$ . . . . . 33 V
Input voltage . . . . . $\pm V_{CC}$
Output current (see Note 2) . . . . . 275 mA
Differential input voltage . . . . . ± 4 V
Maximum junction temperature . . . . . 150°C
Total power dissipation at (or below) 25°C free-air temperature . . . . . See Dissipation Ratings Table
Operating free-air temperature, $T_A$: Commercial . . . . . 0°C to 70°C
Industrial . . . . . −40°C to 85°C
Storage temperature, $T_{stg}$ : Commercial . . . . . −65°C to 125°C
Industrial . . . . . −65°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C

† Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: The THS3112 and THS3115 may incorporate a PowerPAD™ on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI Technical Brief SLMA002 for more information about utilizing the PowerPAD™ thermally enhanced package.

**DISSIPATION RATING TABLE**

| PACKAGE | $\theta_{JA}$ | $T_A$ = 25°C POWER RATING |
|---|---|---|
| D-8 | 95°C/W‡ | 1.32 W |
| DDA | 67°C/W | 1.87 W |
| D-14 | 66.6°C/W‡ | 1.88 W |
| PWP | 37.5°C/W | 3.3 W |

‡ This data was taken using the JEDEC proposed high-K test PCB. For the JEDEC low-K test PCB, the $\theta_{JA}$ is168°C/W for the D-8 package and 122.3°C/W for the D-14 package.

## recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC+}$ to $V_{CC-}$ | Dual supply | ±5 | | ±15 | V |
| | Single supply | 10 | | 30 | |
| Operating free-air temperature, $T_A$ | C-suffix | 0 | | 70 | °C |
| | I-suffix | −40 | | 85 | |
| Shutdown pin input levels, relative to the GND pin | High level (device shutdown) | 2 | | | V |
| | Low level (device active) | | | 0.8 | |

## electrical characteristics over recommended operating free-air temperature range, $T_A$ = 25°C, $V_{CC}$ = ±15 V, $R_F$ = 750 Ω, $R_L$ = 100 Ω (unless otherwise noted)

### dynamic performance

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| BW | Small-signal bandwidth (−3 dB) | $R_L$ = 100 Ω | $R_F$ = 1 kΩ, G = 1 | $V_{CC}$ = ±5 V | | 95 | | MHz |
| | | | | $V_{CC}$ = ±15 V | | 110 | | |
| | | $R_L$ = 100 Ω | $R_F$ = 750 Ω, G = 2 | $V_{CC}$ = ±5 V | | 103 | | |
| | | | | $V_{CC}$ = ±15 V | | 110 | | |
| | Bandwidth (0.1 dB) | | $R_F$ = 750 Ω, G = 2 | $V_{CC}$ = ±5 V | | 25 | | |
| | | | | $V_{CC}$ = ±15 V | | 48 | | |
| SR | Slew rate (see Note 3), G=8 | G = 2 $R_F$ = 680 Ω | $V_O$ = 10 $V_{PP}$ | $V_{CC}$ = ±15 V | | 1550 | | V/µs |
| | | | $V_O$ = 5 $V_{PP}$ | $V_{CC}$ = ±5 V | | 820 | | |
| | | | | $V_{CC}$ = ±15 V | | 1300 | | |
| $t_S$ | Settling time to 0.1% | G = −1 | $V_O$ = 2 $V_{PP}$ | $V_{CC}$ = ±5 V | | 50 | | ns |
| | | | $V_O$ = 5 $V_{PP}$ | $V_{CC}$ = ±15 V | | 63 | | |

NOTE 3: Slew rate is defined from the 25% to the 75% output levels.

### noise/distortion performance

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| THD | Total harmonic distortion | | G = 2, $R_F$ = 680 Ω, $V_{CC}$ = ±15 V, f = 1 MHz | $V_{O(PP)}$ = 2 V | | −78 | | dBc |
| | | | | $V_{O(PP)}$ = 8 V | | −75 | | |
| | | | G = 2, $R_F$ = 680 Ω, $V_{CC}$ = ±5 V, f = 1 MHz | $V_{O(PP)}$ = 2 V | | −76 | | |
| | | | | $V_{O(PP)}$ = 6 V | | −74 | | |
| $V_n$ | Input voltage noise | | $V_{CC}$ = ±5 V, ±15 V | f = 10 kHz | | 2.2 | | nV/√Hz |
| $I_n$ | Input current noise | Noninverting Input | $V_{CC}$ = ±5 V, ±15 V | f = 10 kHz | | 2.9 | | pA/√Hz |
| | | Inverting Input | | | | 10.8 | | |
| | Crosstalk | | G = 2, f = 1 MHz, $V_O$ = 2 Vpp | $V_{CC}$ = ±5 V | | −67 | | dBc |
| | | | | $V_{CC}$ = ±15 V | | −67 | | |
| | Differential gain error | | G = 2, $R_L$ = 150 Ω 40 IRE modulation ±100 IRE Ramp NTSC and PAL | $V_{CC}$ = ±5 V | | 0.01% | | |
| | | | | $V_{CC}$ = ±15 V | | 0.01% | | |
| | Differential phase error | | | $V_{CC}$ = ±5 V | | 0.011° | | |
| | | | | $V_{CC}$ = ±15 V | | 0.011° | | |

## electrical characteristics over recommended operating free-air temperature range, $T_A$ = 25°C, $V_{CC}$ = ±15 V, $R_F$ = 750 Ω, $R_L$ = 100 Ω (unless otherwise noted) (continued)

### dc performance

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IO}$ | Input offset voltage | $V_{CC}$ = ±5 V, $V_{CC}$ = ±15 V | $T_A$ = 25°C | | 6 | 10 | mV |
| | | | $T_A$ = full range | | | 13 | |
| | Channel offset voltage matching | | $T_A$ = 25°C | | 1 | 3 | |
| | | | $T_A$ = full range | | | 4 | |
| | Offset drift | | $T_A$ = full range | | 10 | | µV/°C |
| $I_{IB}$ | − Input bias current | $V_{CC}$ = ±5 V, $V_{CC}$ = ±15 V | $T_A$ = 25°C | | | 23 | µA |
| | | | $T_A$ = full range | | | 30 | |
| | + Input bias current | | $T_A$ = 25°C | | 0.33 | 2 | |
| | | | $T_A$ = full range | | | 3 | |
| | Input offset current | | $T_A$ = 25°C | | 4 | 22 | |
| | | | $T_A$ = full range | | | 30 | |
| $Z_{OL}$ | Open loop transimpedance | $V_{CC}$ = ±5 V, $V_{CC}$ = ±15 V | $R_L$ = 1 kΩ, | | 1 | | MΩ |

### input characteristics

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{ICR}$ | Input common-mode voltage range | $V_{CC}$ = ±5 V | $T_A$ = full range | ±2.5 | ±2.7 | | V |
| | | $V_{CC}$ = ±15 V | | ±12.5 | ±12.7 | | |
| CMRR | Common-mode rejection ratio | $V_{CC}$ = ±5 V, $V_I$ = −2.5 V to 2.5 V | $T_A$ = 25°C | 56 | 62 | | dB |
| | | | $T_A$ = full range | 54 | | | |
| | | $V_{CC}$ = ±15 V, $V_I$ = −12.5 V to 12.5 V | $T_A$ = 25°C | 63 | 67 | | |
| | | | $T_A$ = full range | 60 | | | |
| $R_I$ | Input resistance | + Input | | | 1.5 | | MΩ |
| | | − Input | | | 15 | | Ω |
| $C_i$ | Input capacitance | | | | 2 | | pF |

### output characteristics

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_O$ | Output voltage swing | G = 4, $V_I$ = 1 V, $V_{CC}$ = ±5 V | $R_L$ = 1 kΩ, | $T_A$ = 25°C | | 3.9 | | V |
| | | | $R_L$ = 100 Ω, | $T_A$ = 25°C | 3.6 | 3.8 | | |
| | | | | $T_A$ = full range | 3.4 | | | |
| | | G = 4, $V_I$ = 3.4 V, $V_{CC}$ = ±15 V | $R_L$ = 1 kΩ, | $T_A$ = 25°C | | 13.5 | | |
| | | | $R_L$ = 100 Ω, | $T_A$ = 25°C | 12.2 | 13.3 | | |
| | | | | $T_A$ = full range | 12 | | | |
| $I_O$ | Output current drive | G = 4, $V_I$ = 0.9 V, $V_{CC}$ = ±5 V | $R_L$ = 25 Ω, | $T_A$ = 25°C | 100 | 130 | | mA |
| | | G = 4, $V_I$ = 1.7 V, $V_{CC}$ = ±15 V | $R_L$ = 25 Ω, | | 175 | 270 | | |
| $r_o$ | Output resistance | open loop | | | | 14 | | Ω |

## electrical characteristics over recommended operating free-air temperature range, $T_A$ = 25°C, $V_{CC}$ = ±15 V, $R_F$ = 750 Ω, $R_L$ = 100 Ω, GND = 0 V (unless otherwise noted) (continued)

### power supply

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Quiescent current (per amplifier) | $V_{CC}$ = ±5 V | $T_A$ = 25°C | | 4.4 | 5.5 | mA |
| | | | $T_A$ = full range | | | 6 | |
| | | $V_{CC}$ = ±15 V | $T_A$ = 25°C | | 4.9 | 6.5 | |
| | | | $T_A$ = full range | | | 7.5 | |
| PSRR | Power supply rejection ratio | $V_{CC}$ = ±5 V | $T_A$ = 25°C | 53 | 60 | | dB |
| | | | $T_A$ = full range | 50 | | | |
| | | $V_{CC}$ = ±15 V | $T_A$ = 25°C | 60 | 69 | | |
| | | | $T_A$ = full range | 55 | | | |

### shutdown characteristics (THS3115 only)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{CC(SHDN)}$ | Shutdown quiescent current (per channel) | $V_{GND}$ = 0 V, $V_{CC}$ = ±5 V, ±15 V | | 0.3 | 0.45 | mA |
| $t_{DIS}$ | Disable time (see Note 4) | $V_{CC}$ = ±15 V | | 200 | | ns |
| $t_{EN}$ | Enable time (see Note 4) | $V_{CC}$ = ±15 V | | 300 | | ns |
| $I_{IL(SHDN)}$ | Shutdown pin input bias current for power up | $V_{CC}$ = ±5 V, ±15 V, $V_{(SHDN)}$ = 0 V | | 18 | 25 | µA |
| $I_{IH(SHDN)}$ | Shutdown pin input bias current for power down | $V_{CC}$ = ±5 V, ±15 V, $V_{(SHDN)}$ = 3.3 V | | 110 | 130 | µA |

NOTE 4: Disable/enable time is defined as the time from when the shutdown signal is applied to the SHDN pin to when the supply current has reached half of its final value.

## TYPICAL CHARACTERISTICS

### Table of Graphs

| | | | FIGURE |
|---|---|---|---|
| | Small signal closed loop gain | vs Frequency | 1 − 11, 13, 14 |
| | Gain and phase | vs Frequency | 12 |
| | Small signal closed loop noninverting gain | vs Frequency | 15, 16 |
| | Small signal closed loop inverting gain | vs Frequency | 17, 18 |
| | Small and large signal output | vs Frequency | 19, 20 |
| | Harmonic distortion | vs Frequency | 21, 22 |
| | | vs Peak−to−peak output voltage | 23, 24 |
| $V_n$, $I_n$ | Voltage noise and current noise | vs Frequency | 25 |
| CMRR | Common-mode rejection ratio | vs Frequency | 26 |
| PSRR | Power supply rejection ratio | vs Frequency | 27 |
| | Crosstalk | vs Frequency | 28 |
| $Z_o$ | Output impedance | vs Frequency | 29 |
| SR | Slew rate | vs Output voltage step | 30 |
| $V_{IO}$ | Input offset voltage | vs Free-air temperature | 31 |
| | | vs Common-mode input voltage | 32 |
| $I_B$ | Input bias current | vs Free-air temperature | 33 |
| $V_O$ | Output voltage | vs Output current | 34, 35 |
| | Output voltage headroom | vs Output current | 36 |
| $I_{CC}$ | Supply current (per channel) | vs Supply voltage | 37 |
| | Shutdown response | | 38 |

## TYPICAL CHARACTERISTICS

**SMALL SIGNAL CLOSED LOOP GAIN vs FREQUENCY**

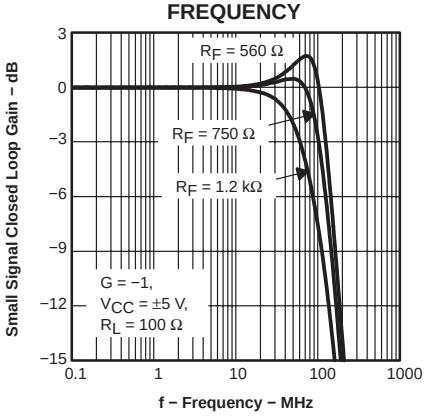



**Figure 1**

**SMALL SIGNAL CLOSED LOOP GAIN vs FREQUENCY**

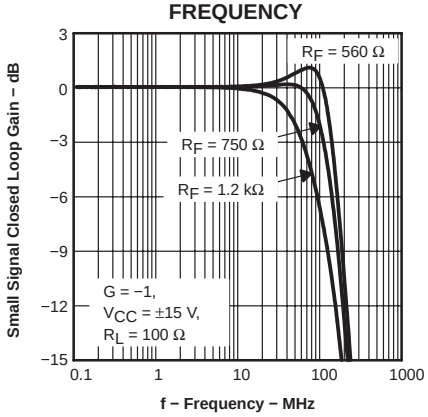



**Figure 2**

**SMALL SIGNAL CLOSED LOOP GAIN vs FREQUENCY**

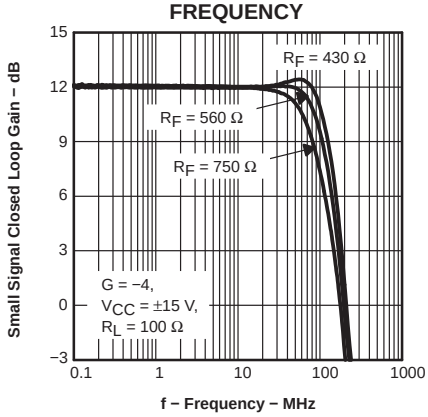



**Figure 3**

**SMALL SIGNAL CLOSED LOOP GAIN vs FREQUENCY**

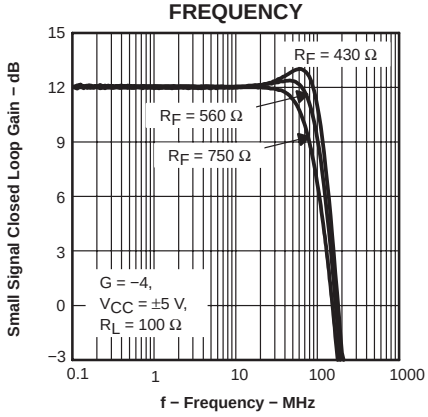



**Figure 4**

**SMALL SIGNAL CLOSED LOOP GAIN vs FREQUENCY**

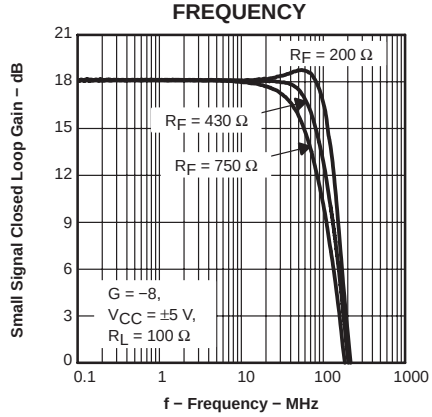



**Figure 5**

**SMALL SIGNAL CLOSED LOOP GAIN vs FREQUENCY**

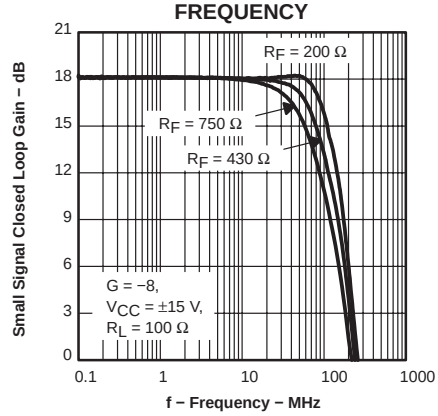



**Figure 6**

**SMALL SIGNAL CLOSED LOOP GAIN vs FREQUENCY**

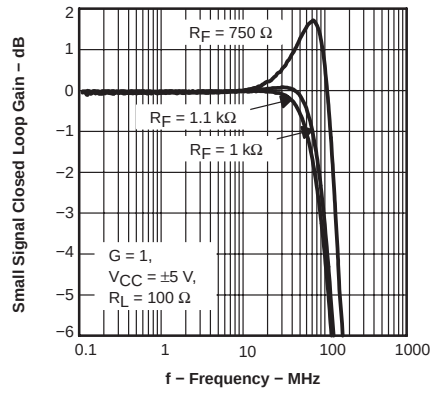



**Figure 7**

**SMALL SIGNAL CLOSED LOOP GAIN vs FREQUENCY**

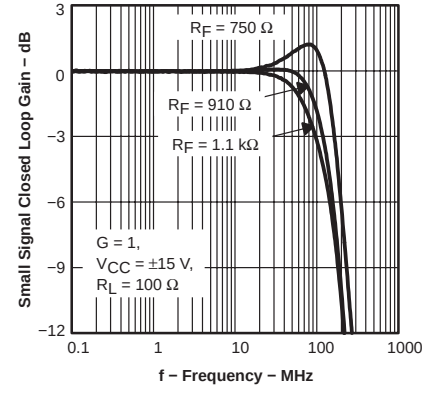



**Figure 8**

**SMALL SIGNAL CLOSED LOOP GAIN vs FREQUENCY**

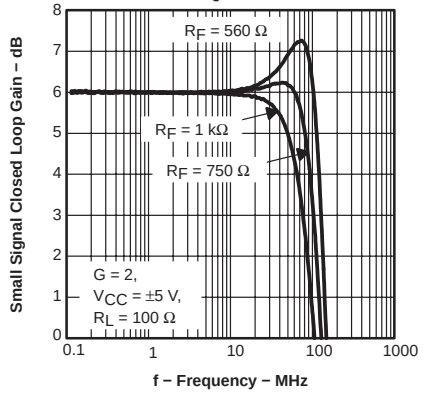



**Figure 9**

## TYPICAL CHARACTERISTICS

**SMALL SIGNAL CLOSED LOOP GAIN vs FREQUENCY**

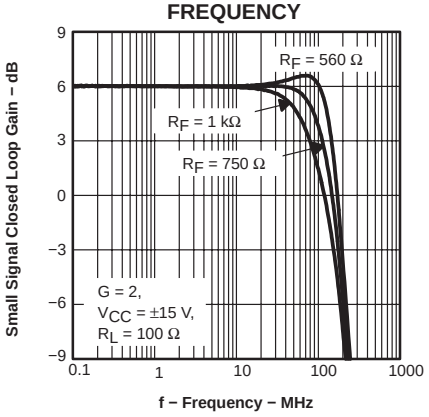



Figure 10

**SMALL SIGNAL CLOSED LOOP GAIN vs FREQUENCY**

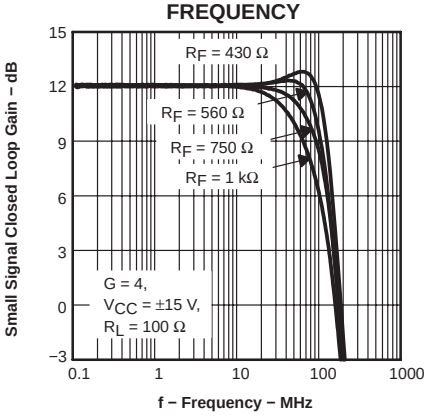



Figure 11

**GAIN AND PHASE vs FREQUENCY**

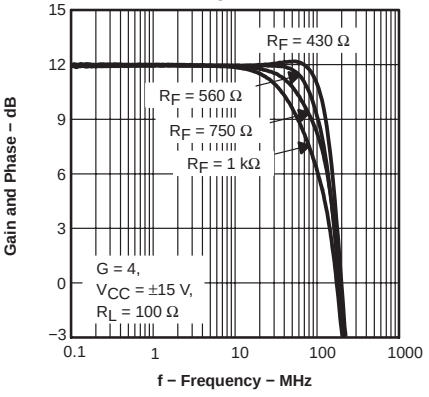



Figure 12

**SMALL SIGNAL CLOSED LOOP GAIN vs FREQUENCY**

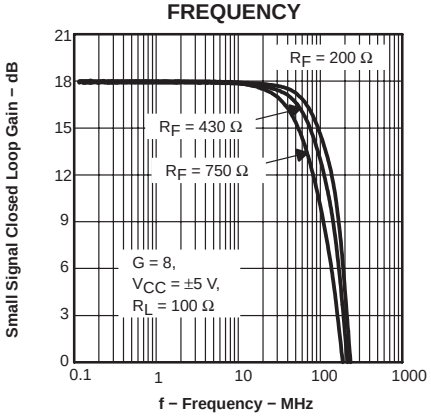



Figure 13

**SMALL SIGNAL CLOSED LOOP GAIN vs FREQUENCY**

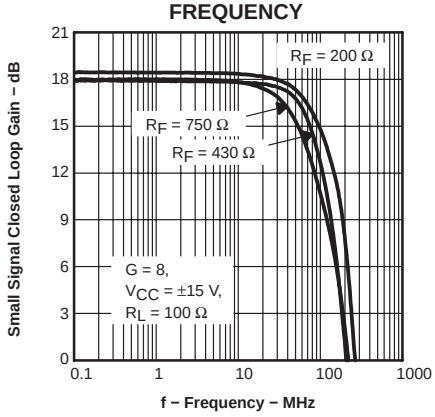



Figure 14

**SMALL SIGNAL CLOSED LOOP NONINVERTING GAIN vs FREQUENCY**

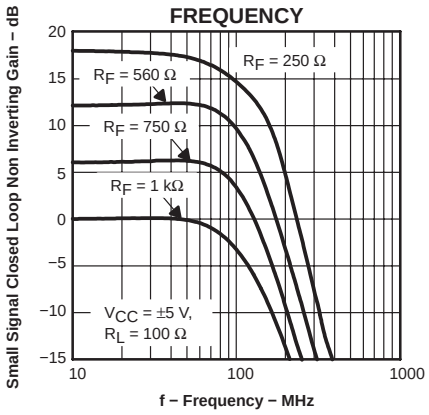



Figure 15

**SMALL SIGNAL CLOSED LOOP NONINVERTING GAIN vs FREQUENCY**

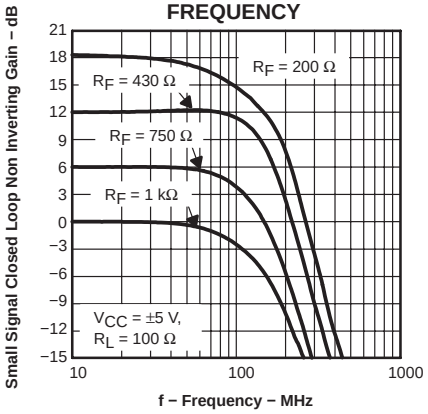



Figure 16

**SMALL SIGNAL CLOSED LOOP INVERTING GAIN vs FREQUENCY**

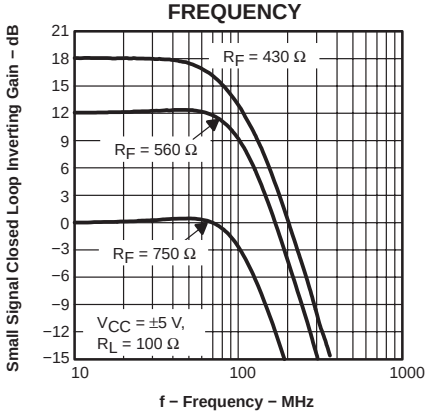



Figure 17

**SMALL SIGNAL CLOSED LOOP INVERTING GAIN vs FREQUENCY**

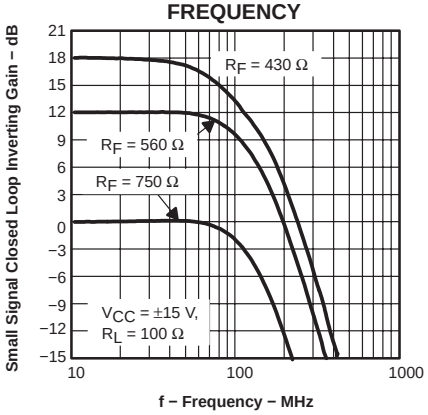



Figure 18

## TYPICAL CHARACTERISTICS

**SMALL AND LARGE SIGNAL OUTPUT vs FREQUENCY**

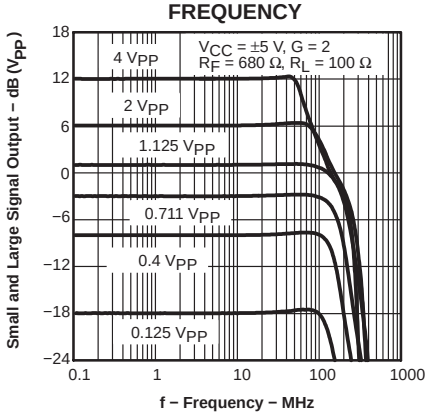



Figure 19

**SMALL AND LARGE SIGNAL OUTPUT vs FREQUENCY**

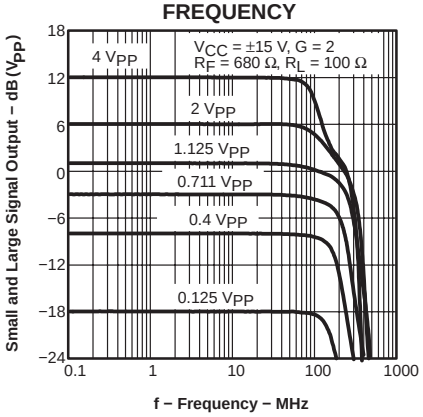



Figure 20

**HARMONIC DISTORTION vs FREQUENCY**

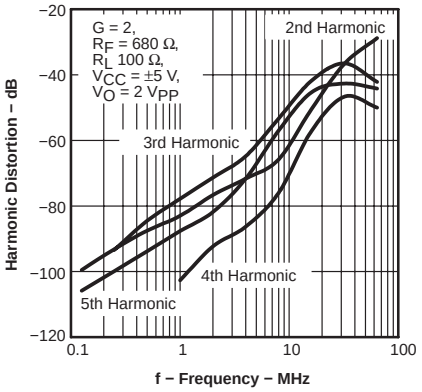



Figure 21

**HARMONIC DISTORTION vs FREQUENCY**

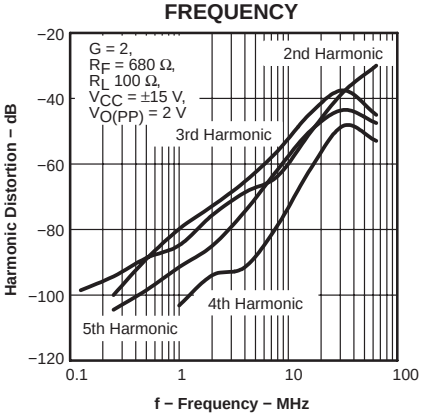



Figure 22

**HARMONIC DISTORTION vs PEAK-TO-PEAK OUTPUT VOLTAGE**

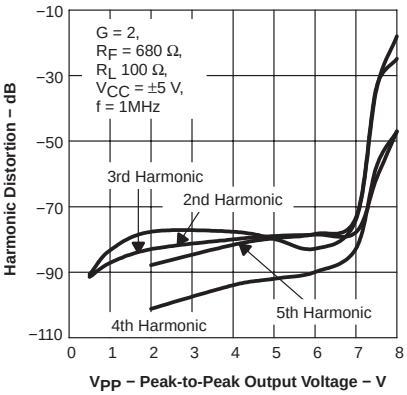



Figure 23

**HARMONIC DISTORTION vs PEAK-TO-PEAK OUTPUT VOLTAGE**

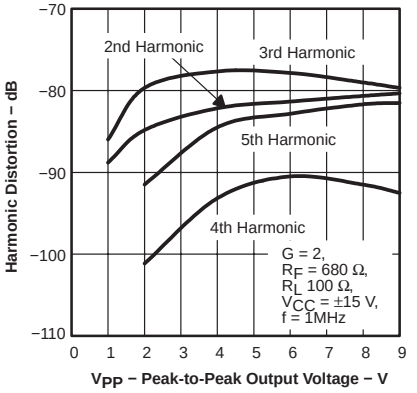



Figure 24

**VOLTAGE NOISE AND CURRENT NOISE vs FREQUENCY**

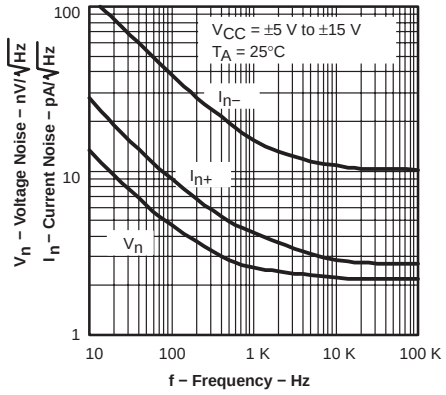



Figure 25

**COMMON-MODE REJECTION RATIO vs FREQUENCY**

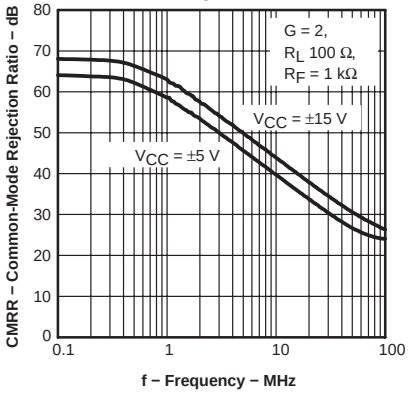



Figure 26

**POWER SUPPLY REJECTION RATIO vs FREQUENCY**

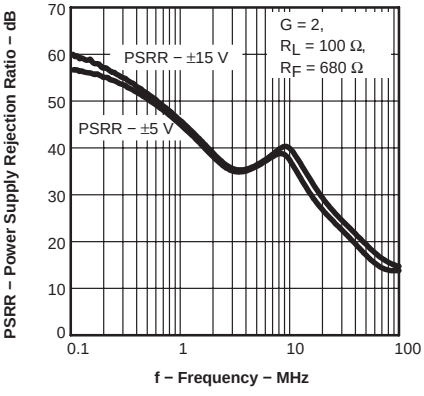



Figure 27

## TYPICAL CHARACTERISTICS

**CROSSTALK vs FREQUENCY**

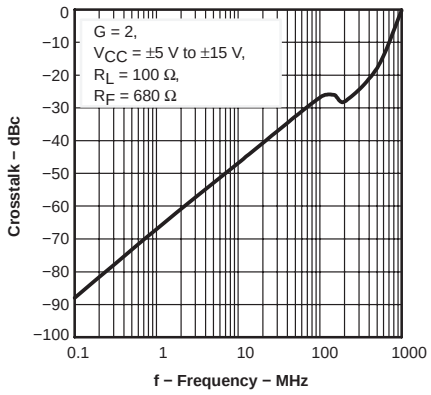



Figure 28

**OUTPUT IMPEDANCE vs FREQUENCY**

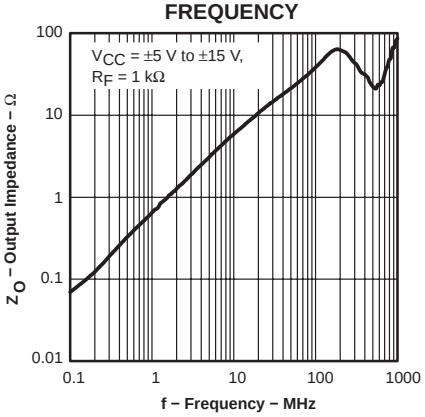



Figure 29

**SLEW RATE vs OUTPUT VOLTAGE STEP**

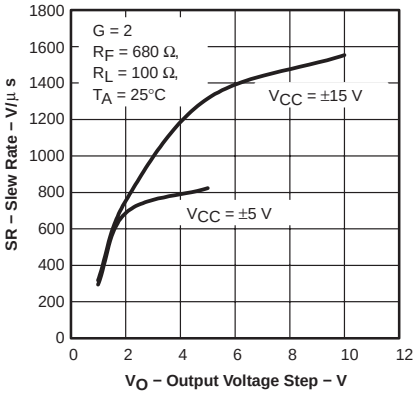



Figure 30

**INPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE**

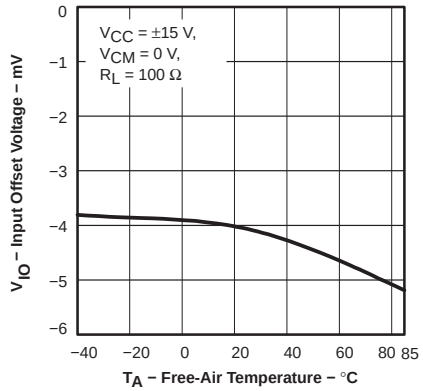



Figure 31

**INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE**

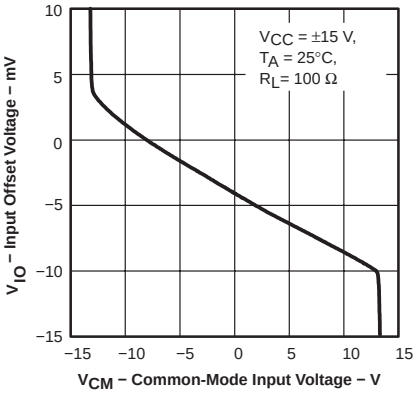



Figure 32

**INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE**

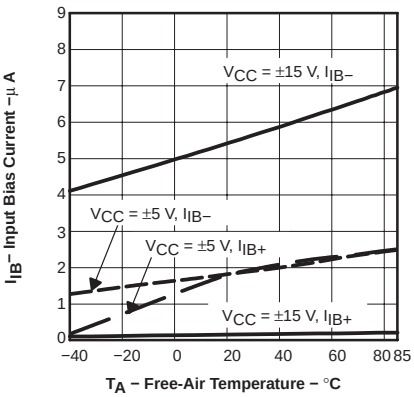



Figure 33

**OUTPUT VOLTAGE vs OUTPUT CURRENT**

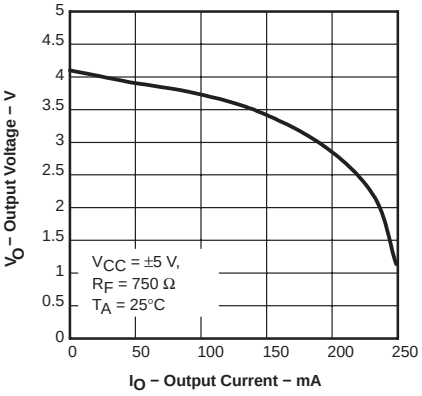



Figure 34

**OUTPUT VOLTAGE vs OUTPUT CURRENT**

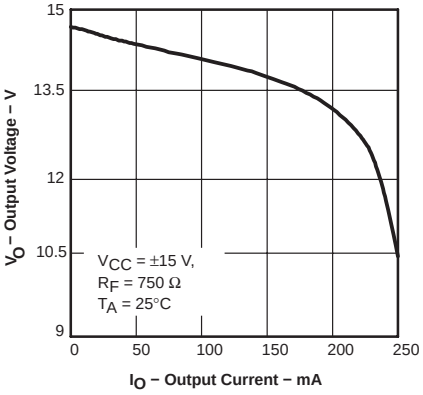



Figure 35

**OUTPUT VOLTAGE HEADROOM vs OUTPUT CURRENT**

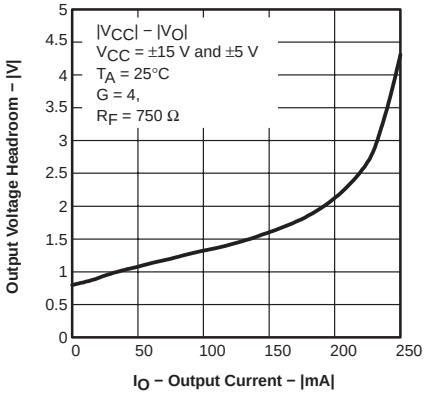



Figure 36

## TYPICAL CHARACTERISTICS

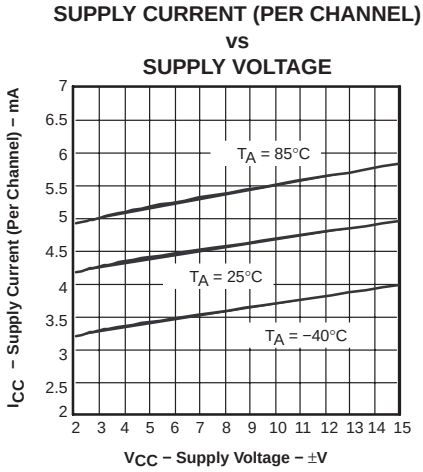



**Figure 37**

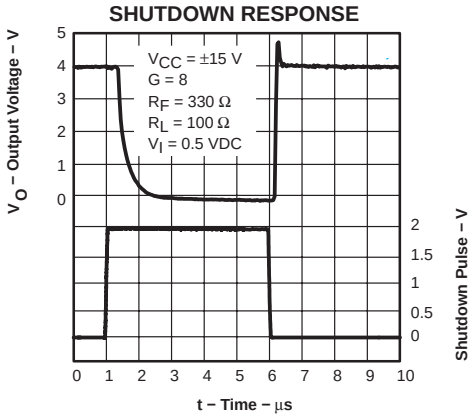



**Figure 38**

## Revision History

| DATE | REV | PAGE | SECTION | DESCRIPTION |
|---|---|---|---|---|
| 1/09 | A | 4 | Electrical Characteristics | Changed input offset voltage values for $T_A$ = 25°C. |
| | | 5 | Electrical Characteristics | Changed PSRR values for VCC = ±15 V. |

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| THS3112CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS3112CDDA | ACTIVE | SO Power PAD | DDA | 8 | 75 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM |
| THS3112CDDAG3 | ACTIVE | SO Power PAD | DDA | 8 | 75 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM |
| THS3112CDDAR | ACTIVE | SO Power PAD | DDA | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM |
| THS3112CDDARG3 | ACTIVE | SO Power PAD | DDA | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM |
| THS3112CDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS3112CDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS3112CDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS3112ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS3112IDDA | ACTIVE | SO Power PAD | DDA | 8 | 75 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM |
| THS3112IDDAG3 | ACTIVE | SO Power PAD | DDA | 8 | 75 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM |
| THS3112IDDAR | ACTIVE | SO Power PAD | DDA | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM |
| THS3112IDDARG3 | ACTIVE | SO Power PAD | DDA | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM |
| THS3112IDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS3115CD | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS3115CDG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS3115CPWP | ACTIVE | HTSSOP | PWP | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| THS3115CPWPG4 | ACTIVE | HTSSOP | PWP | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| THS3115CPWPR | ACTIVE | HTSSOP | PWP | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| THS3115CPWPRG4 | ACTIVE | HTSSOP | PWP | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| THS3115ID | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| THS3115IDG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & | CU NIPDAU | Level-1-260C-UNLIM |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| | | | | | | no Sb/Br) | | |
| THS3115IPWP | ACTIVE | HTSSOP | PWP | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| THS3115IPWPG4 | ACTIVE | HTSSOP | PWP | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| THS3115IPWPR | ACTIVE | HTSSOP | PWP | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| THS3115IPWPRG4 | ACTIVE | HTSSOP | PWP | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

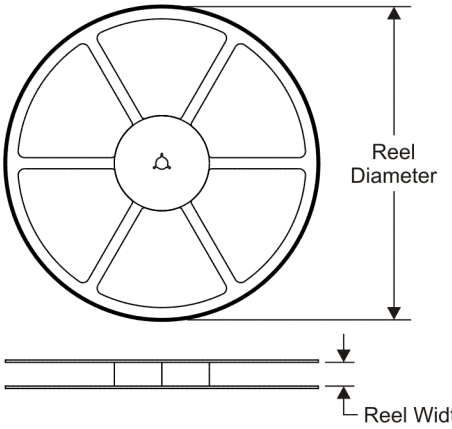
(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

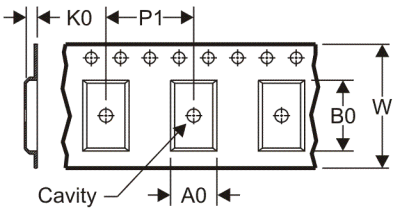
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

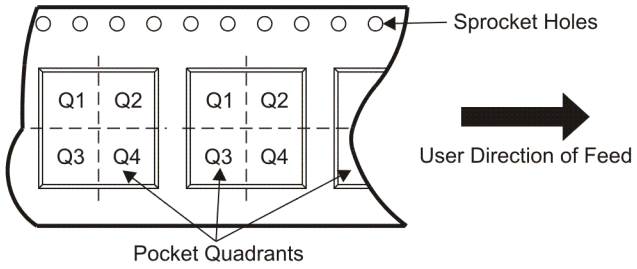



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

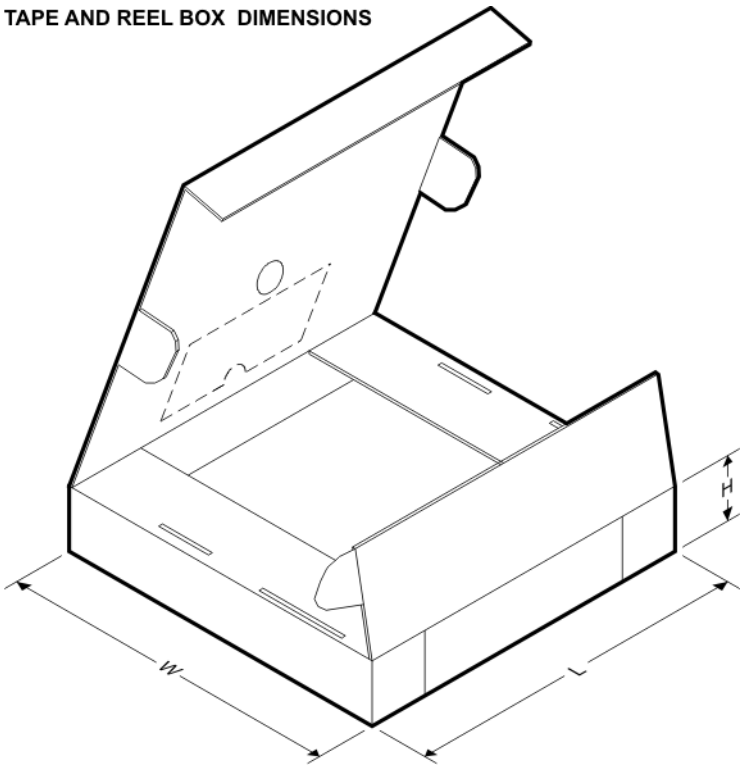
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| THS3112CDDAR | SO Power PAD | DDA | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| THS3112CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| THS3112IDDAR | SO Power PAD | DDA | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| THS3115CPWPR | HTSSOP | PWP | 14 | 2000 | 330.0 | 12.4 | 6.67 | 5.4 | 1.6 | 8.0 | 12.0 | Q1 |
| THS3115IPWPR | HTSSOP | PWP | 14 | 2000 | 330.0 | 12.4 | 6.67 | 5.4 | 1.6 | 8.0 | 12.0 | Q1 |

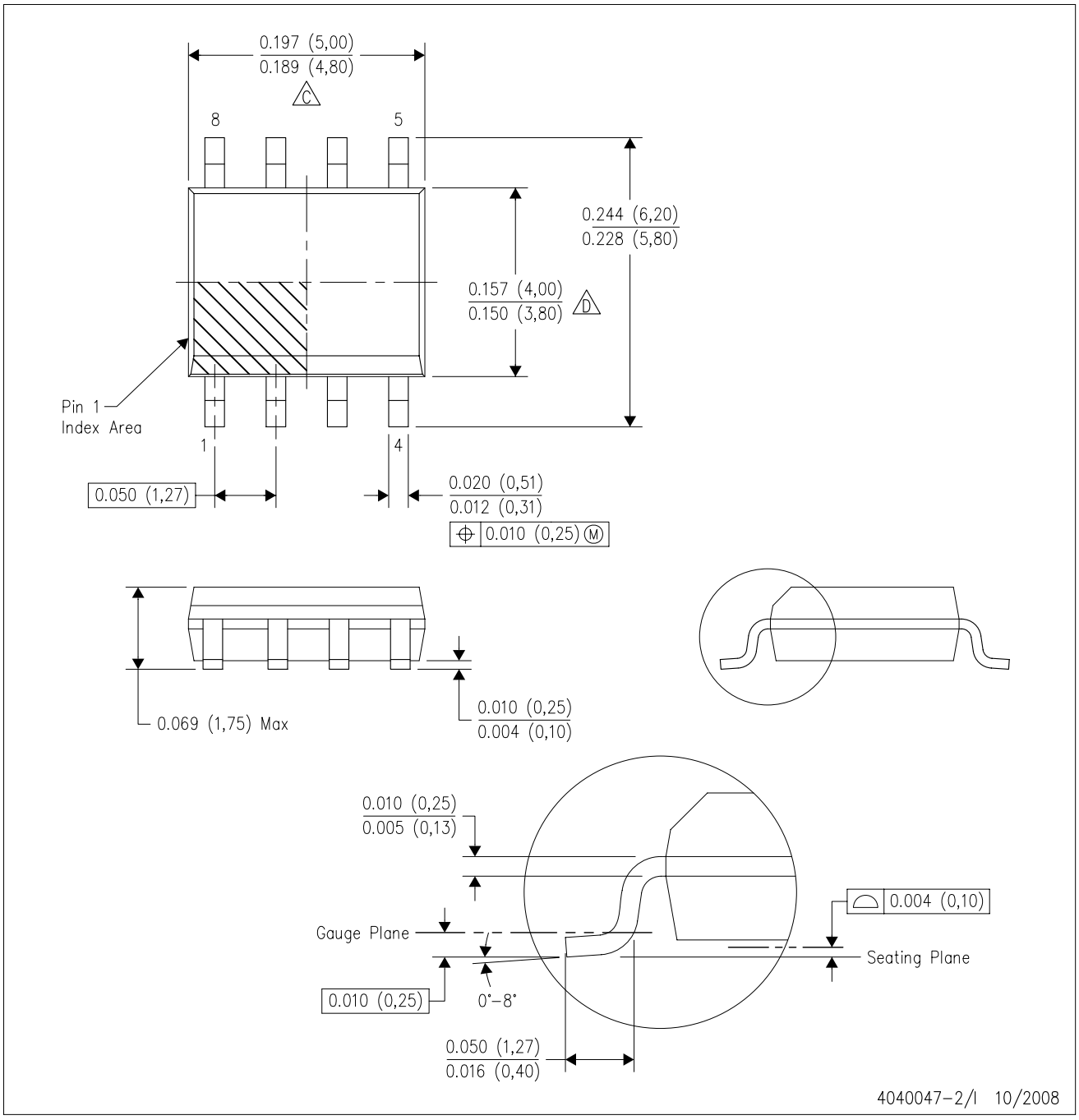
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

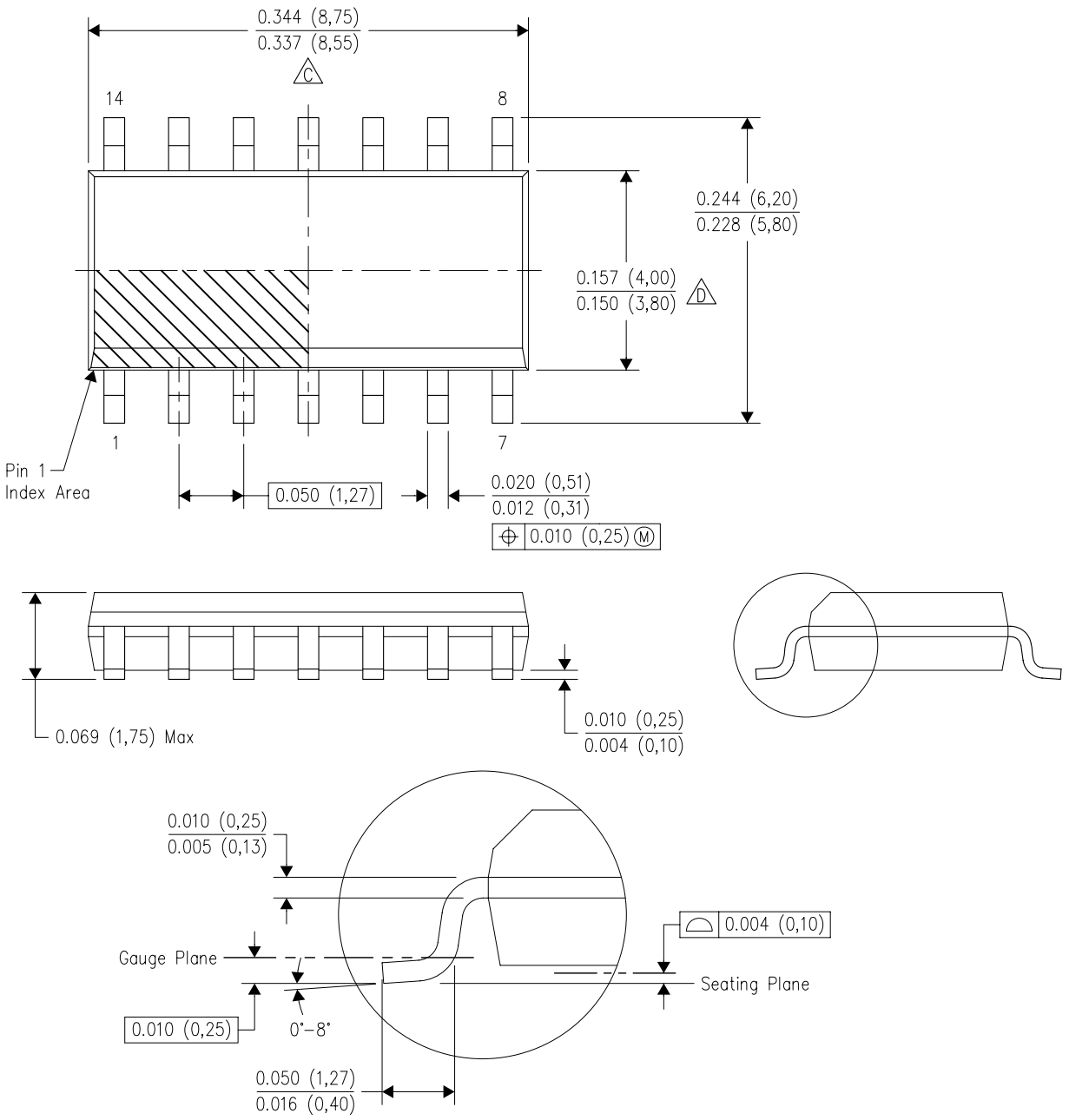
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| THS3112CDDAR | SO PowerPAD | DDA | 8 | 2500 | 346.0 | 346.0 | 29.0 |
| THS3112CDR | SOIC | D | 8 | 2500 | 346.0 | 346.0 | 29.0 |
| THS3112IDDAR | SO PowerPAD | DDA | 8 | 2500 | 346.0 | 346.0 | 29.0 |
| THS3115CPWPR | HTSSOP | PWP | 14 | 2000 | 346.0 | 346.0 | 29.0 |
| THS3115IPWPR | HTSSOP | PWP | 14 | 2000 | 346.0 | 346.0 | 29.0 |

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



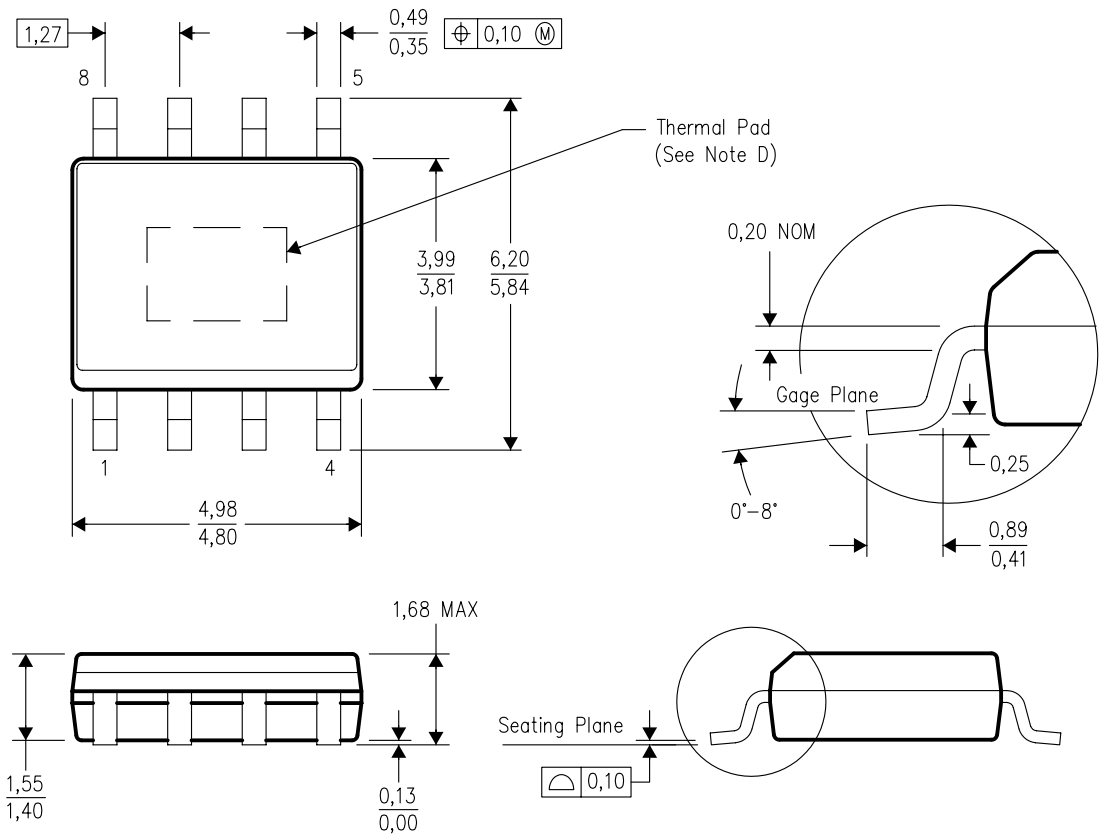

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AB.

## DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE




4202561/D 04/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.

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# THERMAL PAD MECHANICAL DATA

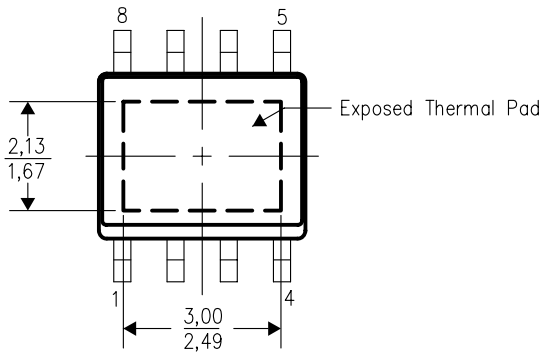
## DDA (R–PDSO–G8)

### THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

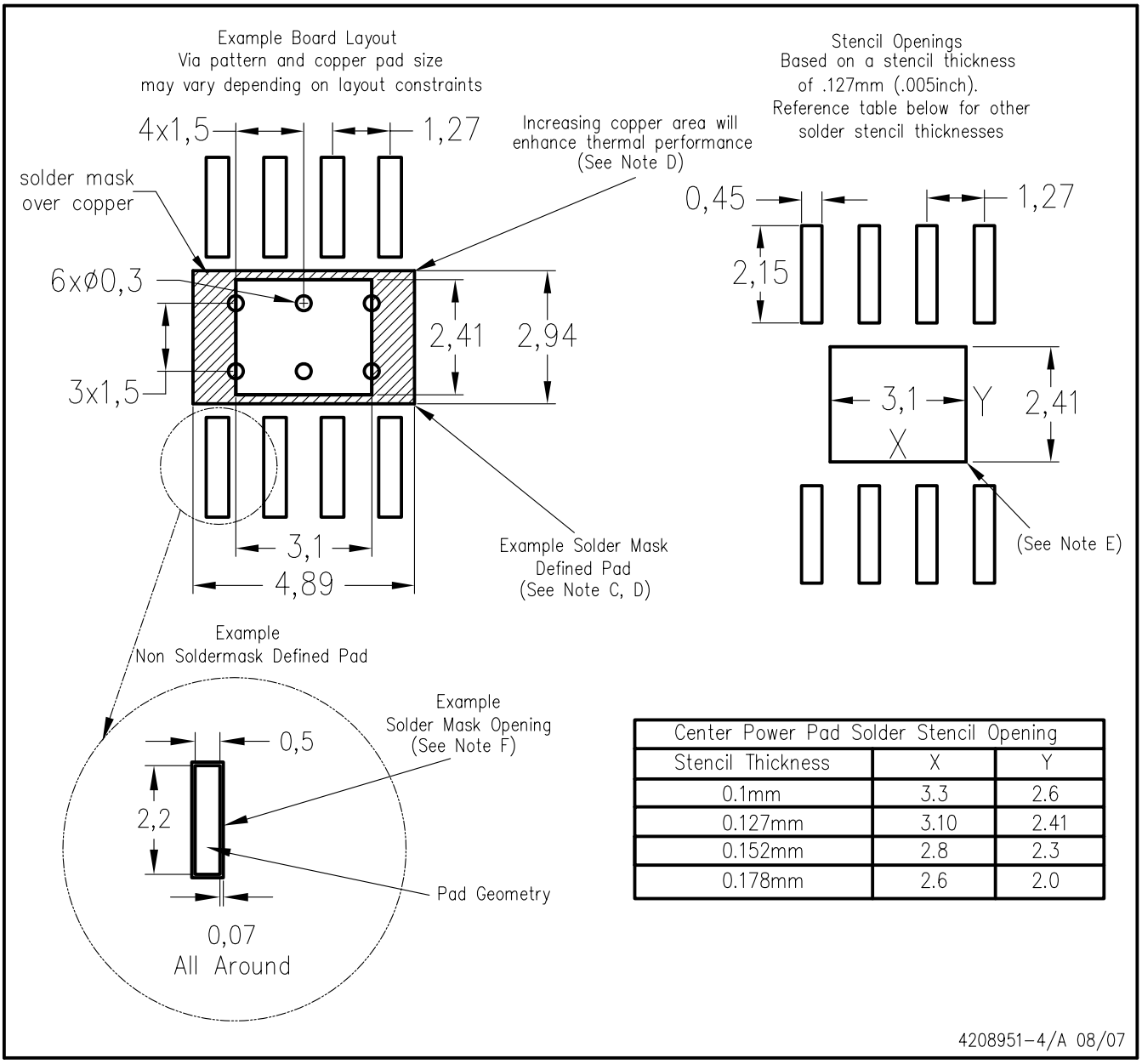



Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

# DDA (R–PDSO–G8) PowerPAD™



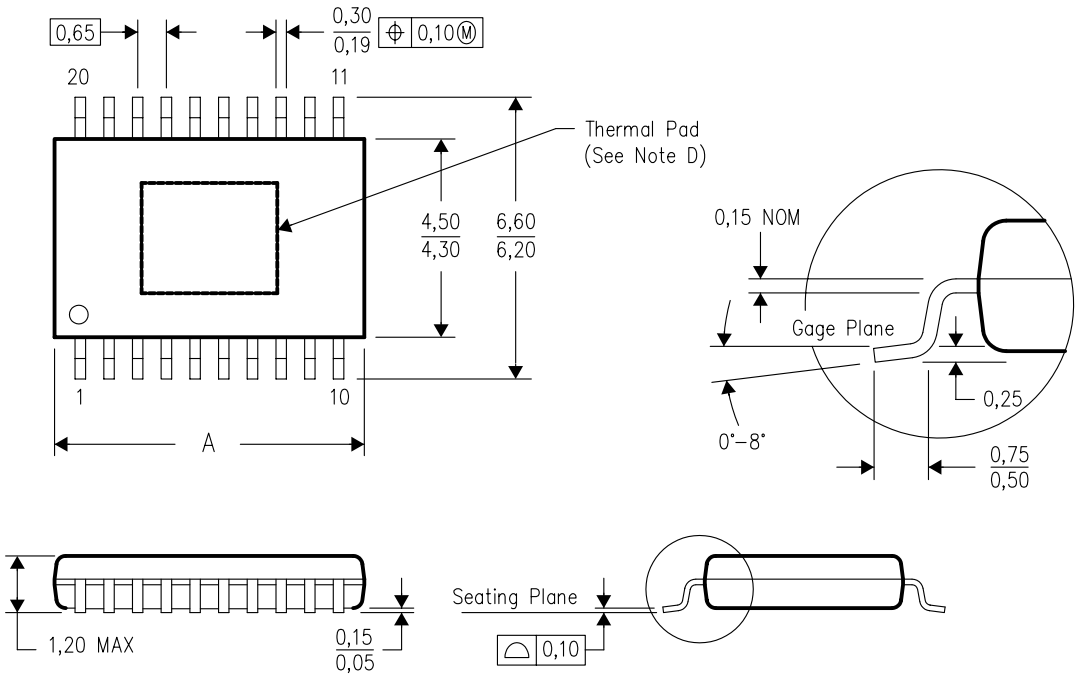

| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 3.3 | 2.6 |
| 0.127mm | 3.10 | 2.41 |
| 0.152mm | 2.8 | 2.3 |
| 0.178mm | 2.6 | 2.0 |

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

## PWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PIN SHOWN




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|
| A MAX | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–153

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# THERMAL PAD MECHANICAL DATA

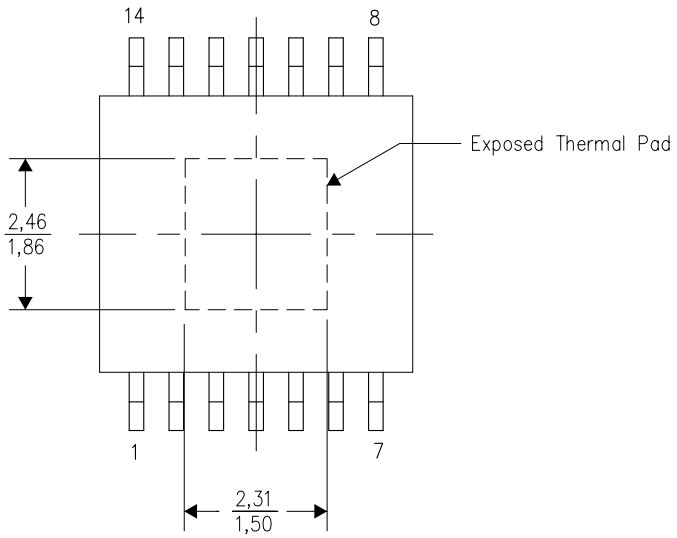
PWP (R–PDSO–G14)

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

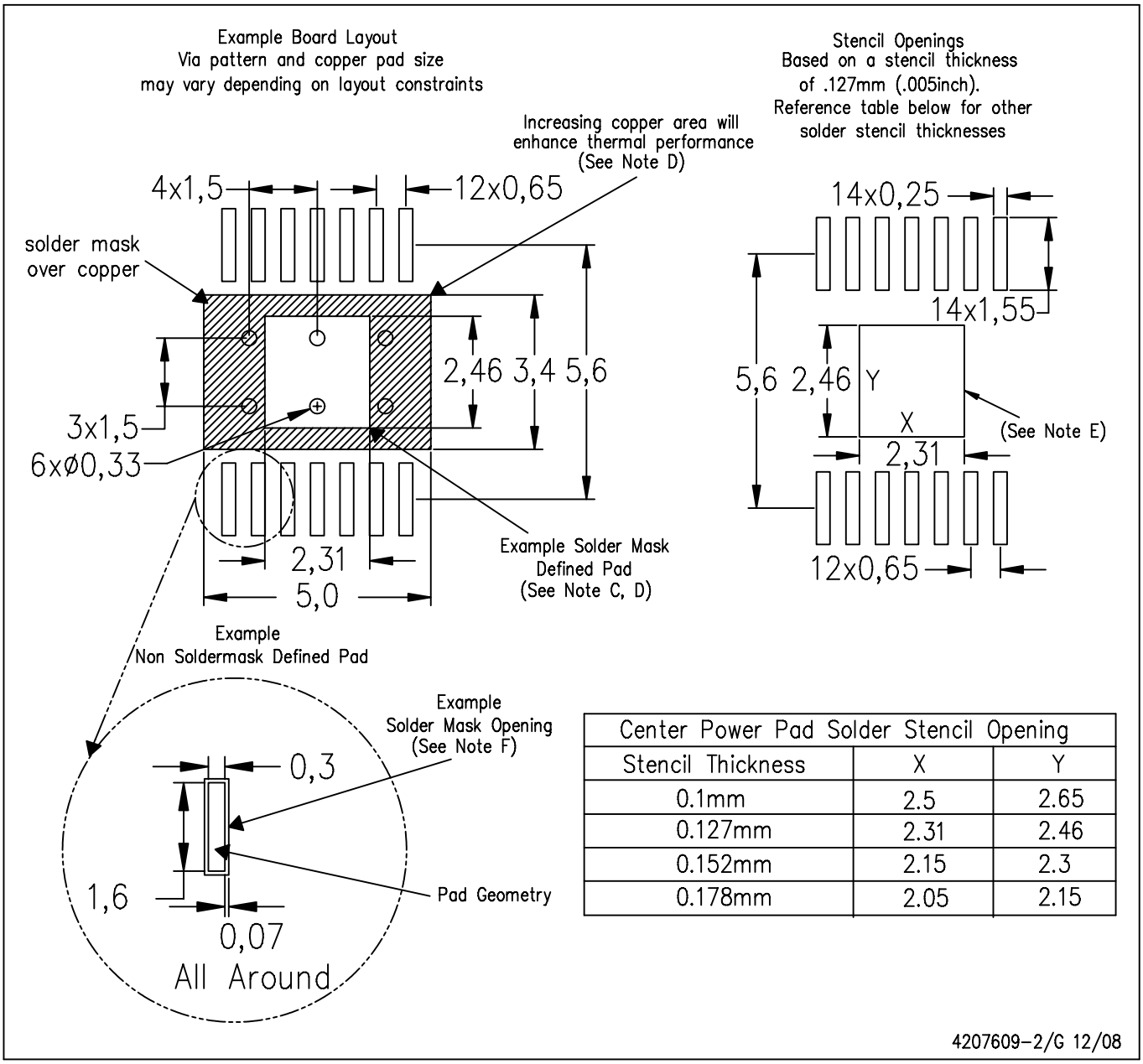



Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

# PWP (R–PDSO–G14) PowerPAD™




| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 2.5 | 2.65 |
| 0.127mm | 2.31 | 2.46 |
| 0.152mm | 2.15 | 2.3 |
| 0.178mm | 2.05 | 2.15 |

4207609–2/G 12/08

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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