

## General-Purpose FET-INPUT OPERATIONAL AMPLIFIERS

### FEATURES

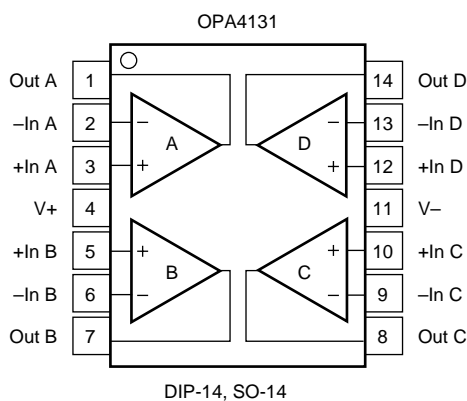
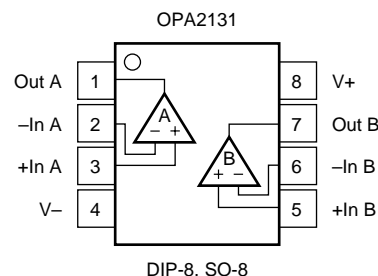
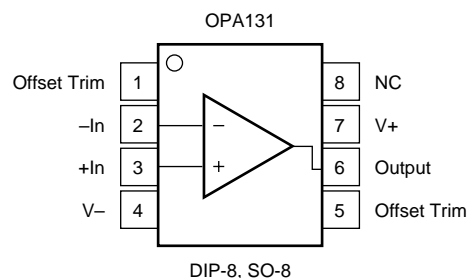
- FET INPUT:  $I_b = 50\text{pA max}$
- LOW OFFSET VOLTAGE:  $750\mu\text{V max}$
- WIDE SUPPLY RANGE:  $\pm 4.5\text{V to } \pm 18\text{V}$
- SLEW RATE:  $10\text{V}/\mu\text{s}$
- WIDE BANDWIDTH:  $4\text{MHz}$
- EXCELLENT CAPACITIVE LOAD DRIVE
- SINGLE, DUAL, QUAD VERSIONS

### DESCRIPTION

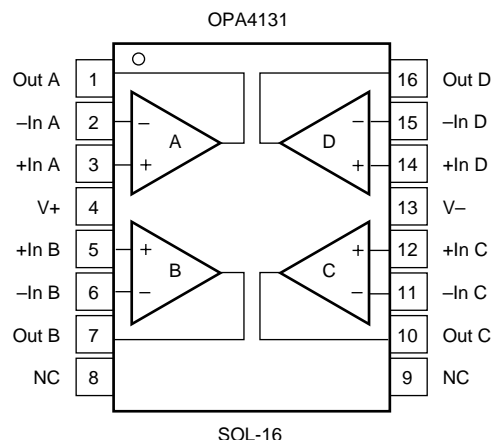
The OPA131 series of FET-input op amps provides high performance at low cost. Single, dual, and quad versions in industry-standard pinouts allow cost-effective design options.

The OPA131 series offers excellent general-purpose performance, including low offset voltage, drift, and good dynamic characteristics.

Single, dual, and quad versions are available in DIP and SO packages. Performance grades include commercial and industrial temperature ranges.



NC = No Connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Supply Voltage, V+ to V–	36V
Input Voltage	(V–) – 0.7V to (V+) + 0.7V
Output Short-Circuit <sup>(2)</sup>	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Short-circuit to ground, one amplifier per package.



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR <sup>(1)</sup>	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
<b>Single</b>						
OPA131	SO-8	D	–40°C to +85°C	OPA131UJ	OPA131UJ	Rails, 100
"	"	"	"	"	OPA131UJ/2K5	Tape and Reel, 2500
OPA131	SO-8	D	–40°C to +85°C	OPA131UA	OPA131UA	Rails, 100
"	"	"	"	"	OPA131UA/2K5	Tape and Reel, 2500
OPA131	SO-8	D	–40°C to +85°C	OPA131U	OPA131U	Rails, 100
"	"	"	"	"	OPA131U/2K5	Tape and Reel, 2500
<b>Dual</b>						
OPA2131	SO-8	D	–40°C to +85°C	OPA2131UJ	OPA2131UJ	Rails, 100
"	"	"	"	"	OPA2131UJ/2K5	Tape and Reel, 2500
OPA2131	SO-8	D	–40°C to +85°C	OPA2131UA	OPA2131UA	Rails, 100
"	"	"	"	"	OPA2131UA/2K5	Tape and Reel, 2500
<b>Quad</b>						
OPA4131	DIP-14	N	–40°C to +85°C	OPA4131PJ	OPA4131PJ	Rails, 25
"	"	"	"	OPA4131PA	OPA4131PA	Rails, 25
OPA4131	SOL-16	DW	–40°C to +85°C	OPA4131UA	OPA4131UA	Rails, 48
"	"	"	"	"	OPA4131UA/1K	Tape and Reel, 1000
OPA4131	SOL-14	D	–40°C to +85°C	OPA4131NJ	OPA4131NJ	Rails, 58
"	"	"	"	OPA4131NA	OPA4131NA	Rails, 58

NOTE: (1) For the most current specifications and package information, refer to our web site at [www.ti.com](http://www.ti.com).

# ELECTRICAL CHARACTERISTICS

At  $T_A = +25^{\circ}\text{C}$ ,  $V_S = \pm 15\text{V}$ , and  $R_L = 2\text{k}\Omega$ , unless otherwise noted.

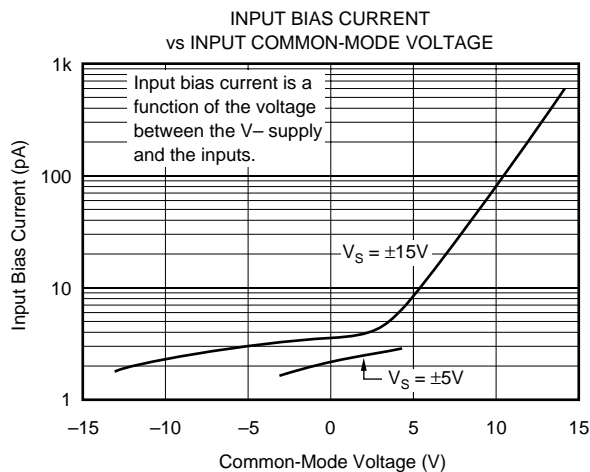
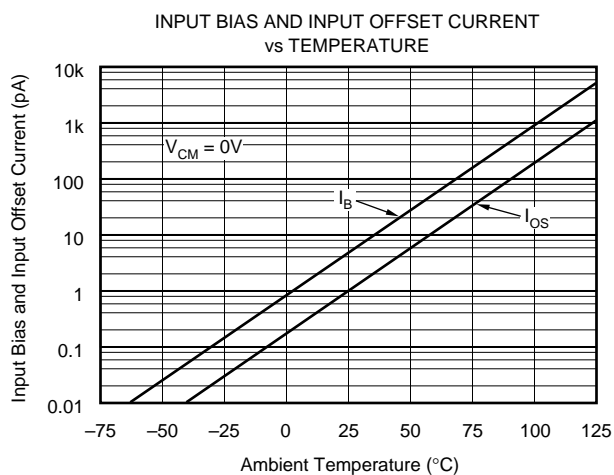
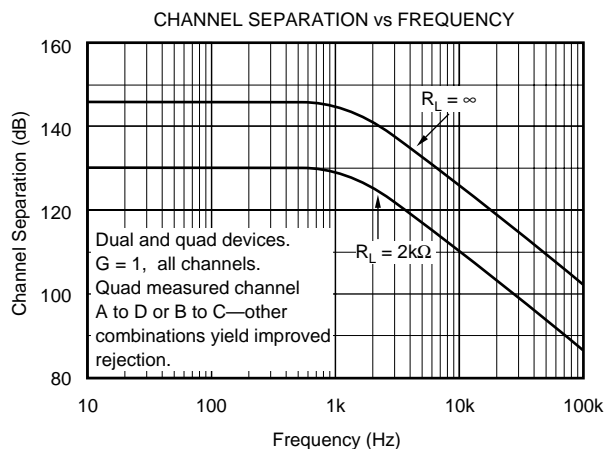
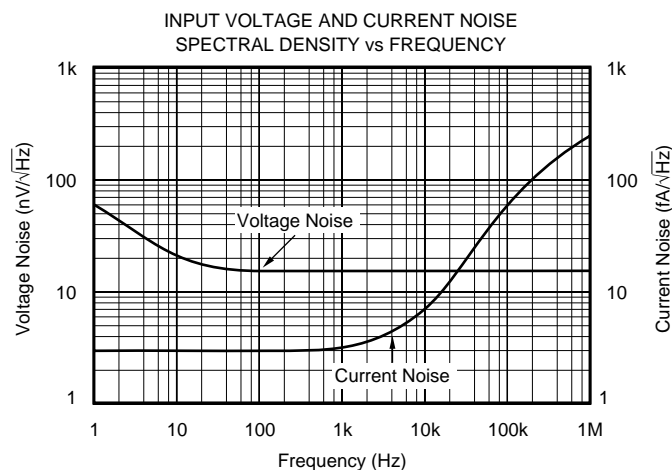
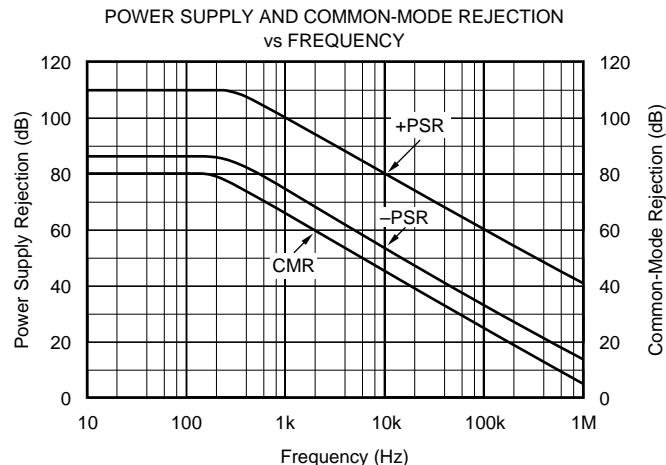
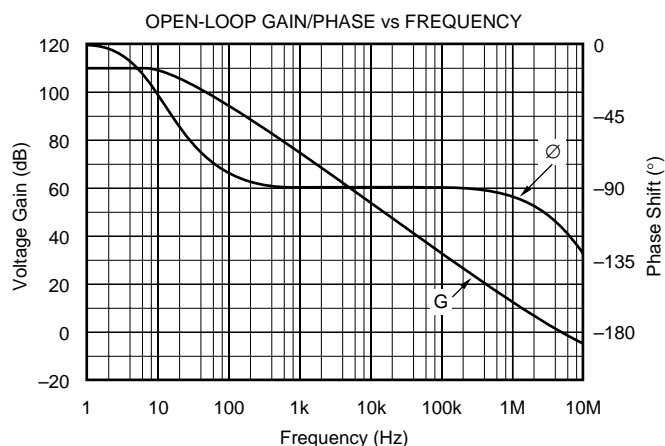
PARAMETER	CONDITION	OPA131UA OPA2131UA OPA4131PA, UA, NA			OPA131UJ OPA2131UJ OPA4131PJ, NJ			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>OFFSET VOLTAGE</b> Input Offset Voltage OPA131U model only vs Temperature <sup>(1)</sup> vs Power Supply OPA131U model only	Operating Temperature Range $V_S = \pm 4.5\text{V}$ to $\pm 18\text{V}$		$\pm 0.2$ $\pm 0.2$ $\pm 2$ 50 50	$\pm 1$ 0.75 $\pm 10$ 200 100		*	$\pm 1.5$	mV mV $\mu\text{V}/^{\circ}\text{C}$ $\mu\text{V}/\text{V}$ $\mu\text{V}/\text{V}$
<b>INPUT BIAS CURRENT<sup>(2)</sup></b> Input Bias Current vs Temperature Input Offset Current	$V_{CM} = 0\text{V}$ $V_{CM} = 0\text{V}$		+5 See Typical Characteristic $\pm 1$	$\pm 50$ $\pm 50$		*	*	pA pA
<b>NOISE</b> Input Voltage Noise Noise Density, $f = 10\text{Hz}$ $f = 100\text{Hz}$ $f = 1\text{kHz}$ $f = 10\text{kHz}$ Current Noise Density, $f = 1\text{kHz}$			21 16 15 15 3			*		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{fA}/\sqrt{\text{Hz}}$
<b>INPUT VOLTAGE RANGE</b> Common-Mode Voltage Range Common-Mode Rejection OPA131U model only	$V_{CM} = -12\text{V}$ to $+14\text{V}$	(V-) + 3 70 80	80 86	(V+) - 1	*	*	*	V dB dB
<b>INPUT IMPEDANCE</b> Differential Common-Mode	$V_{CM} = 0\text{V}$		$10^{10} \parallel 1$ $10^{12} \parallel 3$			*		$\Omega \parallel \text{pF}$ $\Omega \parallel \text{pF}$
<b>OPEN-LOOP GAIN</b> Open-Loop Voltage Gain OPA131U model only	$V_O = -12\text{V}$ to $+12\text{V}$	94 100	110 110		*	*		dB dB
<b>FREQUENCY RESPONSE</b> Gain-Bandwidth Product Slew Rate Settling Time 0.1% 0.01% Total Harmonic Distortion + Noise	$G = -1$ , 10V Step, $C_L = 100\text{pF}$ $G = -1$ , 10V Step, $C_L = 100\text{pF}$ 1kHz, $G = 1$ , $V_O = 3.5\text{V}_{\text{rms}}$		4 10 1.5 2 0.0008			*		MHz $\text{V}/\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$ %
<b>OUTPUT</b> Voltage Output, Positive Negative Short-Circuit Current		(V+) - 3 (V-) + 3	(V+) - 2.5 (V-) + 2.5 $\pm 25$		*	*		V V mA
<b>POWER SUPPLY</b> Specified Operating Voltage Operating Voltage Range Quiescent Current (per amplifier)	$I_O = 0$	$\pm 4.5$	$\pm 15$ $\pm 1.5$	$\pm 18$ $\pm 1.75$	*	*	*	V V mA
<b>TEMPERATURE RANGE</b> Operating Range Storage Thermal Resistance, $\theta_{JA}$ DIP-8 SO-8 DIP-14 SO-14, SOL-16		-55 -55	100 150 80 110	+125 +125	-55 *		+125 *	$^{\circ}\text{C}$ $^{\circ}\text{C}$ $^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$

\* Specifications same as OPA131UA.

NOTES: (1) Ensured by wafer test. (2) High-speed test at  $T_J = 25^{\circ}\text{C}$ .

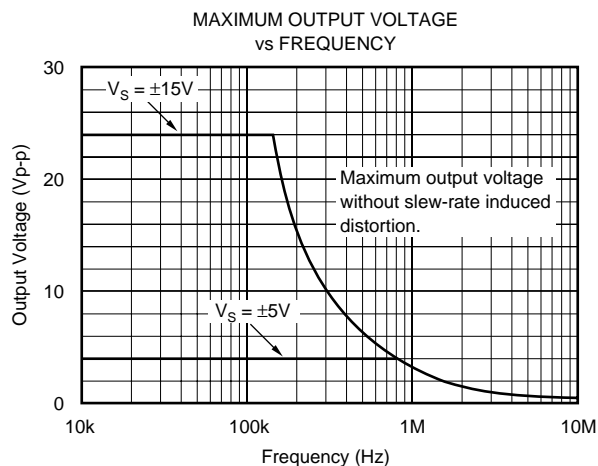
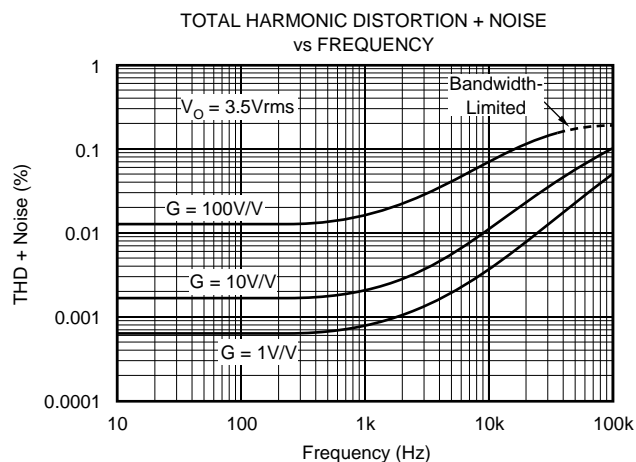
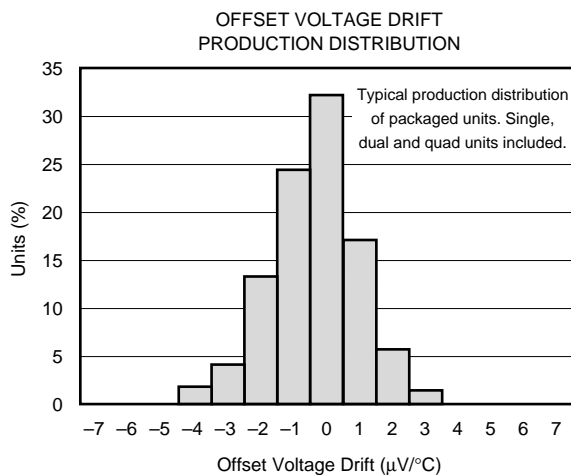
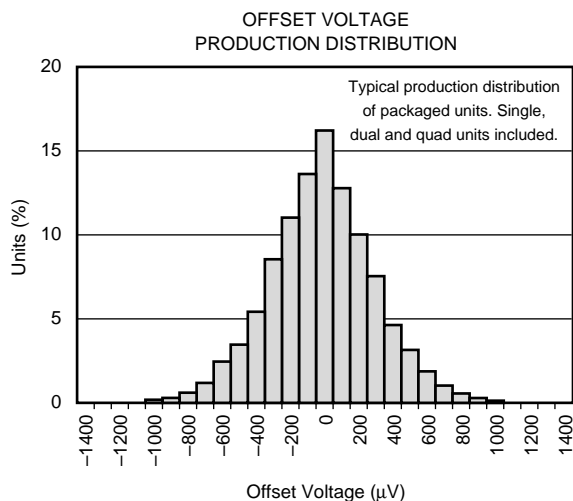
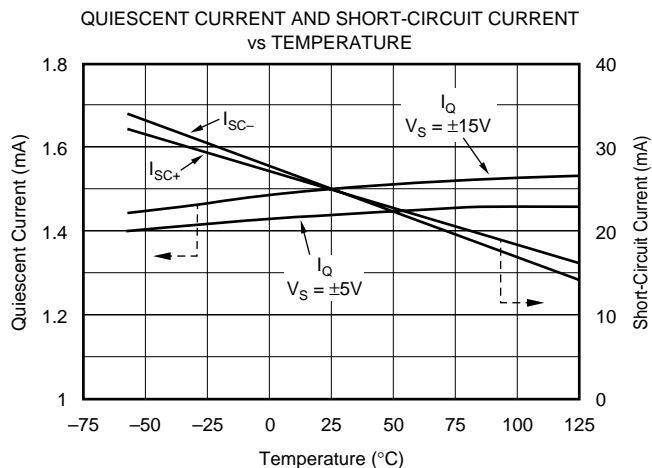
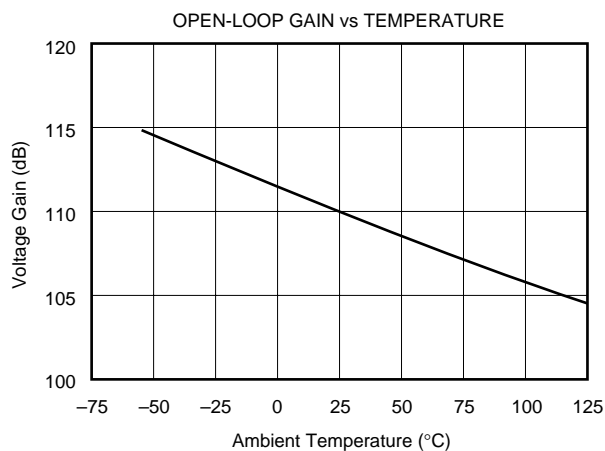
# TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , and  $R_L = 2\text{k}\Omega$ , unless otherwise noted.



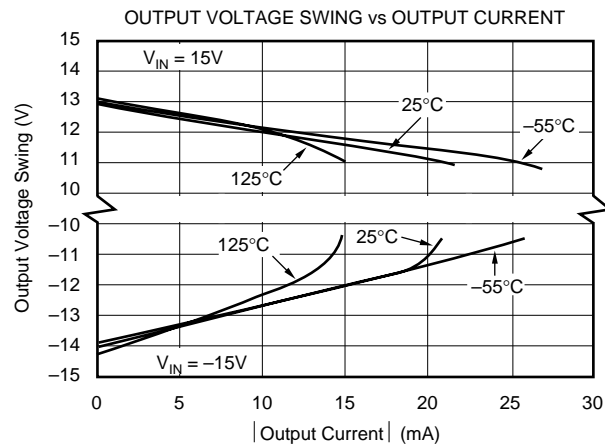
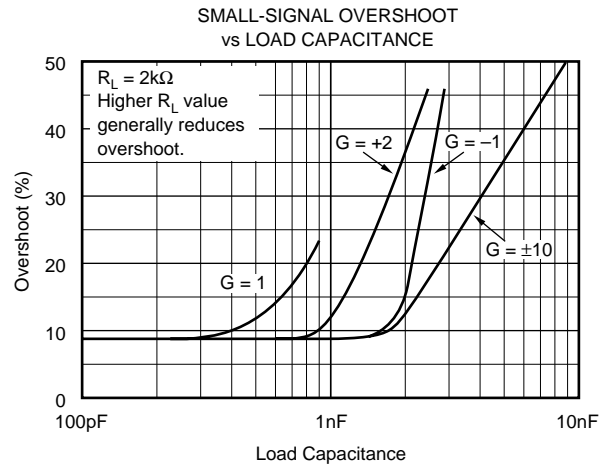
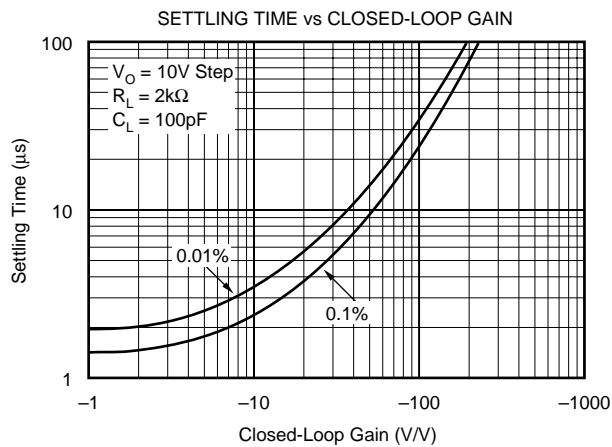
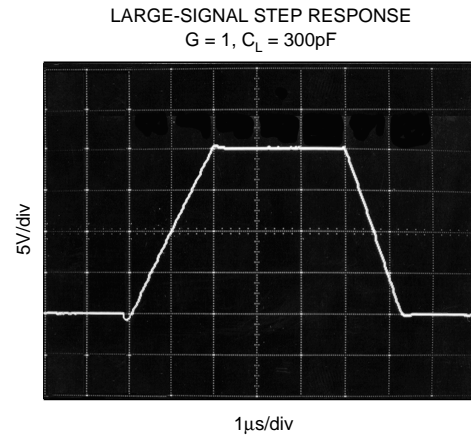
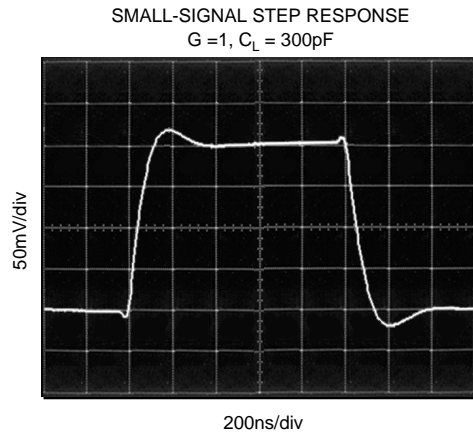
# TYPICAL CHARACTERISTICS (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , and  $R_L = 2\text{k}\Omega$ , unless otherwise noted.



# TYPICAL CHARACTERISTICS (Cont.)

At  $T_{CASE} = +25^{\circ}C$ ,  $V_S = \pm 15V$ , and  $R_L = 2k\Omega$ , unless otherwise noted.



# APPLICATIONS INFORMATION

The OPA131 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. Power-supply pins should be bypassed with 10nF ceramic capacitors or larger.

The OPA131 series op amps are free from unexpected output phase-reversal common with FET op amps. Many FET-input op amps exhibit phase-reversal of the output when the input common-mode voltage range is exceeded. This can occur in voltage-follower circuits, causing serious problems in control-loop applications. All circuitry is completely independent in dual and quad versions, assuring normal behavior when one amplifier in a package is overdriven or short-circuited.

## OFFSET VOLTAGE TRIM

The OPA131 (single op amp version) provides offset voltage trim connections on pins 1 and 5. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 1. This adjustment should be used only to null the offset of the op amp, not system offset or offset produced by the signal source.

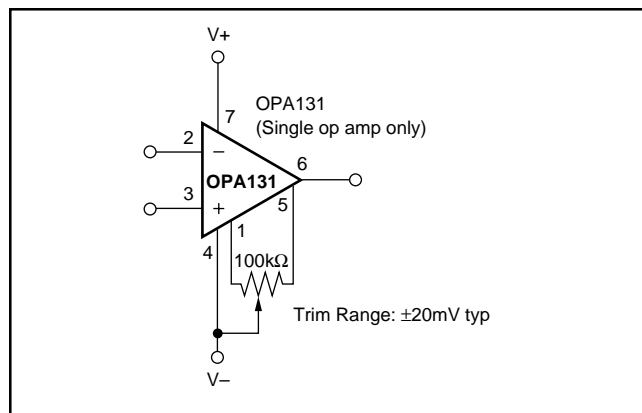


FIGURE 1. OPA131 Offset Voltage Trim Circuit.

## INPUT BIAS CURRENT

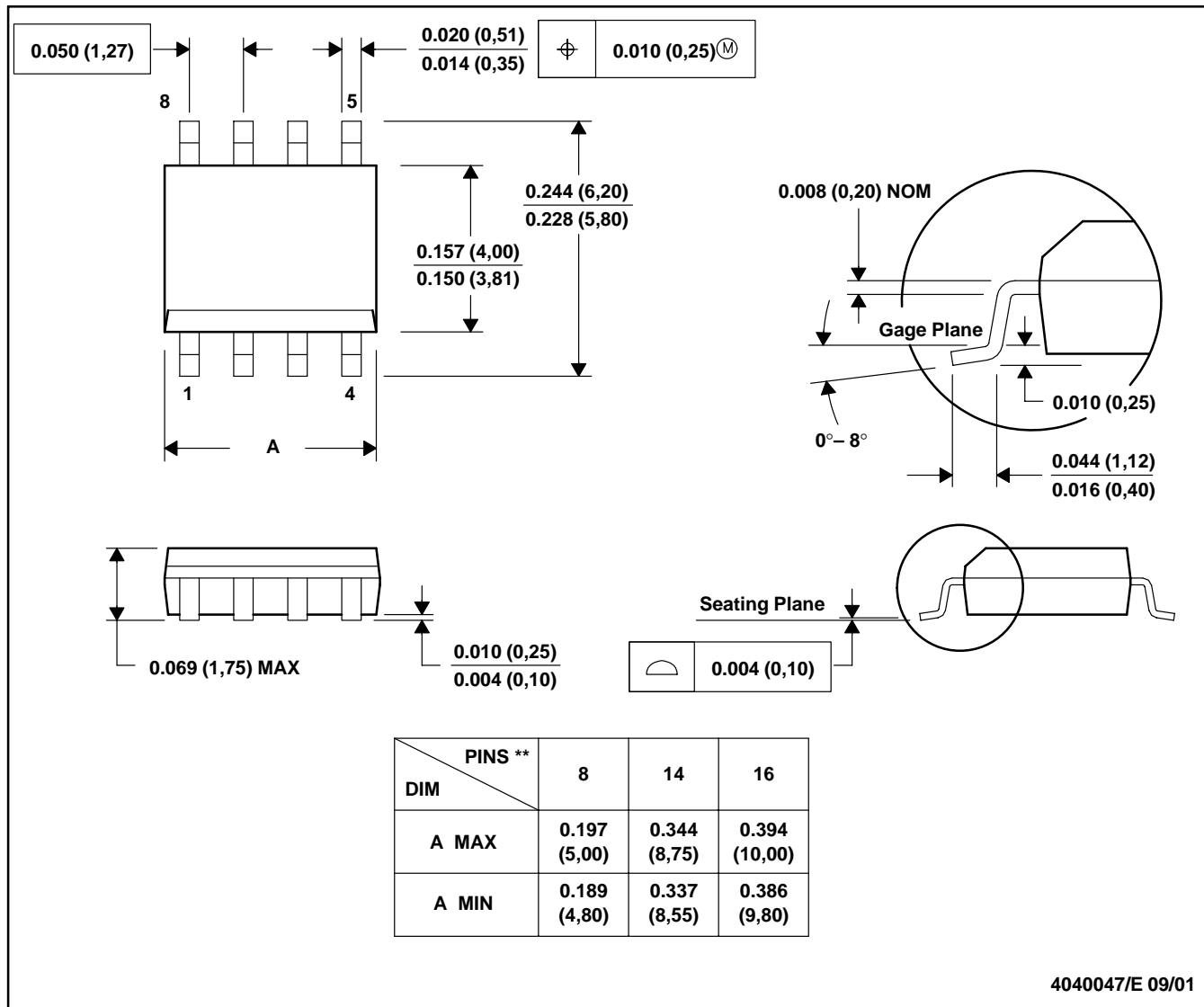
The input bias current is approximately 5pA at room temperature and increases with temperature as shown in the typical characteristic "Input Bias Current vs Temperature."

Input bias current also varies with common-mode voltage and power supply voltage. This variation is dependent on the voltage between the negative power supply and the common-mode input voltage. The effect is shown in the typical curve "Input Bias Current vs Common-Mode Voltage."

D (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



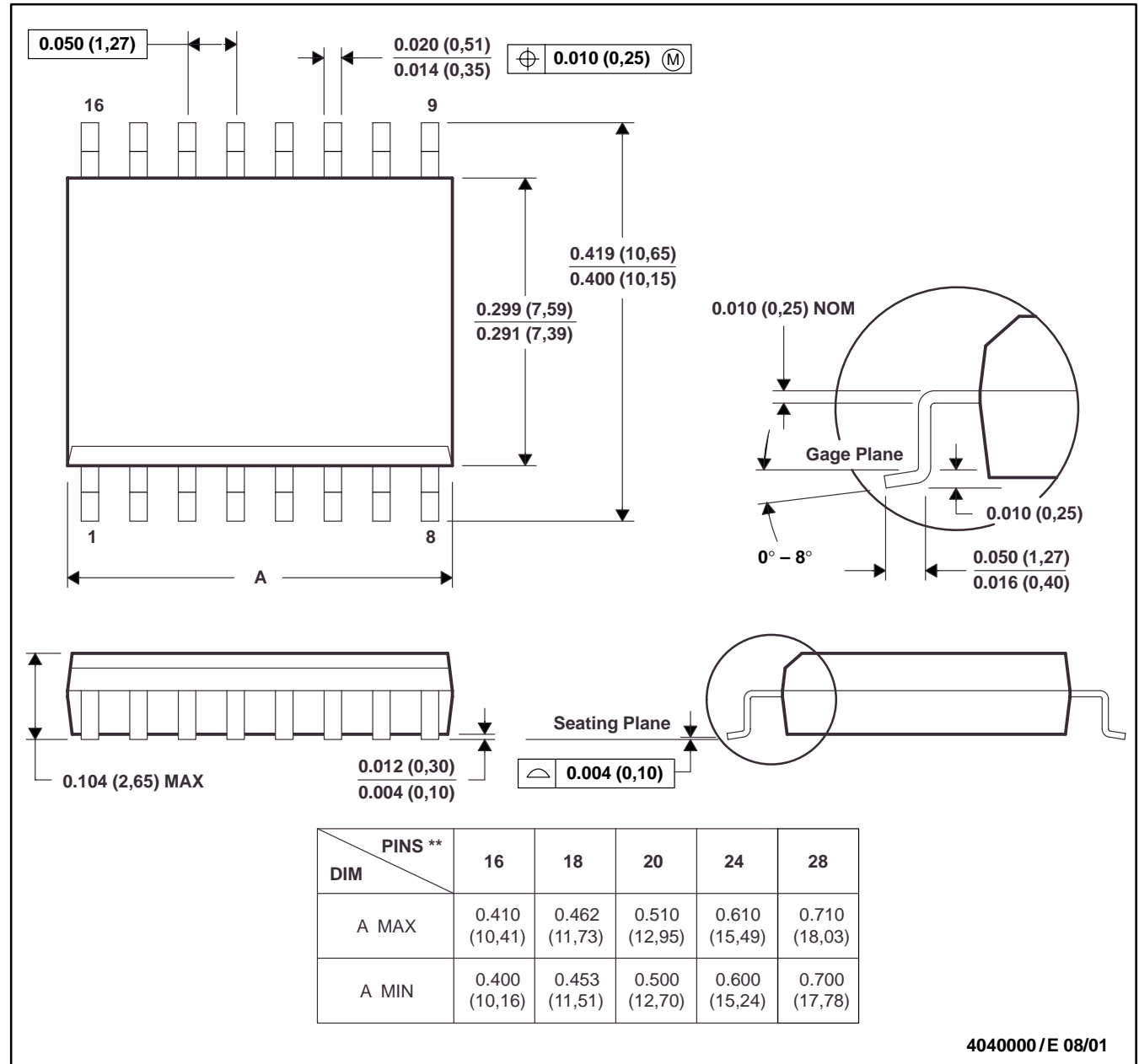
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012



DW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN

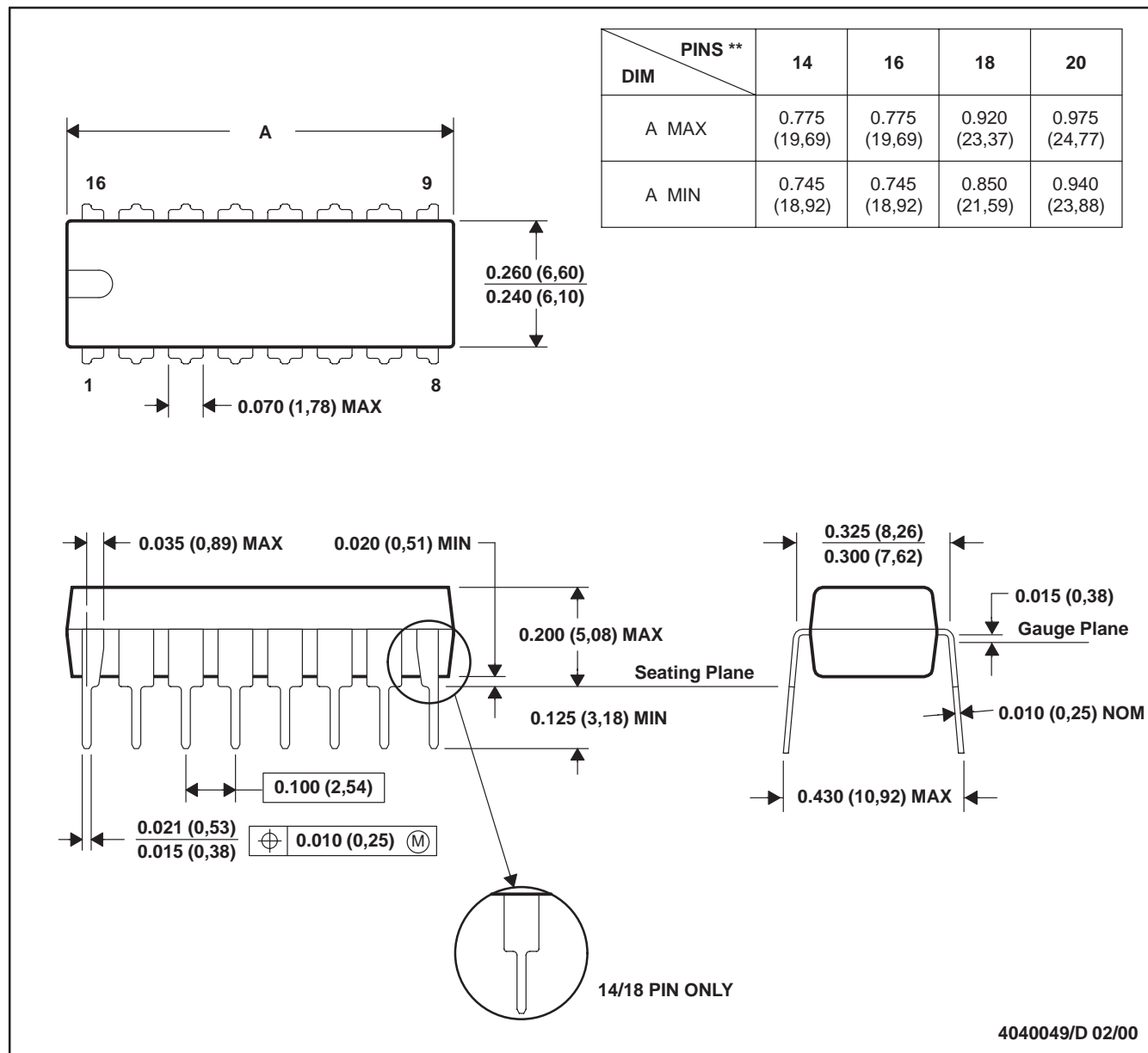


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-013

N (R-PDIP-T\*\*)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001).

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
OPA131P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
OPA131PA	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
OPA131PJ	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
OPA131U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA131UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA131UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA131UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA131UAE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA131UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA131UJ	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA131UJ/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA131UJ/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA131UJE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2131PA	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
OPA2131PJ	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
OPA2131UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2131UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2131UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2131UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2131UAE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2131UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2131UJ	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2131UJ/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2131UJ/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2131UJG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA4131NA	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA4131NAG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
OPA4131NJ	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA4131NJG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA4131PA	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA4131PAG4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA4131PJ	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA4131PJG4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA4131UA	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	Cu NiPdAu	Level-3-260C-168 HR
OPA4131UA/1K	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	Cu NiPdAu	Level-3-260C-168 HR
OPA4131UA/1KG4	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	Cu NiPdAu	Level-3-260C-168 HR
OPA4131UAG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	Cu NiPdAu	Level-3-260C-168 HR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

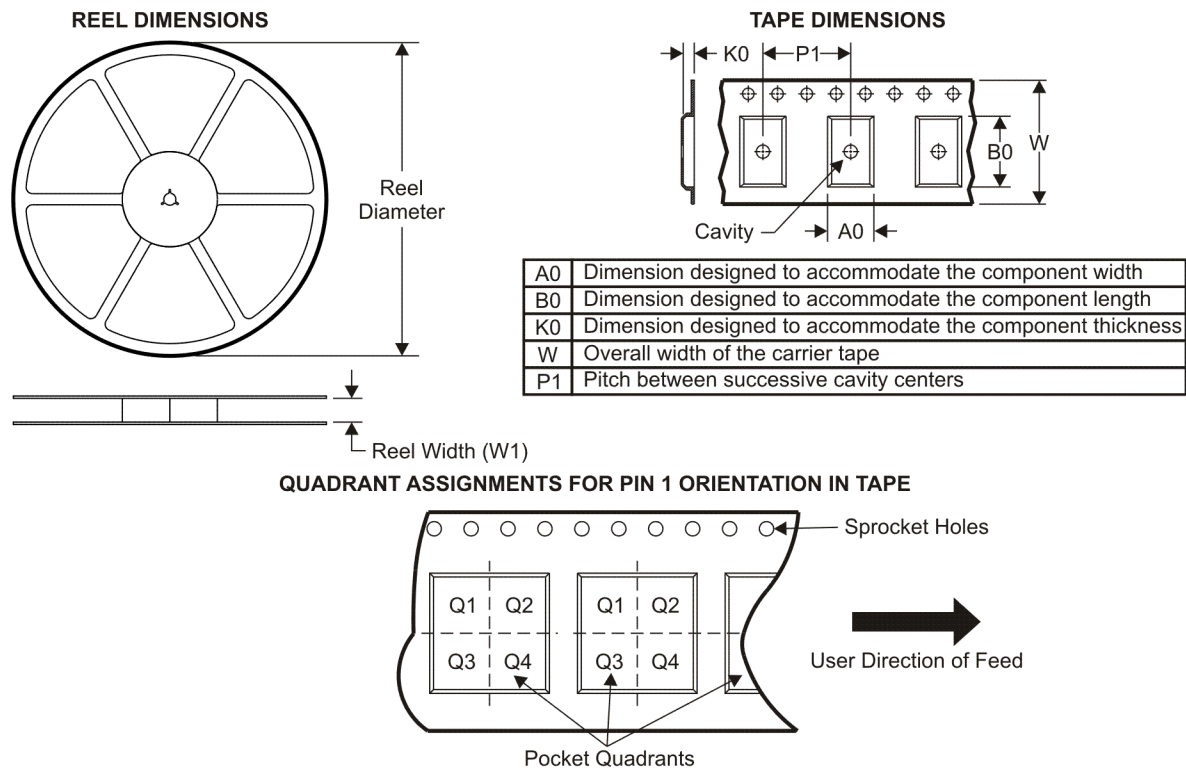
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA131UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA131UJ/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2131UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2131UJ/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4131UA/1K	SOIC	DW	16	1000	330.0	16.4	10.85	10.8	2.7	12.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS

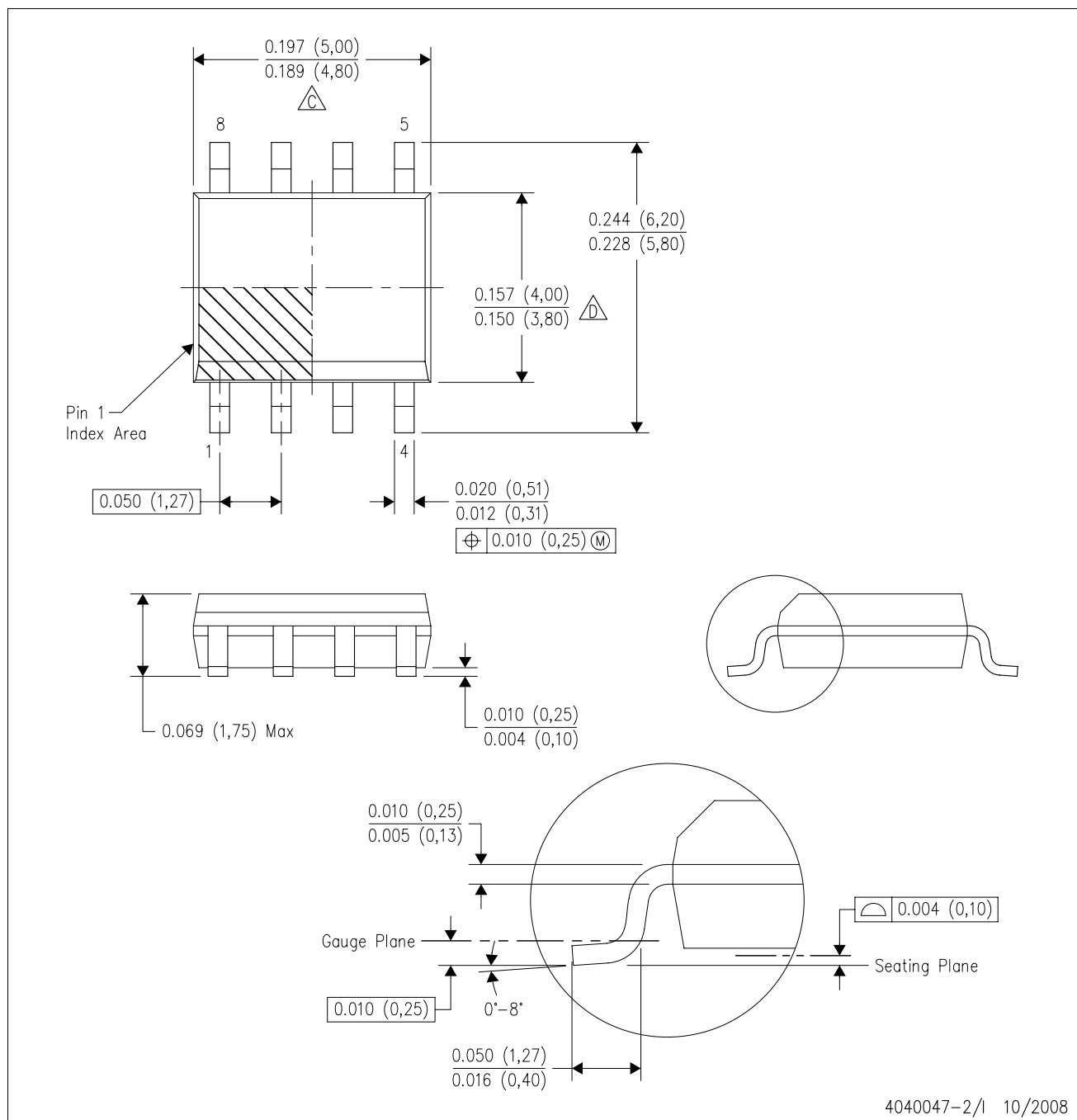


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA131UA/2K5	SOIC	D	8	2500	346.0	346.0	29.0
OPA131UJ/2K5	SOIC	D	8	2500	346.0	346.0	29.0
OPA2131UA/2K5	SOIC	D	8	2500	346.0	346.0	29.0
OPA2131UJ/2K5	SOIC	D	8	2500	346.0	346.0	29.0
OPA4131UA/1K	SOIC	DW	16	1000	346.0	346.0	33.0

D (R-PDSO-G8)

# PLASTIC SMALL-OUTLINE PACKAGE

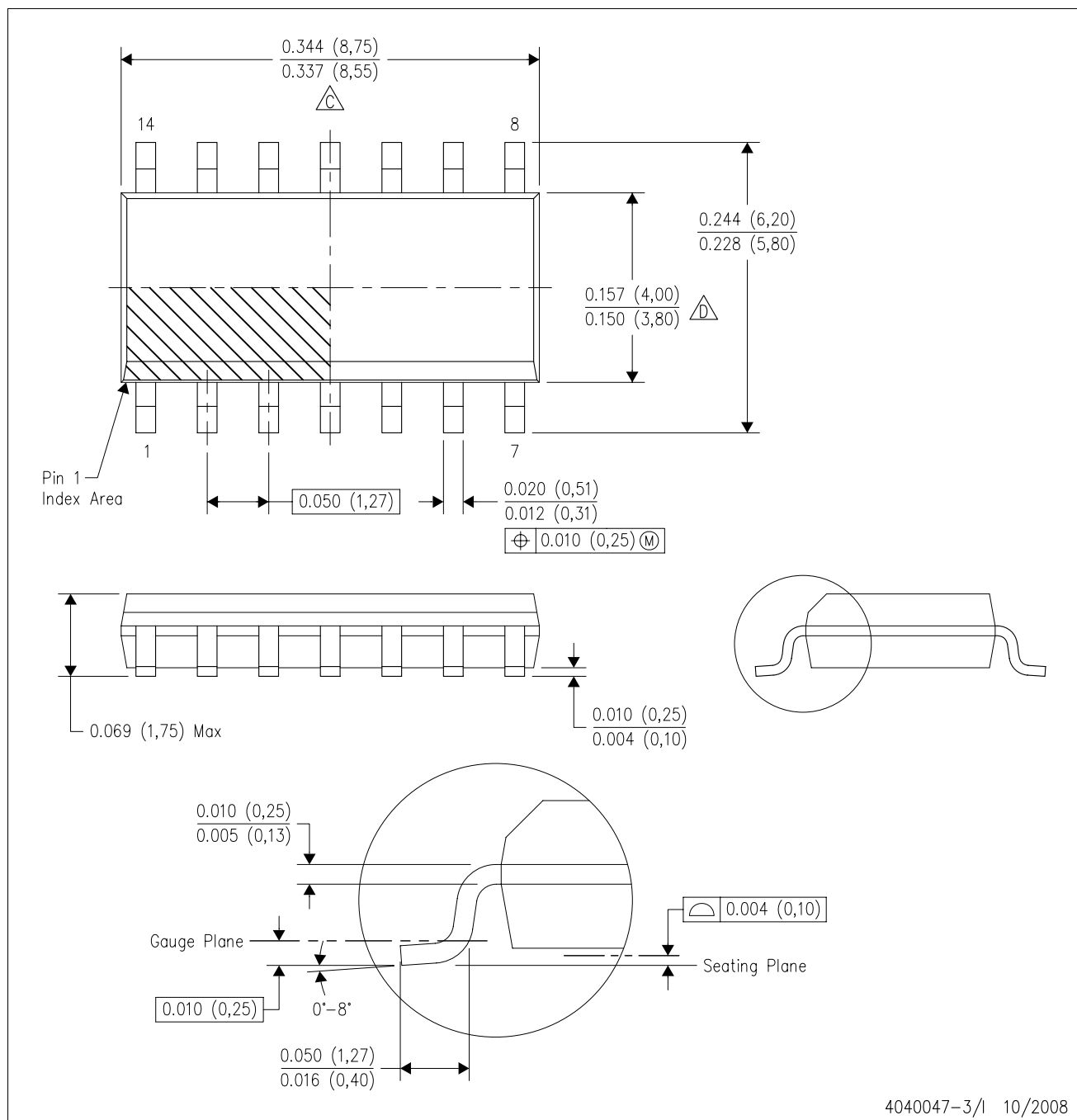


NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.  
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.  
E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AB.



## P (R-PDIP-T8)

## PLASTIC DUAL-IN-LINE

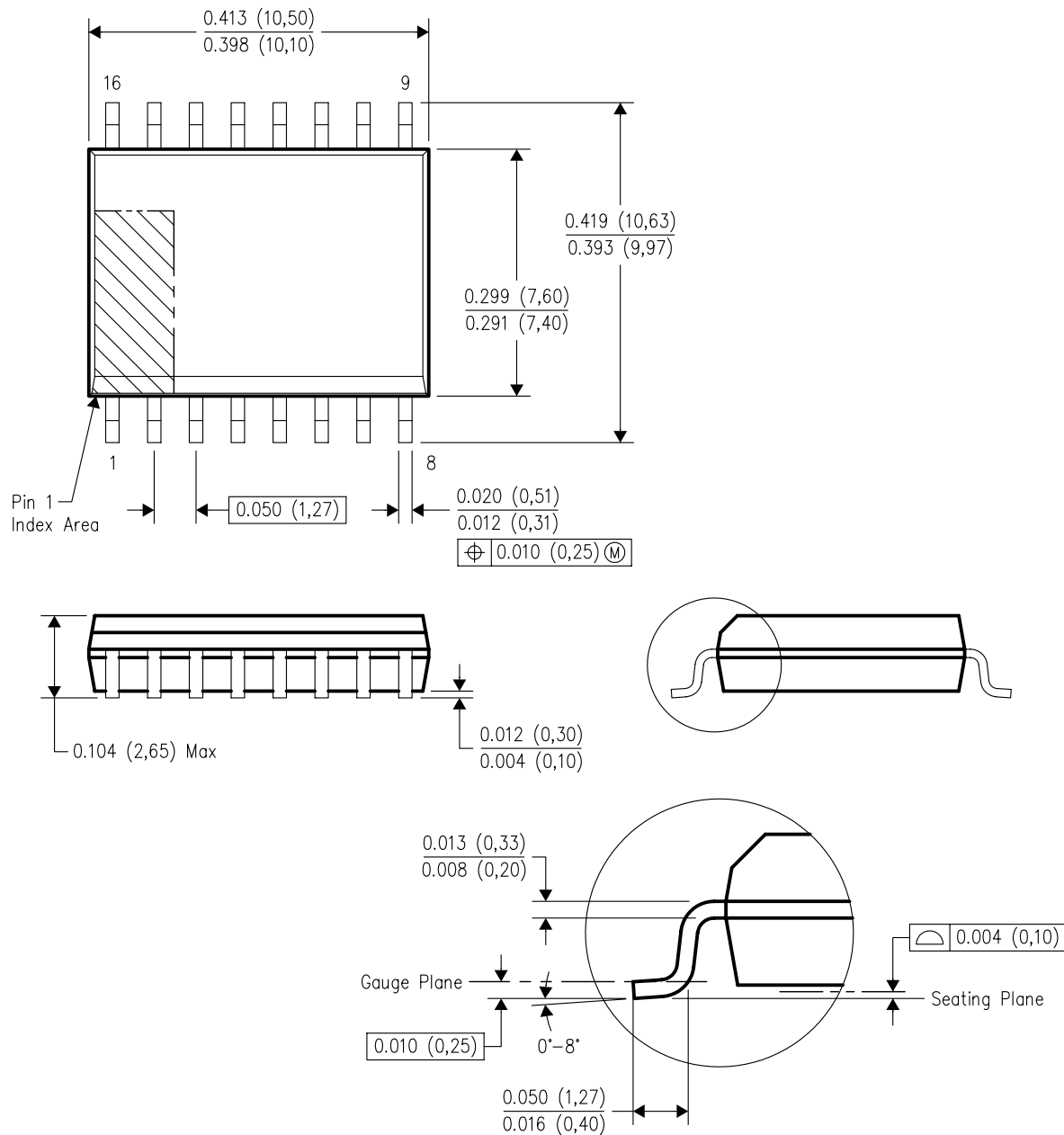


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001

For the latest package information, go to [http://www.ti.com/sc/docs/package/pkg\\_info.htm](http://www.ti.com/sc/docs/package/pkg_info.htm)

## DW (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE



4040000-2/F 06/2004

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed  $0.006 (0,15)$ .
  - Falls within JEDEC MS-013 variation AA.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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