Intel® 80312 I/O Companion Chip

Specification Update

November 2001

Notice: The Intel® 80312 processor may contain design defects or errors known as errata. Characterized errata that may cause the product's behavior to deviate from published specifications are documented in this specification update.

Order Number: 273416-006

Contents

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Revision History

Date	Version	Description
11/15/01	006	Added Specification Clarifications 6 and 7. Added Documentation Changes 15 and 16.
08/21/01	005	Added Specification Clarifications 4 and 5. Added Documentation Changes 10 through 14.
05/04/01	004	Added Document Changes 6 through 9.
04/02/01	003	Added Specification Clarification 3.
03/22/01	002	Added Errata 1. Added Specification Clarifications 1 and 2. Added Document Changes 1 through 5.
08/00	001	This is the new Specification Update document. It contains all identified errata published prior to this date.

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order #
Intel® 80312 I/O Companion Chip Developer's Manual	273410
Intel® 80312 I/O Companion Chip Specification Update	273416
Intel® 80200 Processor based on Intel® XScale™ Microarchitecture Developer's Manual	273411
Intel® 80310 I/O Processor Chipset with Intel® XScale™ Microarchitecture Design Guide	273354
Intel® 80200 Processor based on Intel® XScale™ Microarchitecture Datasheet	273414

Nomenclature

Errata are design defects or errors. These may cause the Product Name's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Product Name product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

▌	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	Errata
	A-0	A-1	A-2			
1	X	X	X	11	NoFix	Single-bit and Multi-bit Error Reporting Cannot Be Individually Enabled by ECC Control Register

Specification Changes

No.	Steppings			Page	Status	Specification Changes
	#-#	#-#	#-#			
						None for this revision of this specification update.

Specification Clarifications

No.	Steppings			Page	Status	Specification Clarifications
	A-0	A-1	A-2			
1	X	X	X	13	Doc	ECC is Always Enabled
2	X	X	X	13	Doc	32-bit SDRAM is Not Supported
3	X	X	X	13	Doc	Non-Battery Backup Systems
4	X	X	X	13	Doc	IRQISR bit 9 can be read as a '1'
5	X	X	X	14	Doc	POCCDR and SOCCDR Functionality
6	X	X	X	14	Doc	'Bus Hold' Devices on the RAD Bus
7	X	X	X	14	Doc	SREQ64# Functionality

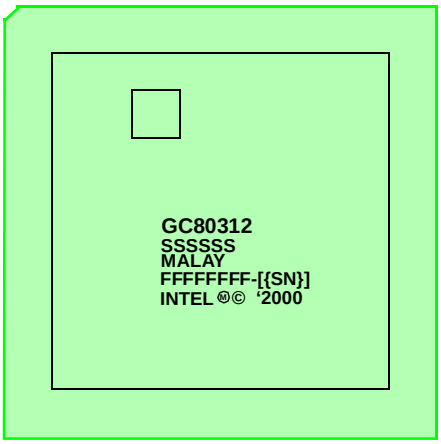
Documentation Changes

No.	Document Revision	Page	Status	Documentation Changes
1	273410-001	15	Doc	Section 3.2.4.3 on page 3-29 has incorrect data
2	273410-001	15	Doc	Figure 5-3 on page 5-7 has missing text
3	273410-001	15	Doc	Section 5.7.38 on page 5-100 has incorrect data
4	273410-001	15	Doc	Section 3.2.3.1 on page 3-13 has incorrect data
5	273410-001	15	Doc	Table 3-4 on page 3-9 has incorrect data
6	273410-001	16	Doc	Table 3-13 on page 3-29 has incorrect data
7	273410-001	17	Doc	Section 3.2.4.3, First paragraph after Table 3-13 has incorrect data
8	273410-001	17	Doc	Section 3.2.4.3, First paragraph after “current” Figure 3-17. H-Matrix has incorrect data
9	273410-001	17	Doc	Section 3.5, Reset Conditions has Incorrect Data
10	273410-001	17	Doc	Section 3.6.2 on page 3-46 has Incorrect Data
11	273410-001	17	Doc	Section 3.2.4.2 on page 3-28 has Incorrect Data
12	273410-001	17	Doc	Section 13.2.2 on page 13-4 has Incorrect Data
13	273410-001	18	Doc	Section 13.2.3 on page 13-5 has Incorrect Data
14	273410-001	18	Doc	Section 15.3.3 on page 15-14 has Incorrect Data
15	273425-007	18	Doc	Section 4.5.2 on page 45 is only correct for the A-1 stepping
16	273410-001	18	Doc	Section 7.5.1 on page 7-11 is only correct for the A-1 stepping

Identification Information

Markings

Topside Markings



Intel® 80312 I/O Companion Chip

Die Details

Part Number	Stepping	QDF/ Spec Number	Voltage (V)	Internal Bus Speed (MHz)	Notes
GC80312	A-1	Q190	3.3	100	Samples - limited testing
GC80312	A-1	SL4Q6	3.3	100	Production
GC80312	A-2	SL57U	3.3	100	Production - Yield improvement, no changes in functionality

Device ID Registers

Device and Stepping	PCI-to-PCI Bridge Unit Revision ID (RIDR - 0x1008)	Address Translation Unit Revision ID Register (ATURID - 0x1208)	Companion Chip Device ID (DEVICEID - 0x1710h)
80312 A-1	0x01	0x01	1887D013
80312 A-2	0x01	0x01	1887D013

NOTE: There are no functionality differences between the A-1 and A-2 steppings of the 80312. Therefore, the Device IDs are the same.

Errata

1. Single-bit and Multi-bit Error Reporting Cannot Be Individually Enabled by ECC Control Register

Problem: The ECC Control Register ECCR is described as having the ability to select multi-bit error and/or single-bit error reporting (see Table 3-23 on page 3-51 of the *Intel® 80312 I/O Companion Chip Developer's Manual*). However, the algorithm does not allow individual enabling; that is, the reporting is either on or off for both multi-bit and single bit error reporting.

Implication: The error reporting selection (enabled or disabled) will apply to both multi-bit and single-bit errors.

Workaround: There is no current workaround. If either the ECCR.0 bit or the ECCR.1 bit is selected for reporting, then both multi-bit and single-bit error reporting are enabled. If neither bit is selected for reporting, then both multi-bit and single-bit error reporting are disabled.

Status: NoFix. See the Table "Summary Table of Changes" on page 7.

Specification Changes

None for this revision of this specification update.

Specification Clarifications

1. ECC is Always Enabled

Problem: ECC is always enabled, therefore do not design an Intel® 80312 I/O companion chip based product without ECC implemented, this will cause severe system errors. On the Intel® 80960RM/RN I/O processors, ECCR.3 can be cleared to disable ECC, but with the 80312 I/O companion chip, ECCR.3 is reserved.

2. 32-bit SDRAM is Not Supported

Problem: The memory controller on the 80312 I/O companion chip supports between 32 and 512 Mbytes of 64-bit SDRAM, but 32-bit SDRAM is not supported. On the 80960RM/RN I/O processors, 32-bit memory was selected by the 32BITMEM_EN# pin (multiplexed on RAD[2]), and by reading a '0' from SDCR.2, this would indicate a 32-bit data bus width. But, for the 80312 I/O companion chip the 32BITMEM_EN# pin does not exist and SDCR.2 is reserved.

3. Non-Battery Backup Systems

Problem: Applications that do not support battery back-up should follow these recommendations:

1. Pull the PWRDELAY pin low through a 1.5K pull-down. Pulling it low will have the effect of keeping the power fail state machine in reset, therefore not allowing the power fail sequence to ever occur.
2. Pull the CKE pins high on the SDRAMs, and leave the SCKE signals on the 80312 as 'no connects'. This will keep the SDRAM from entering a pseudo, self-refresh mode which can cause a lock-up condition on the SDRAM device.

4. IRQISR bit 9 can be read as a ‘1’

Problem: The IRQISR is located at 1700H and bit 9 is listed as ‘reserved’ in the 80312 Developer’s Manual. Bit 9 is actually connected to the C_A0 signal, address 0 for the 80200 interface, and will toggle high and low depending on the address. It defaults to ‘0’ and the bit being set will not cause an interrupt, as it is masked off in hardware so it will not generate an IRQ. However, if you read the IRQISR, the bit can potentially be read as a ‘1’.

This has implications for writing interrupt handlers, where code could be written as:

```
int irqisr_val;

irqisr_val = *MMR_IRQISR;
if (irqisr_val) {  /* sometimes will be true if C_A0 is set, not true if clear */
    handle_irq_interrupt();
}
```

To avoid issues, the code needs to be rewritten to include one additional step to mask out bit 9:

```
int irqisr_val;

irqisr_val = *MMR_IRQISR;
irqisr_val &= 0x00000DFF;  /* masks out everything except the active status
register bits. */
if (irqisr_val) {  /* only will be true if one of the non-reserved bits is set. */
    handle_irq_interrupt();
}
```

5. POCCDR and SOCCDR Functionality

Problem: The Primary Outbound Configuration Cycle Data Register (POCCDR) and Secondary Outbound Configuration Cycle Data Register (SOCCDR) are used to initiate configuration cycles to PCI target devices. On page 5-58, Table 5-26 in the *Intel® 80312 I/O Companion Chip Developer's Manual*, these registers are stated as "Not Available in PCI Configuration Space".

To clarify what this means, if these registers are either read or written via PCI, an unwanted configuration cycle is initiated by the 80312 to the address held in the Primary Outbound Configuration Cycle Address Register (POCCAR) and Secondary Outbound Configuration Cycle Address Register (SOCCAR). An invalid address causes the 80312 to signal a master abort. Only the first 64 bytes in the ATU Configuration Header should be read during configuration. Any thing above 64 bytes up to 256 bytes is defined as device-specific and should not be accessed by a master.

6. 'Bus Hold' Devices on the RAD Bus

Problem: There are five user mode configuration pins (RST_MODE#, ONCE#, RETRY, SPMEM# and 32BITPCI_EN#) and four test mode configuration pins (on RAD8, 7, 4 and 0) that are multiplexed on the RAD[8:0] signals. All these signals have internal pull-ups, so there is no need for external pull-ups. But, if the application requires an active low signal, then an external pull-down needs to be added. The configuration signals are latched on the rising edge of P_RST#. Devices with a 'bus hold' feature (i.e.- CPLD) connected to the RAD bus may pull the RAD[8:0] signals low at the rising edge of P_RST#, causing the 80312 to enter an undesired mode. 80312 designs that use 'bus hold' devices should either turn off the 'bus hold' feature or verify that proper signal levels are being maintained at the rising edge of P_RST#.

7. SREQ64# Functionality

Problem: There is an SREQ64# functionality difference between the A-1 and A-2 steppings of the 80312 I/O companion chip. During the power up sequence, the S_REQ64# signal is sampled by PCI devices on the secondary PCI bus to determine 64-bit or 32-bit PCI operation. On the A-1 stepping, S_REQ64# is deasserted one P_CLK after the deassertion of S_RST# (as stated in the Developer's Manual and Datasheet). On the A-2 stepping, SREQ64# is deasserted ~600ps after the deassertion of S_RST#.

The *PCI Local Bus Specification*, Revision 2.2 has a setup and hold spec for REQ64# with respect to RST#. Even though the Intel Datasheets and Developer's Manuals state that, "S_REQ64# is deasserted one P_CLK after the deassertion of S_RST#", the *PCI Local Bus Specification*, Revision 2.2 states that the RST# to REQ64# hold time is 0-50ns. Since the RST# to REQ64# hold time can be zero, compliant devices should be sampling REQ64# during the REQ64# to RST# setup time which is a minimum of 10 clock cycles. (see pages 128 & 135, table 4-6 and figure 4-11 of the *PCI Local Bus Specification*, Revision 2.2)

The implication of this change is that some 64-bit PCI devices on the secondary PCI bus only works in 32-bit PCI mode. This could be due to using a non-PCI compliant device or because of trace delays between the S_RST# and S_REQ64# signals. Proper functionality should be verified on 80312 A-2 designs. The processor stepping identification is listed on page 10. Also see Documentation Changes #15 and 16 for corrections to the datasheet and manual.

Documentation Changes

1. Section 3.2.4.3 on page 3-29 has incorrect data

Problem: The first sentence incorrectly states, 'When enabled'. ECC is always enabled on the 80312 I/O companion chip, it is not optional.

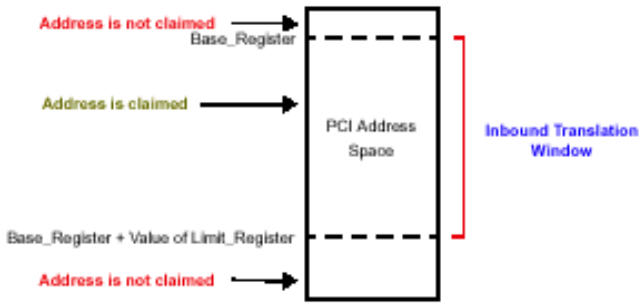
Workaround: Remove 'When enabled'.

Affected Docs: *Intel® 80312 I/O Companion Chip Developer's Manual*

2. Figure 5-3 on page 5-7 has missing text

Problem: The figure shows 'se_Register + Value...'. It should be 'Base_Register + Value...'.

Workaround: Replace Figure 5-3 with the following:



Affected Docs: *Intel® 80312 I/O Companion Chip Developer's Manual*

3. Section 5.7.38 on page 5-100 has incorrect data

Problem: Last paragraph is incorrect. It states, 'Note that bits 4:0, bits 12:11, bit 9 and bit 7 can result...'. Bit 12 is a reserved bit, so it should be removed from this sentence.

Workaround: Change the last paragraph to the following: 'Note that bits 4:0, 11, 9 and 7 can result...'

Affected Docs: *Intel® 80312 I/O Companion Chip Developer's Manual*

4. Section 3.2.3.1 on page 3-13 has incorrect data

Problem: The first sentence states, 'The MCU supports an ECC only memory subsystem ranging from 32 to 528Mbytes.' It should be 512 Mbytes, not 528 Mbytes.

Workaround: Change this sentence to the following: 'The MCU supports an ECC only memory subsystem ranging from 32 to 512 Mbytes.'

Affected Docs: *Intel® 80312 I/O Companion Chip Developer's Manual*

5. Table 3-4 on page 3-9 has incorrect data

Problem: Table 3-4 lists incorrect wait states for the flash bus.

Workaround: Replace Table 3-4 with the following:

Flash Speed	Address-to-Data Wait States	Recovery Wait States
<= 55 ns	8	4
<= 115 ns	12	4
<= 175 ns	20	4

Affected Docs: *Intel® 80312 I/O Companion Chip Developer's Manual*

6. Table 3-13 on page 3-29 has incorrect data

Problem: Syndrome Decoding Error Types and Symptoms are incorrectly stated.

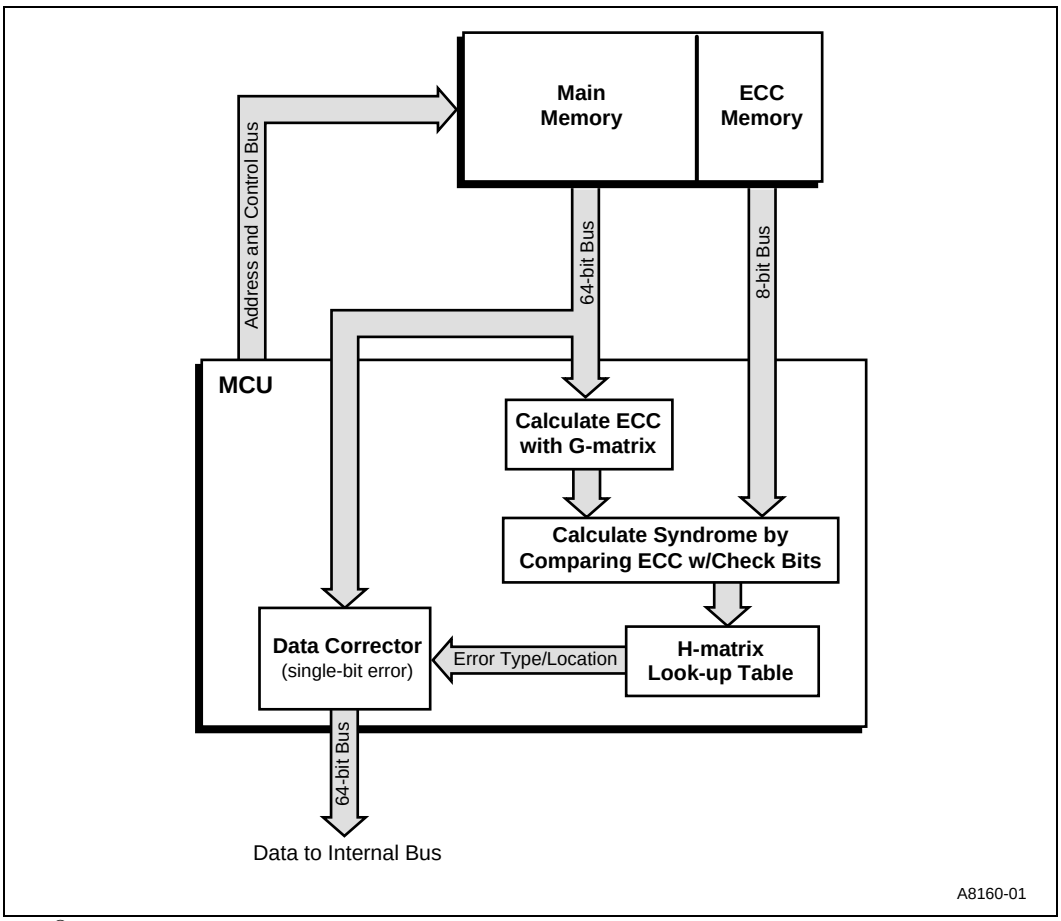
Workaround: Replace Table 3-13 with the following and, add the adjacent paragraph with “new” Figure 3-17:

Table 3-13. Syndrome Decoding

Error Type	Symptom
None	The syndrome is 0000 0000.
Single-Bit	Use the H-Matrix in Figure 3-18 to determine which bit the MCU will invert to fix the error.
Multi-Bit	If the Syndrome does not match an 8-bit value in the H-matrix, the error is uncorrectable

Figure 3-17 shows how the data flows through the ECC hardware for a read transaction.

Figure 3-17. ECC Read Data Flow



Affected Docs: *Intel® 80312 I/O Companion Chip Developer’s Manual*

7. Section 3.2.4.3, First paragraph after Table 3-13 has incorrect data

Problem: First sentence incorrectly states error types for corrected Table 3-13:
...When decoding the syndrome indicates a double-bit or nibble error...

Should read as follows:
...When decoding the syndrome indicates a “multi”-bit error...

Affected Docs: *Intel® 80312 I/O Companion Chip Developer’s Manual*

8. Section 3.2.4.3, First paragraph after “current” Figure 3-17. H-Matrix has incorrect data

Problem: First sentence incorrectly states error types for corrected Table 3-13:
...When error reporting is enabled in the ECCR and the MCU detects a nibble, single-bit, or double-bit error...

Should read as follows:
...When error reporting is enabled in the ECCR and the MCU detects a single-bit or “multi”-bit error...

Affected Docs: *Intel® 80312 I/O Companion Chip Developer’s Manual*

9. Section 3.5, Reset Conditions has Incorrect Data

Problem: The last sentence in the first paragraph incorrectly states:
Reads issued prior to a write to the same address results in an ECC error ***(if enabled)*** and ***is*** not recommended.

This should state:
Reads issued prior to a write to the same address results in an ECC error and *are* not recommended.

10. Section 3.6.2 on page 3-46 has Incorrect Data

Problem: The second sentence in the first paragraph incorrectly states, “The SDCR specifies the drive strength for the MCU pins, the bus width, and power failure handling.”

Workaround: Remove “,the bus width, and power failure handling”. This sentence should read as follows: “The SDCR specifies the drive strength for the MCU pins.”

11. Section 3.2.4.2 on page 3-28 has Incorrect Data

Problem: The first sentence incorrectly states, “When the internal bus master writes less than the data bus width programmed in the SDCR, then…”

Workaround: Remove “programmed in the SDCR”. This sentence should read as follows: “When the internal bus master writes less than the data bus width, then the MCU translates the write transaction into a read-modify-write transaction.”

12. Section 13.2.2 on page 13-4 has Incorrect Data

Problem: The first sentence is incorrect. It states, “The GPIO Input Data Register reflects the state of the appropriate IRQ bus pin following the deassertion of P_RST#.” This register does not reflect the state of the IRQ pin.

Workaround: Sentence should read as, “The GPIO Input Data Register reflects the state of the appropriate GPIO pins following the deassertion of P_RST#.”

13. Section 13.2.3 on page 13-5 has Incorrect Data

Problem: The first sentence is incorrect. It states, “The GPIO Output Data Register is driven on a per bit basis on the appropriate IRQ bus pin following the deassertion of P_RST#...” This register does not drive the IRQ pin.

Workaround: Sentence should read as, “The GPIO Output Data Register is driven on a per bit basis on the appropriate GPIO pins following the deassertion of P_RST#...”

14. Section 15.3.3 on page 15-14 has Incorrect Data

Problem: The last sentence in the second paragraph is incorrect. It states, “…a valid input clock (S_CLK) and...” The input clock is from P_CLK, not S_CLK.

Workaround: Sentence should read as, “To ensure that all internal logic has stabilized in the reset state, a valid input clock (P_CLK) and Vcc must be present and stable for a specified time before P_RST# can be deasserted.”

15. Section 4.5.2 on page 45 is only correct for the A-1 stepping

Problem: The second sentence in Note 7 states, ‘S_REQ64# is deasserted one P_CLK after the deassertion of S_RST#’. This statement is not correct for the A-2 stepping of the 80312 I/O companion chip.

Workaround: This statement is only correct for the A-1 stepping of the 80312. See specification clarification #7 for A-2 stepping functionality.

Affected Docs: *Intel® 80312 I/O Companion Chip Datasheet*

16. Section 7.5.1 on page 7-11 is only correct for the A-1 stepping

Problem: The last sentence states, ‘S_REQ64# remains valid for one clock (P_CLK) after S_RST# deasserts’. This statement is not correct for the A-2 stepping of the 80312 I/O companion chip.

Workaround: This statement is only correct for the A-1 steppings of the 80312. See specification clarification #7 for A-2 stepping functionality.

Affected Docs: *Intel® 80312 I/O Companion Chip Developer’s Manual*