
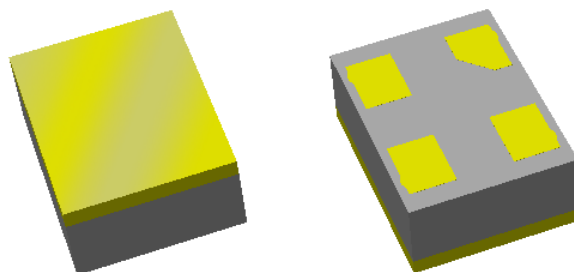


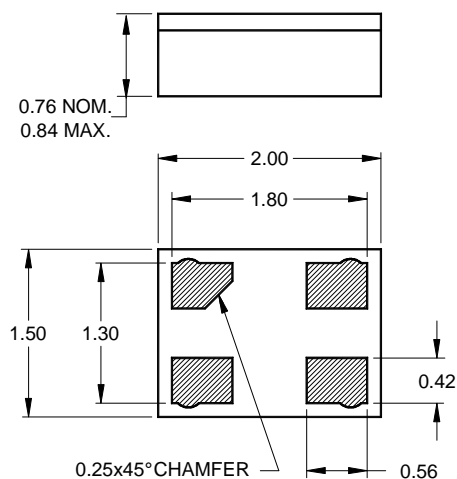
Features

- For GPS applications
- Usable bandwidth 2 MHz
- Very Low loss
- Single-ended operation at 50 Ω
- No impedance matching required for operation at 50 Ω
- Single-ended operation
- Ceramic Chip Scale Package (CSP)
- Hermetic
- Suitable for Automotive applications - Compliant to the AEC-Q200 reliability standard
- Manufacturing facilities are certified with ISO/TS 16949:2002
- RoHS compliant (2002/95/EC), Pb-free 



Package

Surface Mount 2.00 x 1.50 x 0.76 mm
CSP-8E

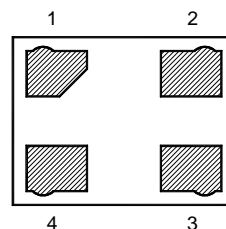


Dimensions shown are nominal in millimeters
All tolerances are ± 0.10 mm

Body: Al_2O_3 ceramic
Lid: Kovar or Alloy 42, Au over Ni plated
Terminations: Au plating 0.5 - 1.0 μ m,
over a 2 - 6 μ m Ni plating

Pin Configuration

Bottom View



| Pin No. | Description |
|---------|-------------|
| 1 | Input |
| 3 | Output |
| 2,4 | Case ground |

Electrical Specifications ⁽¹⁾

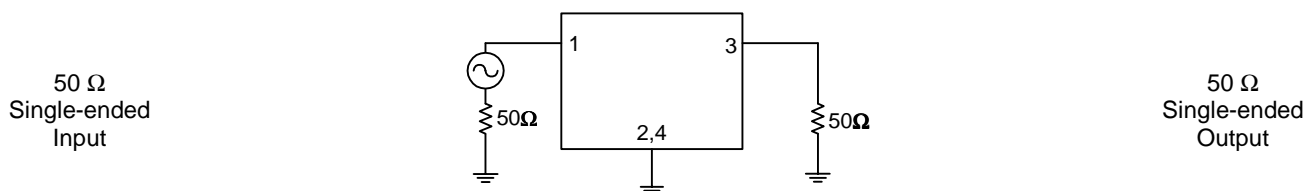
Operating Temperature Range: ⁽²⁾ -40 to +85 °C

| Parameter ⁽³⁾ | Minimum | Typical ⁽⁴⁾ | Maximum | Unit |
|--|---------|------------------------|---------|--------|
| Center Frequency | - | 1575.42 | - | MHz |
| Insertion Loss 1574.42 - 1576.42 MHz | - | 1.25 | 1.6 | dB |
| Absolute Attenuation | | | | |
| 0 - 1475 MHz | 30 | 36 | - | dB |
| 1475 - 1527.42 MHz | 30 | 33 | - | dB |
| 1623.42 - 1750 MHz | 30 | 37 | - | dB |
| 1750 - 1800 MHz | 32 | 36 | - | dB |
| 1800 - 1990 MHz | 32 | 38 | - | dB |
| 1990 - 3000 MHz | 30 | 40 | - | dB |
| 3000 - 4000 MHz | 20 | 25 | - | dB |
| 4000 - 6000 MHz | 15 | 17 | - | dB |
| Passband Variation 1574.42 - 1576.42 MHz | - | 0.25 | 0.5 | dB p-p |
| Input/Output Return Loss 1574.42 - 1576.42 MHz | 10 | 18 | - | dB |
| Source Impedance ⁽⁵⁾ | - | 50 | - | Ω |
| Load Impedance ⁽⁵⁾ | - | 50 | - | Ω |

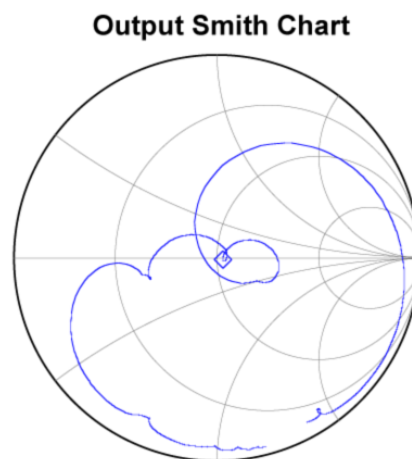
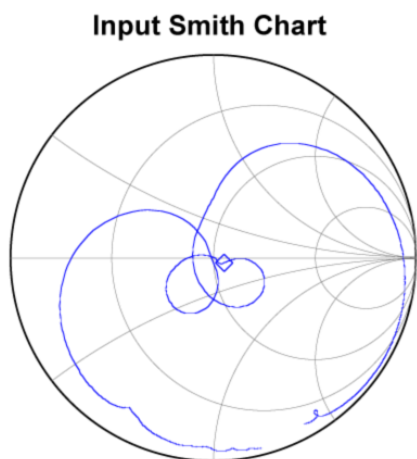
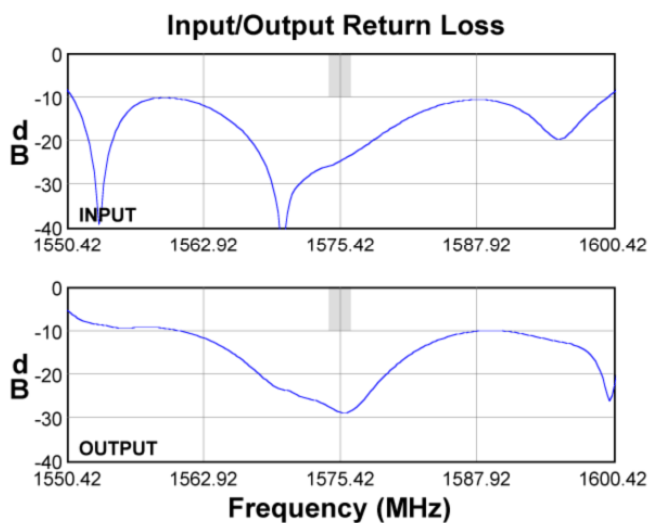
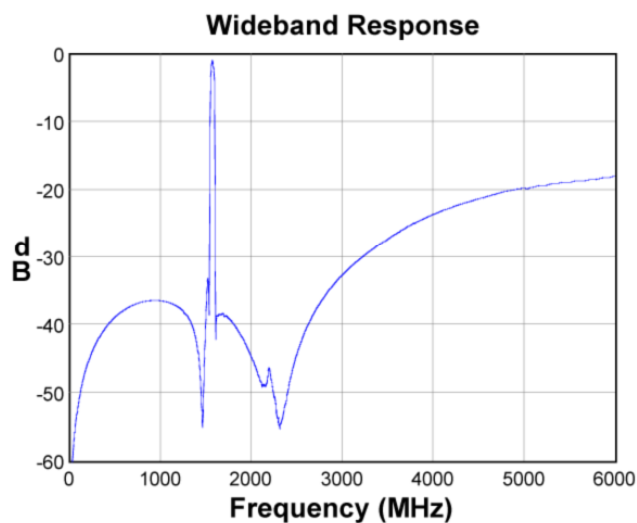
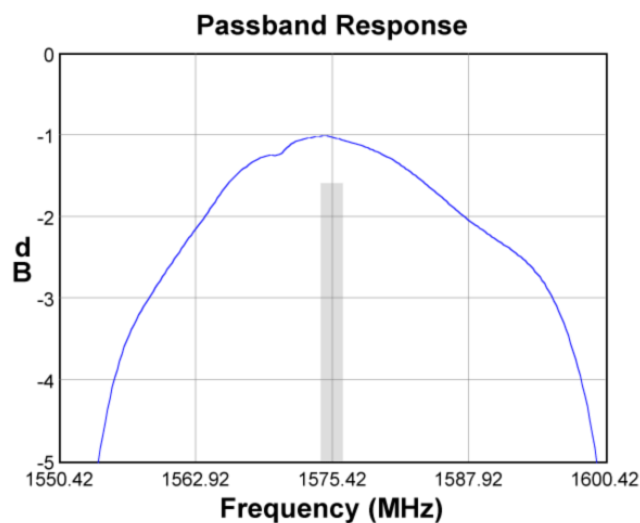
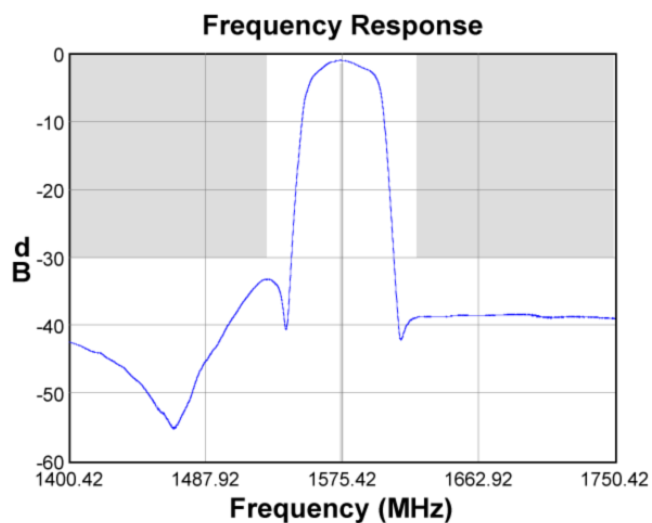
Notes:

1. All specifications are based on TriQuint test circuit shown below
2. In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature
3. Electrical margin has been built into the design to account for the variations due to temperature drift and manufacturing tolerances
4. Typical values are based on average measurements at room temperature
5. This is the optimum impedance in order to achieve the performance shown

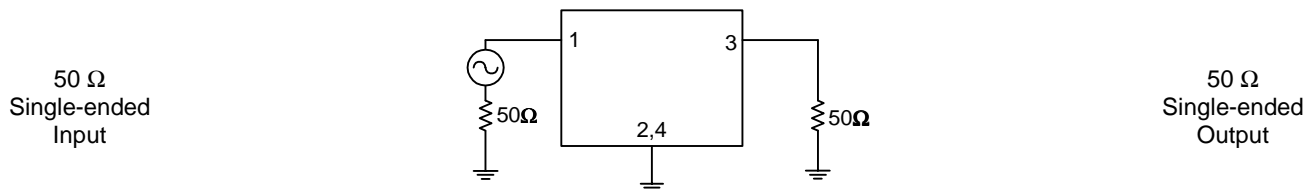
Test Circuit:



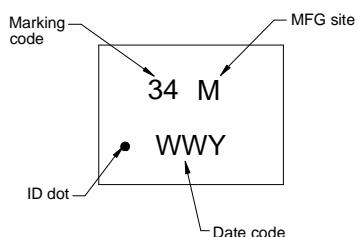
Typical Performance (at +25°C)



Matching Schematics

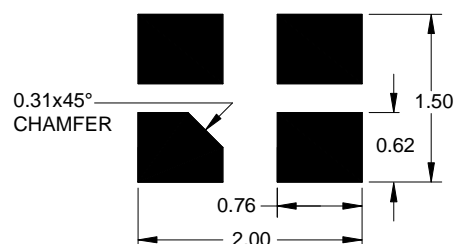


Marking



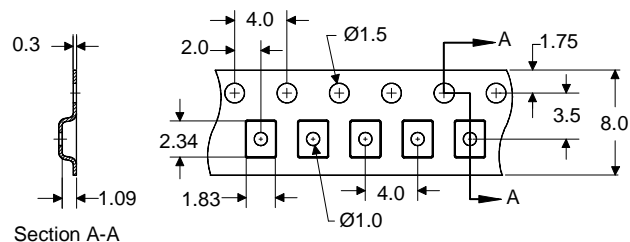
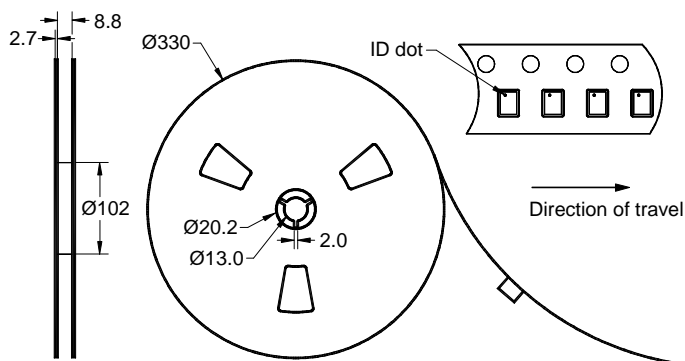
The date code consists of: WW = 2 digit week,
Y = last digit of year, M = manufacturing site code

PCB Footprint



This footprint represents a recommendation only
Dimensions shown are nominal in millimeters

Tape and Reel




Dimensions shown are nominal in millimeters
Packaging quantity: 10000 units/reel

Maximum Ratings


| Parameter | Symbol | Minimum | Maximum | Unit |
|-----------------------------|------------------|---------|---------|------|
| Operating Temperature Range | T | -40 | +85 | °C |
| Storage Temperature Range | T _{stg} | -55 | +125 | °C |

Important Notes

Warnings

- Electrostatic Sensitive Device (ESD) 
- Avoid ultrasonic exposure

RoHS Compliance

- This product complies with EU directive 2002/95/EC (RoHS) 

Solderability

- Compatible with JEDEC J-STD-020C **Pb-free** process, **260°C** peak reflow temperature ([see soldering profile](#))

Links to Additional Technical Information

[PCB Layout Tips](#)

[Qualification Flowchart](#)

[Soldering Profile](#)

[S-Parameters](#)

[RoHS Information](#)

[Other Technical Information](#)

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[Representatives or distributors](#)