



STP22NE10L

N - CHANNEL 100V - 0.07 Ω - 22A TO-220
STripFET™ POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STP22NE10L	100 V	< 0.085 Ω	22 A

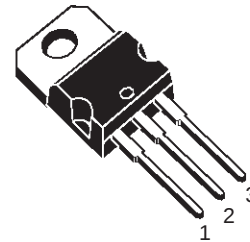
- TYPICAL R_{DS(on)} = 0.07 Ω
- LOW THRESHOLD DRIVE
- LOGIC LEVEL DEVICE

DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

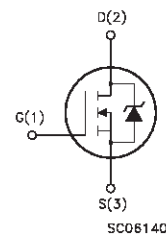
APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- DC-DC & DC-AC CONVERTERS



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	100	V
V _{DGR}	Drain- gate Voltage (R _{GS} = 20 k Ω)	100	V
V _{GS}	Gate-source Voltage	± 20	V
I _D	Drain Current (continuous) at T _c = 25 °C	22	A
I _D	Drain Current (continuous) at T _c = 100 °C	14	A
I _{DM} (●)	Drain Current (pulsed)	88	A
P _{tot}	Total Dissipation at T _c = 25 °C	90	W
	Derating Factor	0.6	W/°C
E _{AS} (1)	Single Pulse Avalanche Energy	250	mJ
T _{stg}	Storage Temperature	-65 to 175	°C
T _j	Max. Operating Junction Temperature	175	°C

(●) Pulse width limited by safe operating area

(1) starting T_j = 25 °C, I_D = 22A, V_{DD} = 50V

STP22NE10L

THERMAL DATA

$R_{thj-case}$	Thermal Resistance Junction-case	Max	1.67	$^{\circ}C/W$
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	62.5	$^{\circ}C/W$
T_l	Maximum Lead Temperature For Soldering Purpose		300	$^{\circ}C$

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250 \mu A$ $V_{GS} = 0$	100			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ $T_c = 125^{\circ}C$			1 10	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20 V$			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250 \mu A$	1	1.6	2.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10 V$ $I_D = 15 A$ $V_{GS} = 5 V$ $I_D = 15 A$		0.07 0.085	0.085 0.1	Ω Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10 V$	22			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (*)$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 15 A$		19		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25 V$ $f = 1 MHz$ $V_{GS} = 0$		1750 165 45		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 50\text{ V}$ $I_D = 8\text{ A}$		40		ns
t_r	Rise Time	$R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, see fig. 3)		80		ns
Q_g	Total Gate Charge	$V_{DD} = 80\text{ V}$ $I_D = 16\text{ A}$ $V_{GS} = 10\text{ V}$		24	31	nC
Q_{gs}	Gate-Source Charge			55		nC
Q_{gd}	Gate-Drain Charge			11		nC

SWITCHING OFF

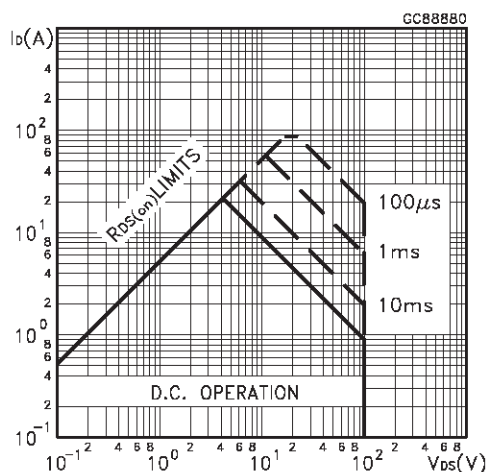
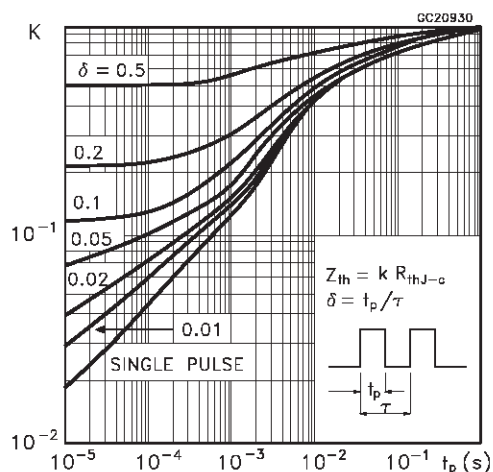
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off Delay Time	$V_{DD} = 50\text{ V}$ $I_D = 8\text{ A}$		45		ns
t_f	Fall Time	$R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, see fig. 3)		12		ns
$t_{d(off)}$	Off-voltage Rise Time	$V_{clamp} = 80\text{ V}$ $I_D = 16\text{ A}$		12		ns
t_f	Fall Time	$R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$		17		ns
t_c	Cross-over Time	(Inductive Load, see fig. 5)		35		ns

SOURCE DRAIN DIODE

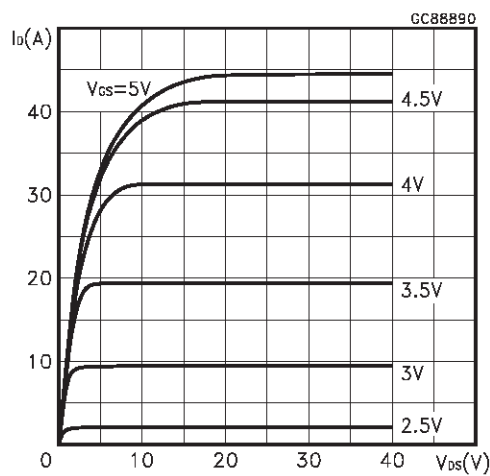
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				22	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				88	A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 16\text{ A}$ $V_{GS} = 0$			1.5	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 16\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 40\text{ V}$ $T_J = 150\text{ }^\circ\text{C}$ (see test circuit, fig. 5)		100		ns
Q_{rr}	Reverse Recovery Charge			300		nC
I_{RRM}	Reverse Recovery Current			6		A

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

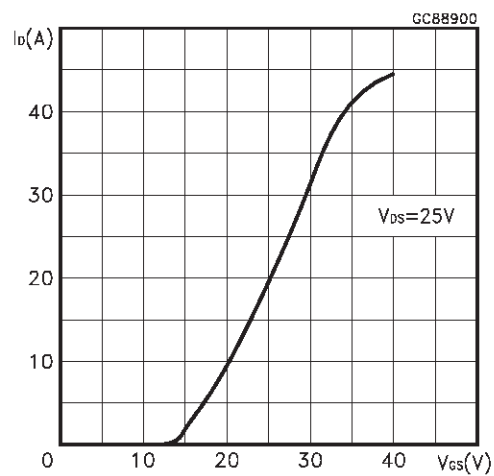
(•) Pulse width limited by safe operating area

Safe Operating Area**Thermal Impedance**

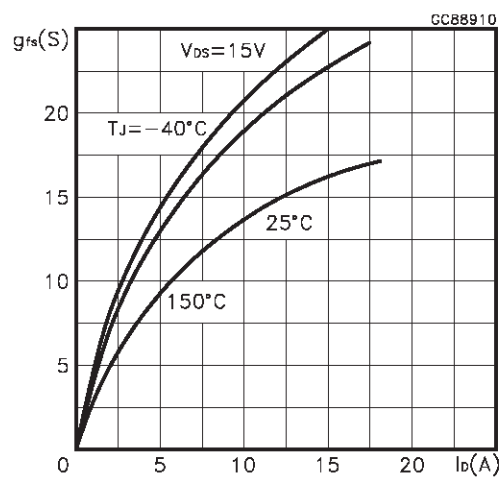
Output Characteristics



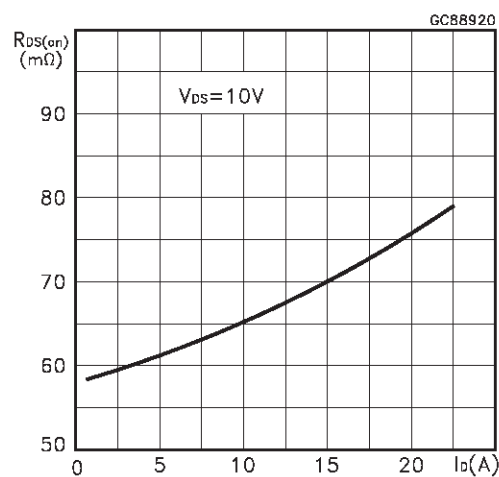
Transfer Characteristics



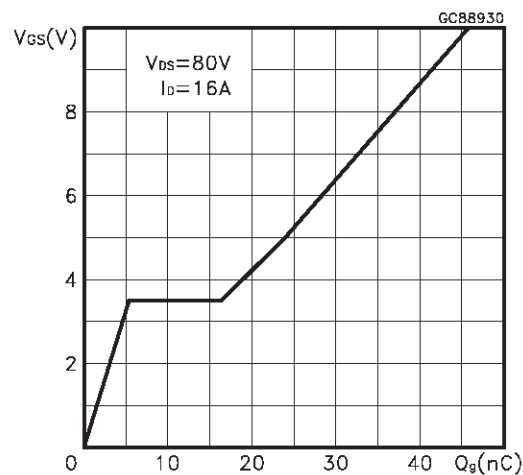
Transconductance



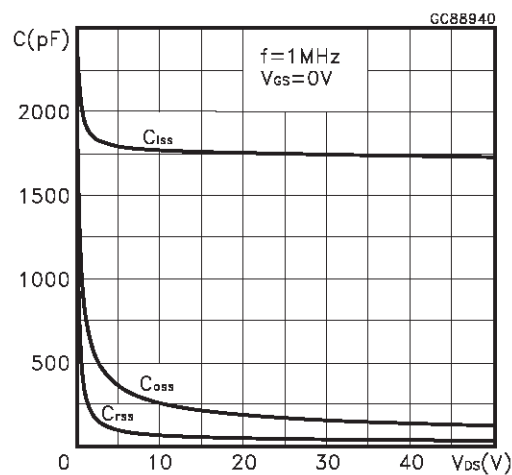
Static Drain-source On Resistance



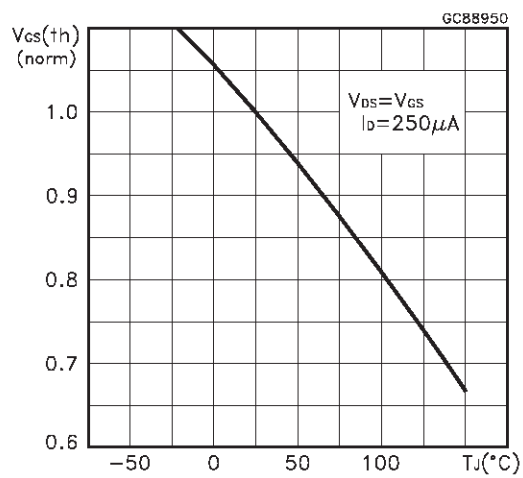
Gate Charge vs Gate-source Voltage



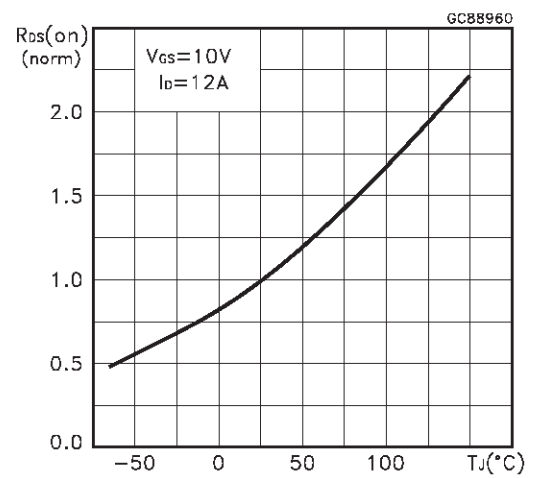
Capacitance Variations



Normalized Gate Threshold Voltage vs Temperature



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

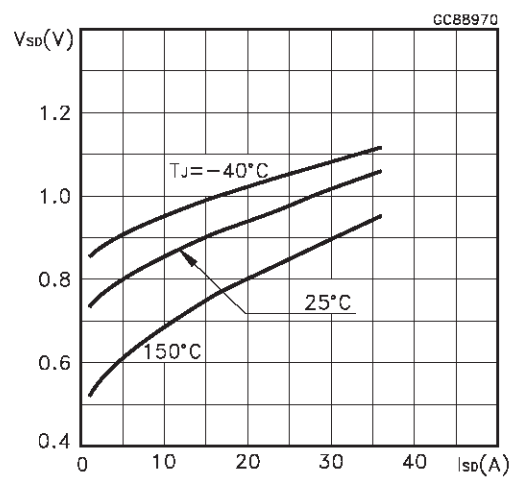


Fig. 2: Unclamped Inductive Waveform

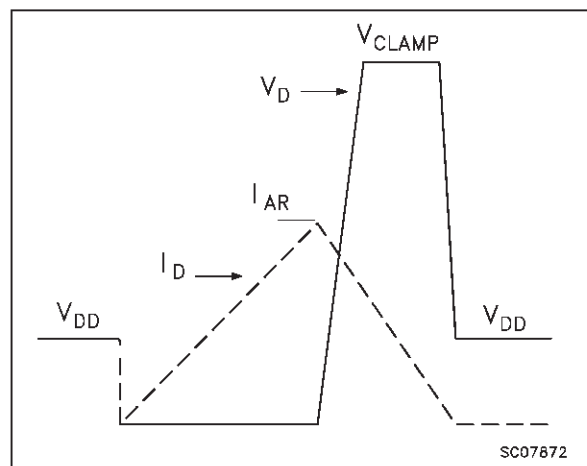
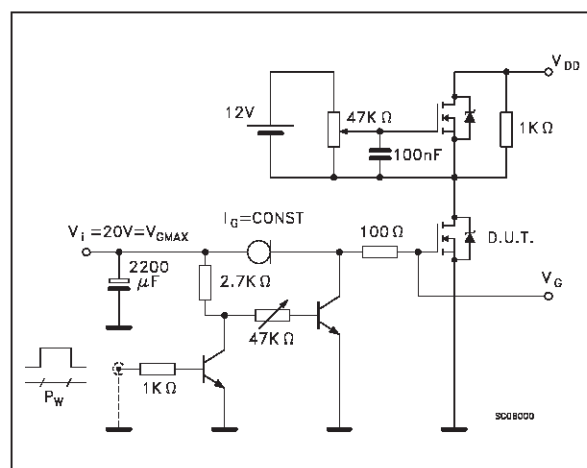
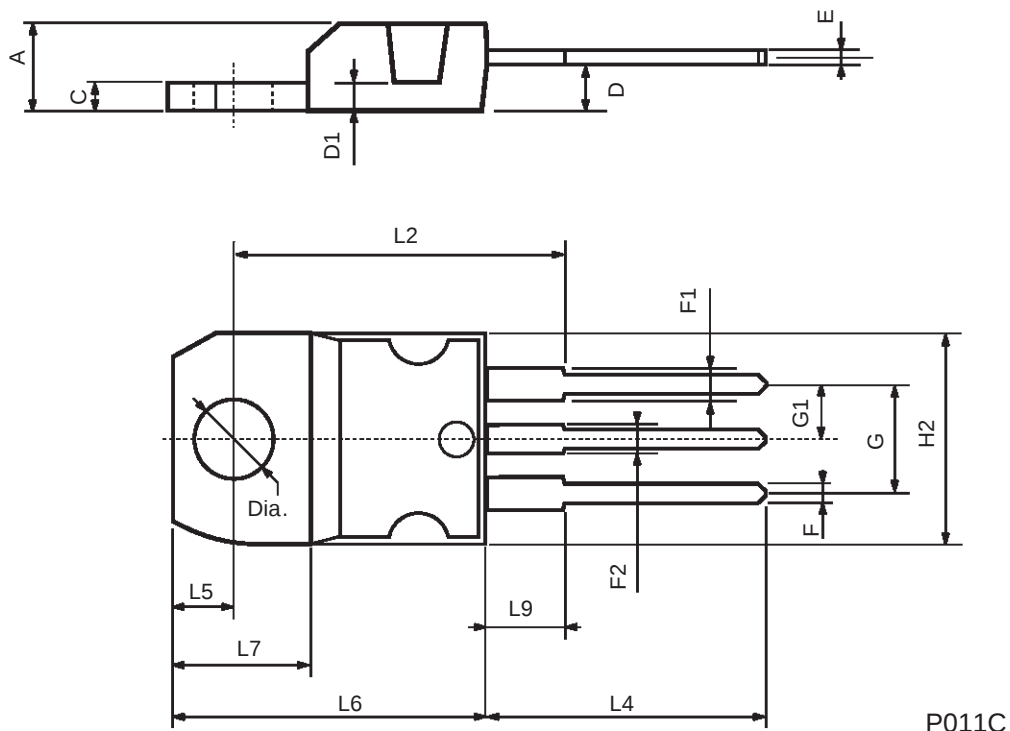


Fig. 4: Gate Charge test Circuit



TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



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