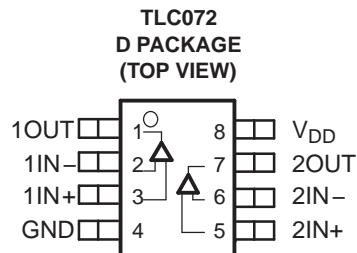


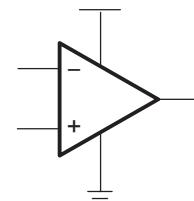
WIDE-BANDWIDTH HIGH-OUTPUT-DRIVE SINGLE-SUPPLY OPERATIONAL AMPLIFIER

FEATURES

- Qualified for Automotive Applications
- Wide Bandwidth . . . 10 MHz
- High-Output Drive
 - I_{OH} . . . 57 mA at V_{DD} – 1.5 V
 - I_{OL} . . . 55 mA at 0.5 V
- High Slew Rate
 - SR_+ . . . 16 V/ μ s
 - SR_- . . . 19 V/ μ s
- Wide Supply Range . . . 4.5 V to 16 V
- Supply Current . . . 1.9 mA/Channel
- Ultralow Power Shutdown Mode I_{DD} . . . 125 mA/Channel
- Low Input Noise Voltage . . . 7 nV/ $\sqrt{\text{Hz}}$
- Input Offset Voltage . . . 60 μ V
- Small 8-Pin SOIC Package



Operational Amplifier



DESCRIPTION/ORDERING INFORMATION

The first members of TI's new BiMOS general-purpose operational amplifier family are the TLC07x. The BiMOS family concept is simple: provide an upgrade path for BiFET users who are moving away from dual-supply to single-supply systems and demand higher AC and dc performance. With performance rated from 4.5 V to 16 V across commercial (0°C to 70°C) and an extended industrial temperature range (-40°C to 125°C), BiMOS suits a wide range of audio, automotive, industrial and instrumentation applications. Familiar features like offset nulling pins enable higher levels of performance in a variety of applications.

Developed in TI's patented LBC3 BiCMOS process, the new BiMOS amplifiers combine a very high input impedance low-noise CMOS front end with a high-drive bipolar output stage, thus providing the optimum performance features of both. AC performance improvements over the TL07x BiFET predecessors include a bandwidth of 10 MHz (an increase of 300%) and voltage noise of 7 nV/ $\sqrt{\text{Hz}}$ (an improvement of 60%). DC improvements include a factor of 4 reduction in input offset voltage down to 1.5 mV (maximum) in the standard grade, and a power supply rejection improvement of greater than 40 dB to 130 dB. Added to this list of impressive features is the ability to drive ± 50 -mA loads comfortably from an ultrasmall-footprint MSOP PowerPAD™ package, which positions the TLC07x as the ideal high-performance general-purpose operational amplifier family.

ORDERING INFORMATION⁽¹⁾

T_A	PACKAGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOIC – D	Reel of 2500	TC072Q

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



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PowerPAD is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

V_{DD}	Supply voltage ⁽²⁾	17 V
V_{ID}	Differential input voltage range	$\pm V_{DD}$
	Continuous total power dissipation	See Dissipation Ratings Table
T_A	Operating free-air temperature range	–40°C to 125°C
T_J	Maximum virtual-junction temperature	150°C
T_{stg}	Storage temperature range	–65°C to 150°C
T_{lead}	Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential voltages, are with respect to GND.

DISSIPATION RATINGS

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	$T_A \leq 25^\circ\text{C}$ POWER RATING
D	38.3	176	710 mW

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{DD}	Supply voltage	Single supply	4.5	16
		Split supply	±2.25	±8
V_{ICR}	Common-mode input voltage	+0.5	$V_{DD} - 0.8$	V
T_A	Operating free-air temperature	–40	125	°C

ELECTRICAL CHARACTERISTICS

$V_{DD} = 5$ V, at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^{(1)}$	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD} = 5$ V, $V_{IC} = 2.5$ V, $V_O = 2.5$ V, $R_S = 50 \Omega$	25°C	390	1900	3000	μ V
			Full range			3000	
α_{VIO}	Temperature coefficient of input offset voltage	$V_{DD} = 5$ V, $V_{IC} = 2.5$ V, $V_O = 2.5$ V, $R_S = 50 \Omega$	25°C	1.2			μ V/°C
I_{IO}	Input offset current	$V_{DD} = 5$ V, $V_{IC} = 2.5$ V, $V_O = 2.5$ V, $R_S = 50 \Omega$	25°C	0.7	50	700	pA
			Full range			700	
I_{IB}	Input bias current	$V_{DD} = 5$ V, $V_{IC} = 2.5$ V, $V_O = 2.5$ V, $R_S = 50 \Omega$	25°C	1.5	50	700	pA
			Full range			700	
V_{ICR}	Common-mode input voltage	$R_S = 50 \Omega$	25°C	0.5 to 4.2			V
			Full range	0.5 to 4.2			
V_{OH}	High-level output voltage	$V_{IC} = 2.5$ V	$I_{OH} = -1$ mA	25°C	4.1	4.3	V
				Full range	3.9		
			$I_{OH} = -20$ mA	25°C	3.7	4	
				Full range	3.5		
			$I_{OH} = -35$ mA	25°C	3.4	3.8	
				Full range	3.2		
V_{OL}	Low-level output voltage	$V_{IC} = 2.5$ V	$I_{OL} = 1$ mA	25°C	0.18	0.25	V
				Full range	0.35		
			$I_{OL} = 20$ mA	25°C	0.35	0.39	
				Full range	0.45		
			$I_{OL} = 35$ mA	25°C	0.43	0.55	
				Full range	0.7		
I_{OS}	Short-circuit output current		$I_{OL} = 50$ mA	25°C	0.48	0.63	mA
				Full range	0.7		
			Sourcing	25°C	100		
				25°C	100		
			Sinking	25°C	57		
				25°C	55		
I_O	Output current	$V_{OH} = 1.5$ V from positive rail $V_{OL} = 0.5$ V from negative rail	25°C	100	120		mA
			Full range	100			
A_{VD}	Large-signal differential voltage amplification	$V_{O(PP)} = 3$ V, $R_L = 10$ k Ω	25°C	100	120		dB
			Full range	100			
$r_{i(d)}$	Differential input resistance		25°C	1000			$\text{G}\Omega$
C_{IC}	Common-mode input capacitance	$f = 10$ kHz	25°C	22.9			pF
Z_O	Closed-loop output impedance	$f = 10$ kHz, $A_V = 10$	25°C	0.25			Ω
$CMRR$	Common-mode rejection ratio	$V_{IC} = 1$ to 3 V, $R_S = 50 \Omega$	25°C	80	95		dB
			Full range	80			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.5$ V to 16 V, $V_{IC} = V_{DD}/2$, No load	25°C	80	100		dB
			Full range	80			
I_{DD}	Supply current (per channel)	$V_O = 2.5$ V, No load	25°C	1.9	2.5		mA
			Full range	3.5			

(1) Full range is –40°C to 125°C.

OPERATING CHARACTERISTICS

$V_{DD} = 5$ V, at specified free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^{(1)}$	MIN	TYP	MAX	UNIT
SR+	Positive slew rate at unity gain $V_{O(PP)} = 0.8$ V, $C_L = 50$ pF, $R_L = 10$ k Ω	25°C	10	16		V/ μ s
		Full range	9.5			
SR-	Negative slew rate at unity gain $V_{O(PP)} = 0.8$ V, $C_L = 50$ pF, $R_L = 10$ k Ω	25°C	12.5	19		V/ μ s
		Full range	10			
V_n	Equivalent input noise voltage $f = 100$ Hz	25°C		12		nV/ $\sqrt{\text{Hz}}$
				7		
I_n	Equivalent input noise current $f = 1$ kHz	25°C		0.6		fA/ $\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise $V_{O(PP)} = 3$ V, $R_L = 10$ k Ω and 250 Ω , $f = 1$ kHz	25°C		0.002		%
				0.012		
				0.085		
GBWP	Gain-bandwidth product $f = 10$ kHz, $R_L = 10$ k Ω	25°C		10		MHz
t_s	Settling time $V_{(STEP)PP} = 1$ V, $A_V = -1$, $C_L = 10$ pF, $R_L = 10$ k Ω	25°C	0.1%		0.18	μ s
			0.01%		0.39	
			0.1%		0.18	
			0.01%		0.39	
ϕ_m	Phase margin $R_L = 10$ k Ω	25°C	$C_L = 50$ pF		32	°
			$C_L = 0$ pF		40	
G_m	Gain margin $R_L = 10$ k Ω	25°C	$C_L = 50$ pF		2.2	dB
			$C_L = 0$ pF		3.3	

(1) Full range is -40 °C to 125 °C.

ELECTRICAL CHARACTERISTICS

$V_{DD} = 12$ V, at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^{(1)}$	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD} = 12$ V, $V_{IC} = 6$ V, $V_O = 6$ V, $R_S = 50$ Ω	25°C	390	1900	3000	μ V
			Full range			3000	
α_{VIO}	Temperature coefficient of input offset voltage	$V_{DD} = 12$ V, $V_{IC} = 6$ V, $V_O = 6$ V, $R_S = 50$ Ω	25°C	1.2			μ V/°C
I_{IO}	Input offset current	$V_{DD} = 12$ V, $V_{IC} = 6$ V, $V_O = 6$ V, $R_S = 50$ Ω	25°C	0.7	50	700	pA
			Full range			700	
I_{IB}	Input bias current	$V_{DD} = 12$ V, $V_{IC} = 6$ V, $V_O = 6$ V, $R_S = 50$ Ω	25°C	1.5	50	700	pA
			Full range			700	
V_{ICR}	Common-mode input voltage	$R_S = 50$ Ω	25°C	0.5 to 11.2			V
			Full range	0.5 to 11.2			
V_{OH}	High-level output voltage	$V_{IC} = 6$ V	$I_{OH} = -1$ mA	25°C	11.1	11.2	V
				Full range	11		
			$I_{OH} = -20$ mA	25°C	10.8	109	
				Full range	10.7		
			$I_{OH} = -35$ mA	25°C	10.6	10.7	
				Full range	10.3		
V_{OL}	Low-level output voltage	$V_{IC} = 6$ V	$I_{OL} = 1$ mA	25°C	0.17	0.25	V
				Full range		0.35	
			$I_{OL} = 20$ mA	25°C	0.35	0.45	
				Full range		0.5	
			$I_{OL} = 35$ mA	25°C	0.4	0.52	
				Full range		0.6	
I_{OS}	Short-circuit output current		$I_{OL} = 50$ mA	25°C	0.45	0.6	mA
				Full range		0.65	
			Sourcing	25°C	150		
				25°C	150		
			Sinking	25°C	57		
				25°C	55		
I_O	Output current	$V_{OH} = 1.5$ V from positive rail $V_{OL} = 0.5$ V from negative rail	25°C	120	140		mA
			Full range	120			
A_{VD}	Large-signal differential voltage amplification	$V_{O(PP)} = 8$ V, $R_L = 10$ k Ω	25°C	120	140		dB
			Full range	120			
$r_{i(d)}$	Differential input resistance		25°C	1000			$\text{G}\Omega$
C_{IC}	Common-mode input capacitance	$f = 10$ kHz	25°C	21.6			pF
Z_O	Closed-loop output impedance	$f = 10$ kHz, $A_V = 10$	25°C	0.25			Ω
$CMRR$	Common-mode rejection ratio	$V_{IC} = 1$ to 10 V, $R_S = 50$ Ω	25°C	80	100		dB
			Full range	80			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.5$ V to 16 V, $V_{IC} = V_{DD}/2$, No load	25°C	80	100		dB
			Full range	80			
I_{DD}	Supply current (per channel)	$V_O = 7.5$ V, No load	25°C	2.1	2.9		mA
			Full range			3.5	

(1) Full range is –40°C to 125°C.

OPERATING CHARACTERISTICS

$V_{DD} = 12$ V, at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^{(1)}$	MIN	TYP	MAX	UNIT
SR+	Positive slew rate at unity gain	$V_{O(PP)} = 2$ V, $C_L = 50$ pF, $R_L = 10$ k Ω	25°C	10	16		V/ μ s
			Full range	9.5			
SR-	Negative slew rate at unity gain	$V_{O(PP)} = 2$ V, $C_L = 50$ pF, $R_L = 10$ k Ω	25°C	12.5	19		V/ μ s
			Full range	10			
V_n	Equivalent input noise voltage	$f = 100$ Hz	25°C	12			nV/ $\sqrt{\text{Hz}}$
		$f = 1$ kHz		7			
I_n	Equivalent input noise current	$f = 1$ kHz	25°C	0.6			fA/ $\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise	$V_{O(PP)} = 8$ V, $R_L = 10$ k Ω and 250 Ω , $f = 1$ kHz	$A_V = 1$	25°C	0.002		%
			$A_V = 10$		0.005		
			$A_V = 100$		0.022		
GBWP	Gain-bandwidth product	$f = 10$ kHz, $R_L = 10$ k Ω	25°C	10			MHz
t_s	Settling time	$V_{(STEP)PP} = 1$ V, $A_V = -1$, $C_L = 10$ pF, $R_L = 10$ k Ω	0.1%	25°C	0.17		μ s
			0.01%		0.22		
		$V_{(STEP)PP} = 1$ V, $A_V = -1$, $C_L = 47$ pF, $R_L = 10$ k Ω	0.1%		0.17		
			0.01%		0.29		
ϕ_m	Phase margin	$R_L = 10$ k Ω	$C_L = 50$ pF	25°C	37		°
			$C_L = 0$ pF		42		
G_m	Gain margin	$R_L = 10$ k Ω	$C_L = 50$ pF	25°C	3.1		dB
			$C_L = 0$ pF		4		

(1) Full range is -40 °C to 125 °C.

TYPICAL CHARACTERISTICS

Table 1. Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	vs Common-mode input voltage	1, 2
I_{IO}	Input offset current	vs Free-air temperature	3, 4
I_{IB}	Input bias current	vs Free-air temperature	3, 4
V_{OH}	High-level output voltage	vs High-level output current	5, 7
V_{OL}	Low-level output voltage	vs Low-level output current	6, 8
Z_o	Output impedance	vs Frequency	9
I_{DD}	Supply current	vs Supply voltage	10
PSRR	Power supply rejection ratio	vs Frequency	11
CMRR	Common-mode rejection ratio	vs Frequency	12
V_n	Equivalent input noise voltage	vs Frequency	13
$V_{O(PP)}$	Peak-to-peak output voltage	vs Frequency	14, 15
	Crosstalk	vs Frequency	16
	Differential voltage gain	vs Frequency	17, 18
	Phase	vs Frequency	17, 18
ϕ_m	Phase margin	vs Load capacitance	19, 20
	Gain margin	vs Load capacitance	21, 22
	Gain-bandwidth product	vs Supply voltage	23
SR	Slew rate	vs Supply voltage	24
		vs Free-air temperature	25, 26
THD + N	Total harmonic distortion plus noise	vs Frequency	27, 28
		vs Peak-to-peak output voltage	29, 30
	Large-signal follower pulse response		31, 32
	Small-signal follower pulse response		33
	Large-signal inverting pulse response		34, 35
	Small-signal inverting pulse response		36

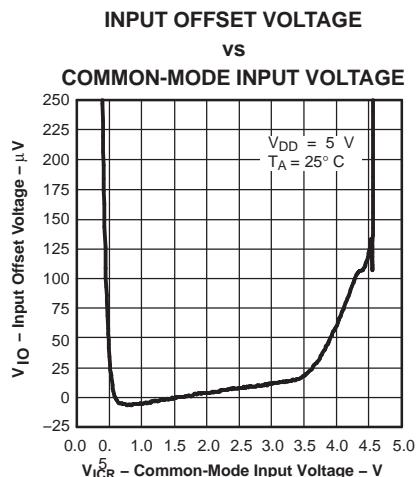


Figure 1.
INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

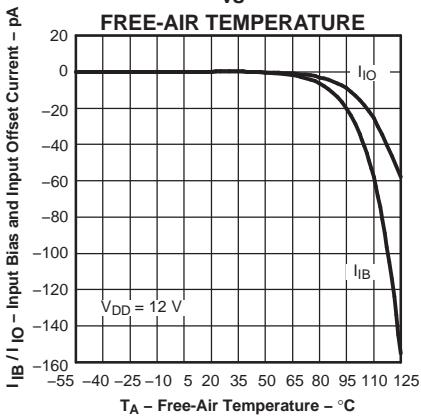


Figure 4.
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

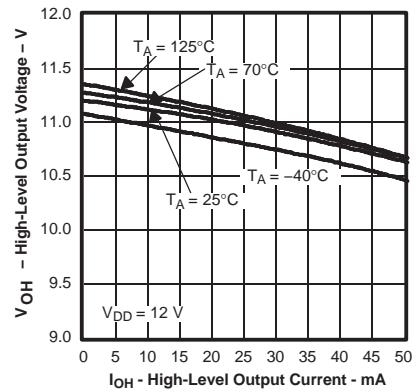


Figure 7.

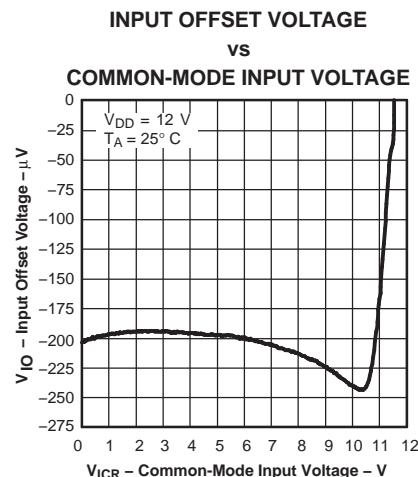


Figure 2.
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

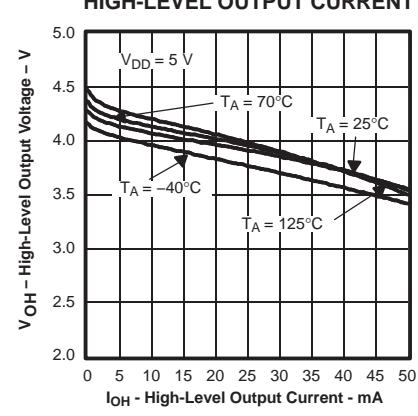


Figure 5.
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

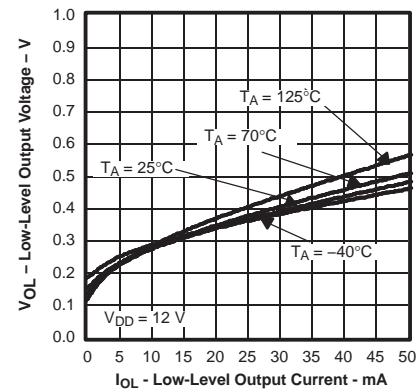


Figure 8.

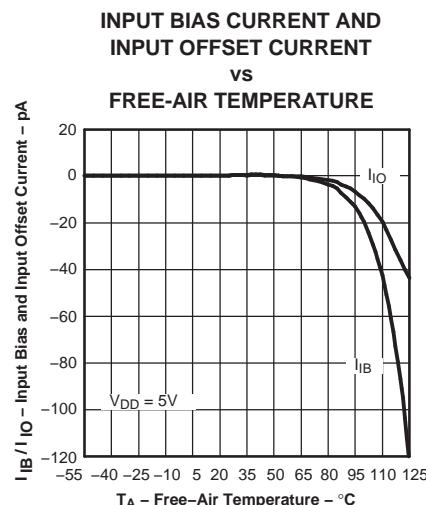


Figure 3.
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

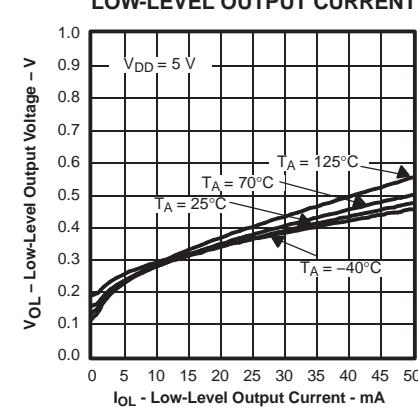


Figure 6.
OUTPUT IMPEDANCE
vs
FREQUENCY

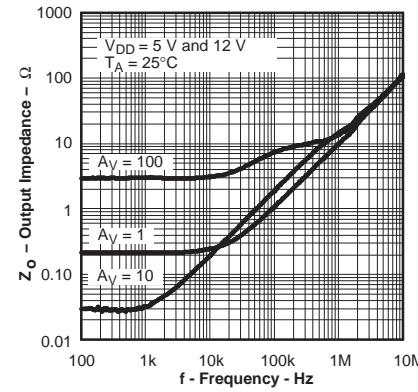
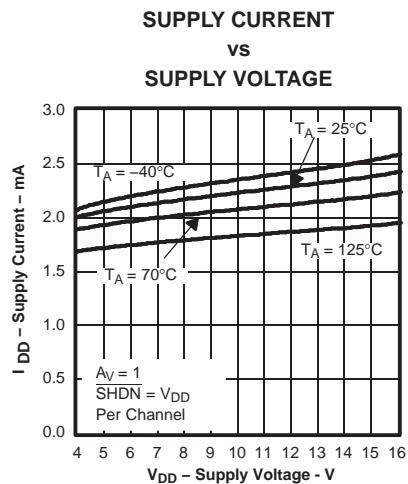
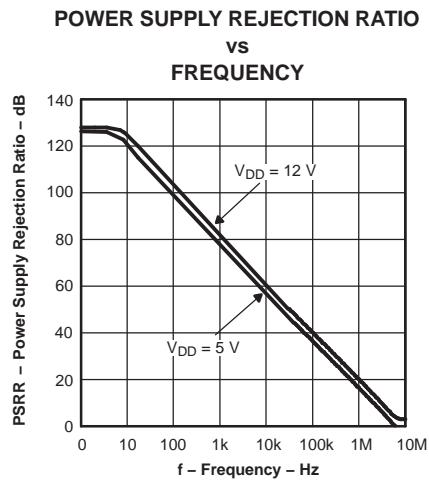
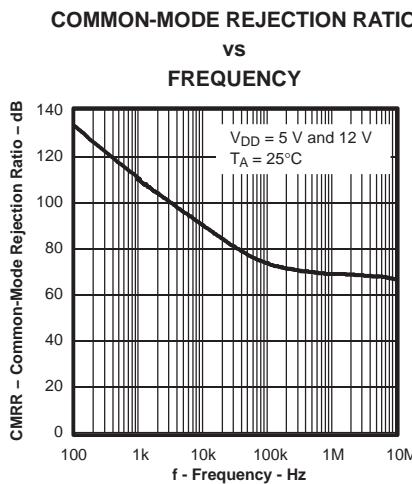
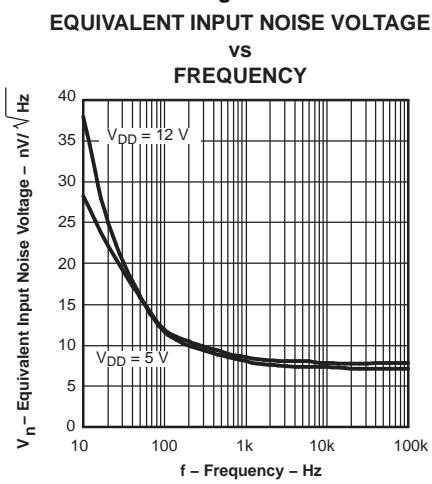
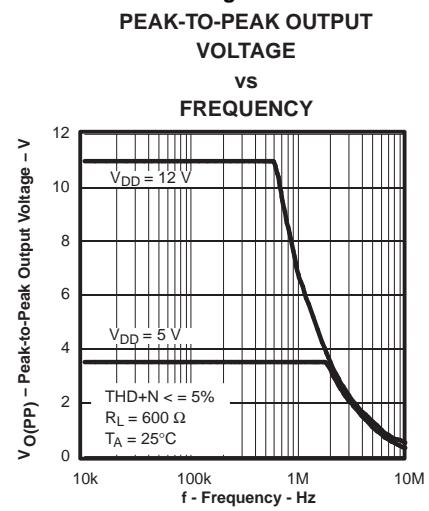
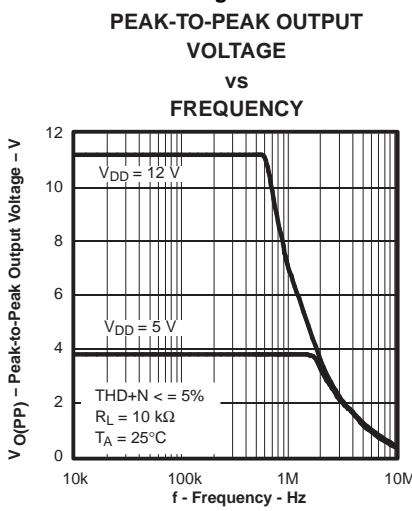
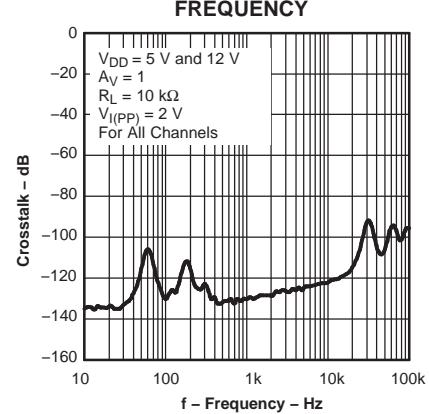


Figure 9.


Figure 10.

Figure 11.

Figure 12.

Figure 13.

Figure 14.

Figure 15.

Figure 16.

DIFFERENTIAL VOLTAGE GAIN AND
PHASE
VS
FREQUENCY

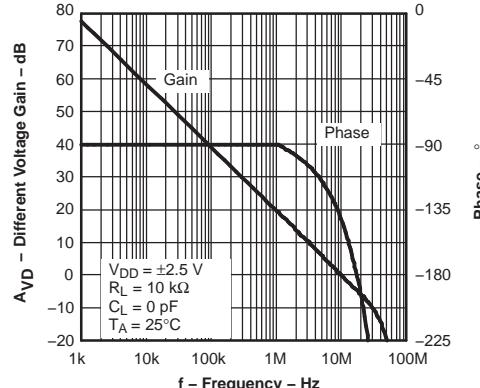


Figure 17.

DIFFERENTIAL VOLTAGE GAIN AND
PHASE
VS
FREQUENCY

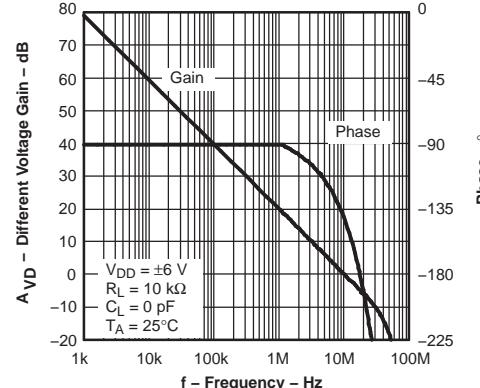
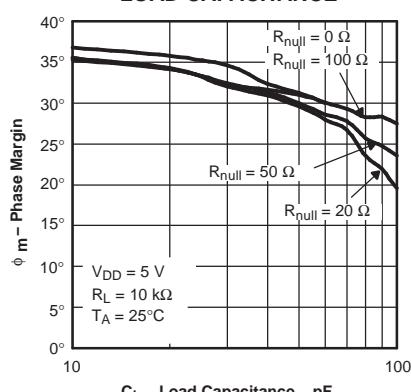


Figure 18.

PHASE MARGIN
VS

LOAD CAPACITANCE

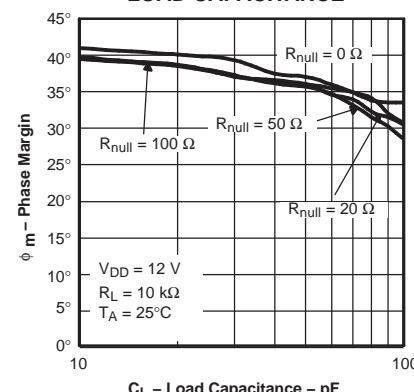


CL – Load Capacitance – pF

Figure 19.

PHASE MARGIN

VS
LOAD CAPACITANCE

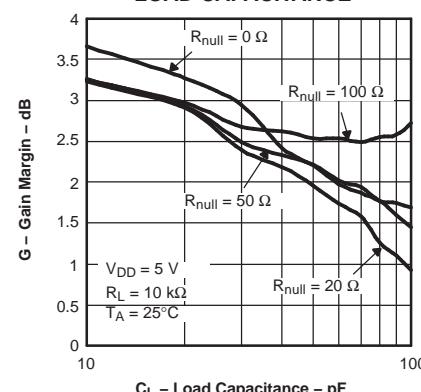


CL – Load Capacitance – pF

Figure 20.

GAIN MARGIN
VS

LOAD CAPACITANCE

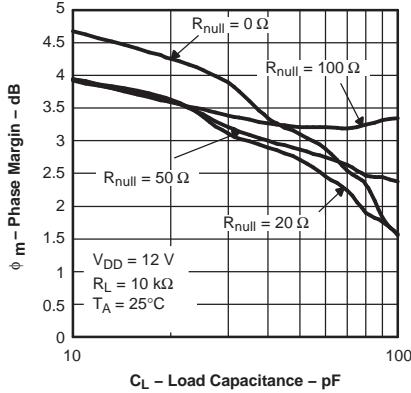


CL – Load Capacitance – pF

Figure 21.

GAIN MARGIN

VS
LOAD CAPACITANCE

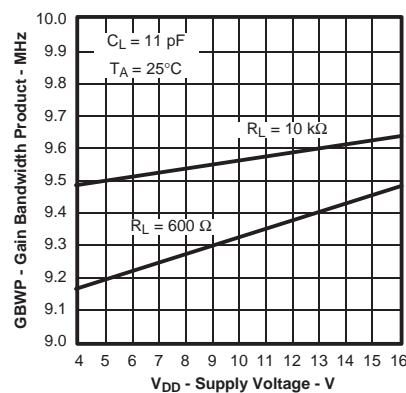


CL – Load Capacitance – pF

Figure 22.

GAIN BANDWIDTH PRODUCT

VS
SUPPLY VOLTAGE

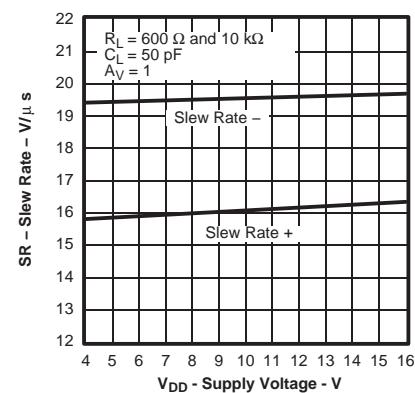


VDD - Supply Voltage - V

Figure 23.

SLEW RATE
VS

SUPPLY VOLTAGE



VDD - Supply Voltage - V

Figure 24.

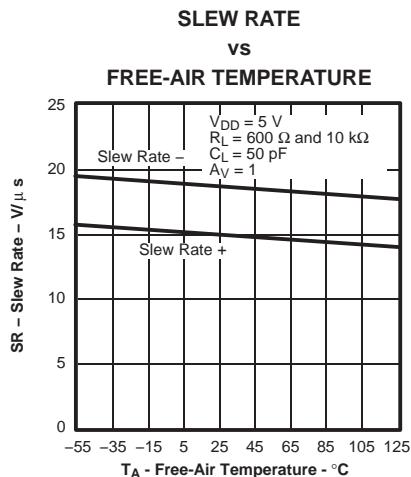


Figure 25.
TOTAL HARMONIC DISTORTION
PLUS NOISE

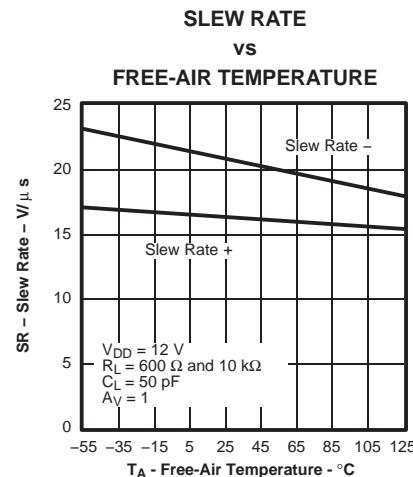


Figure 26.
TOTAL HARMONIC DISTORTION
PLUS NOISE

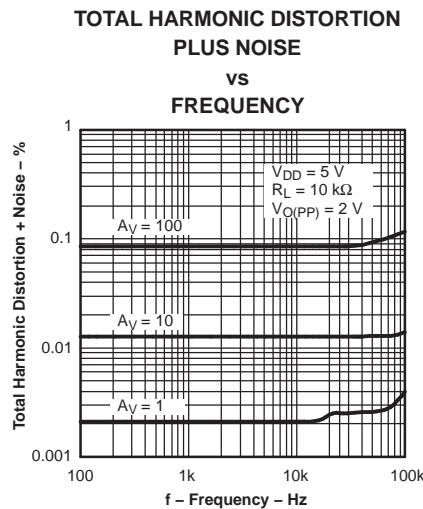


Figure 27.
TOTAL HARMONIC DISTORTION
PLUS NOISE

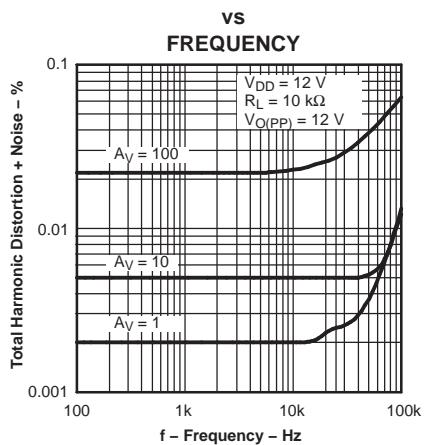


Figure 28.
LARGE SIGNAL FOLLOWER
PULSE RESPONSE

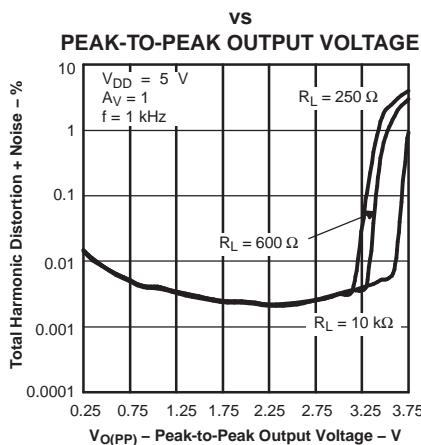


Figure 29.
LARGE SIGNAL FOLLOWER
PULSE RESPONSE

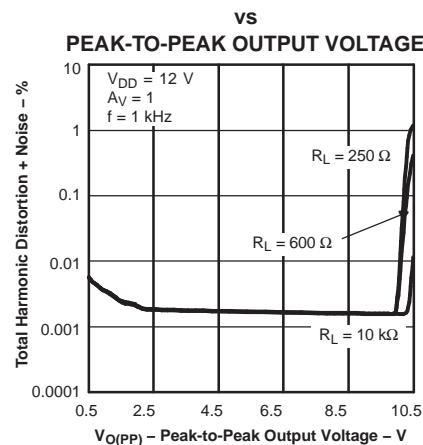


Figure 30.
SMALL SIGNAL FOLLOWER PULSE
RESPONSE

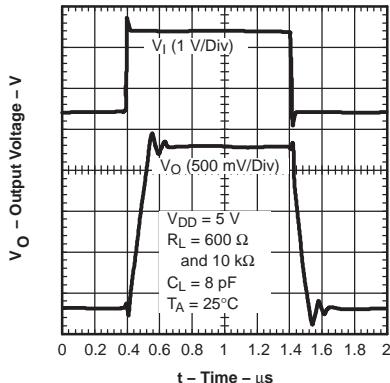


Figure 31.

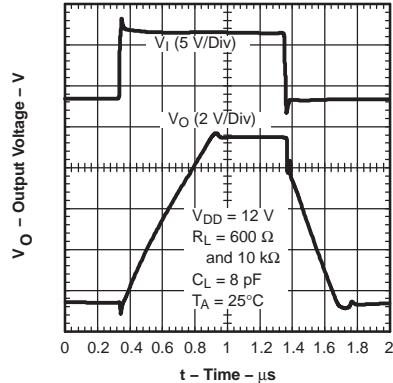


Figure 32.

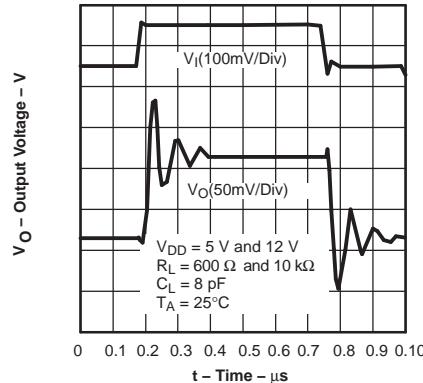
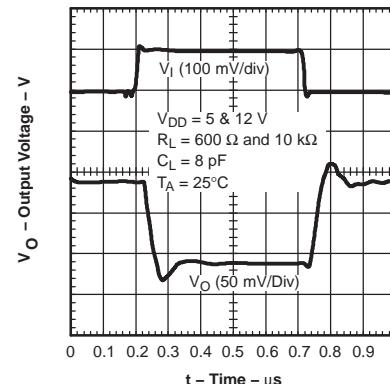
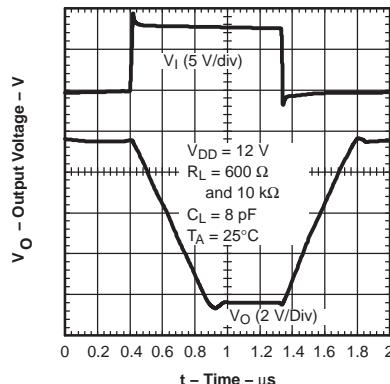
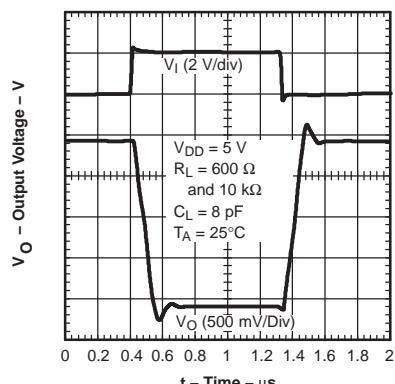


Figure 33.

LARGE SIGNAL INVERTING
PULSE RESPONSELARGE SIGNAL INVERTING
PULSE RESPONSESMALL SIGNAL INVERTING
PULSE RESPONSE

PARAMETER MEASUREMENT INFORMATION

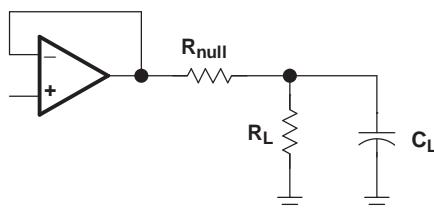


Figure 37. Input Offset Voltage Null Circuit

APPLICATION INFORMATION

Driving a Capacitive Load

When the amplifier is configured in this manner, capacitive loading directly on the output decreases the device's phase margin, leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series (R_{NULL}) with the output of the amplifier, as shown in Figure 38. A minimum value of 20 Ω should work well for most applications.

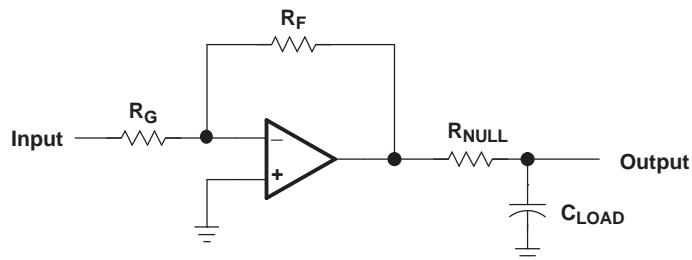


Figure 38. Driving a Capacitive Load

Offset Voltage

The output offset voltage (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula (see Figure 39) can be used to calculate the output offset voltage:

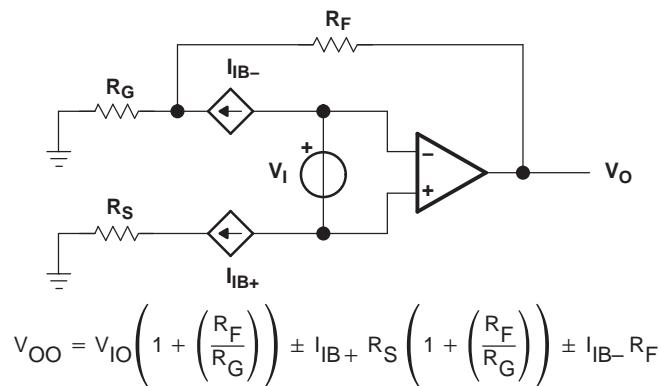


Figure 39. Output Offset Voltage Model

High-Speed CMOS Input Amplifiers

The TLC072 is a high-speed low-noise CMOS input operational amplifier that has an input capacitance of the order of 20 pF. Any resistor used in the feedback path adds a pole in the transfer function equivalent to the input capacitance multiplied by the combination of source resistance and feedback resistance. For example, a gain of -10, a source resistance of 1 k Ω , and a feedback resistance of 10 k Ω add an additional pole at approximately 8 MHz. This is more apparent with CMOS amplifiers than bipolar amplifiers due to their greater input capacitance.

This is of little consequence on slower CMOS amplifiers, as this pole normally occurs at frequencies above their unity-gain bandwidth. However, the TLC07x with its 10-MHz bandwidth means that this pole normally occurs at frequencies where there is on the order of 5-dB gain left and the phase shift adds considerably.

The effect of this pole is the strongest with large feedback resistances at small closed loop gains. As the feedback resistance is increased, the gain peaking increases at a lower frequency and the 180° phase shift crossover point also moves down in frequency, decreasing the phase margin.

For the TLC072, the maximum feedback resistor recommended is 5 k Ω ; larger resistances can be used but a capacitor in parallel with the feedback resistor is recommended to counter the effects of the input capacitance pole.

The TLC072 with a 1-V step response has an 80% overshoot with a natural frequency of 3.5 MHz when configured as a unity gain buffer and with a 10-k Ω feedback resistor. By adding a 10-pF capacitor in parallel with the feedback resistor, the overshoot is reduced to 40% and eliminates the natural frequency, resulting in a much faster settling time (see Figure 40). The 10-pF capacitor was chosen for convenience only.

Load capacitance had little effect on these measurements due to the excellent output drive capability of the TLC072.

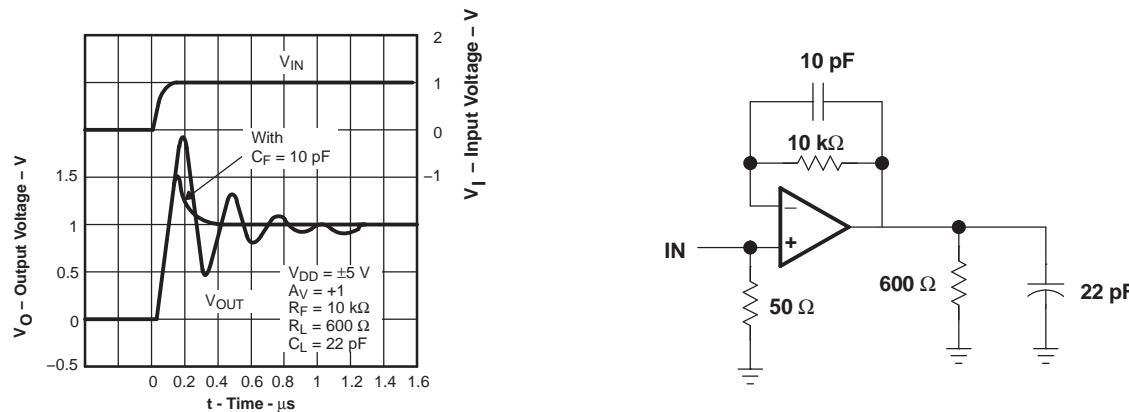


Figure 40. 1-V Step Response

General Configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 41).

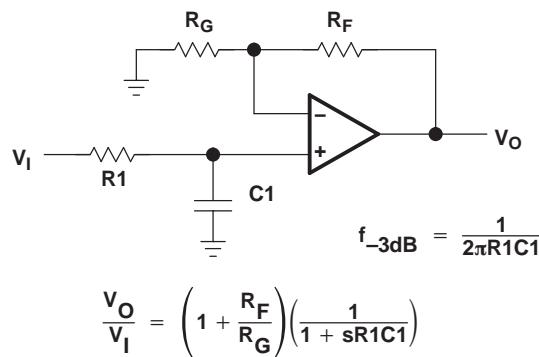


Figure 41. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task (see [Figure 42](#)). For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

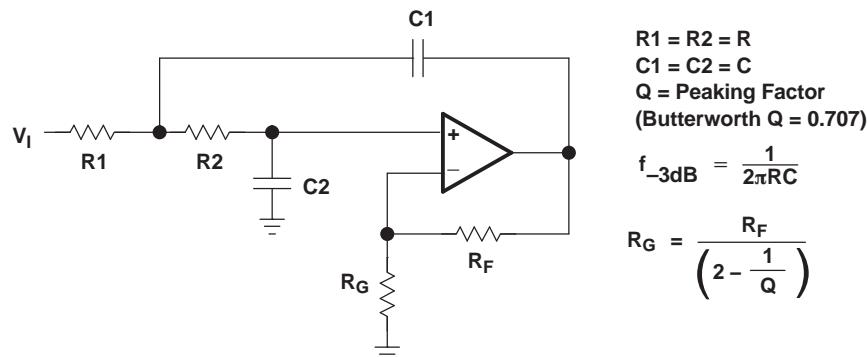


Figure 42. Two-Pole Low-Pass Sallen-Key Filter

Circuit Layout Considerations

To achieve the levels of high performance of the TLC072, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- **Ground planes**

A ground plane should be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.

- **Proper power supply decoupling**

Use a 6.8- μF tantalum capacitor in parallel with a 0.1- μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1- μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1- μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inch between the device power terminals and the ceramic capacitors.

- **Sockets**

Sockets can be used but are not recommended. The additional lead inductance in the socket pins often leads to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.

- **Short trace runs/compact part placements**

Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.

- **Surface-mount passive components**

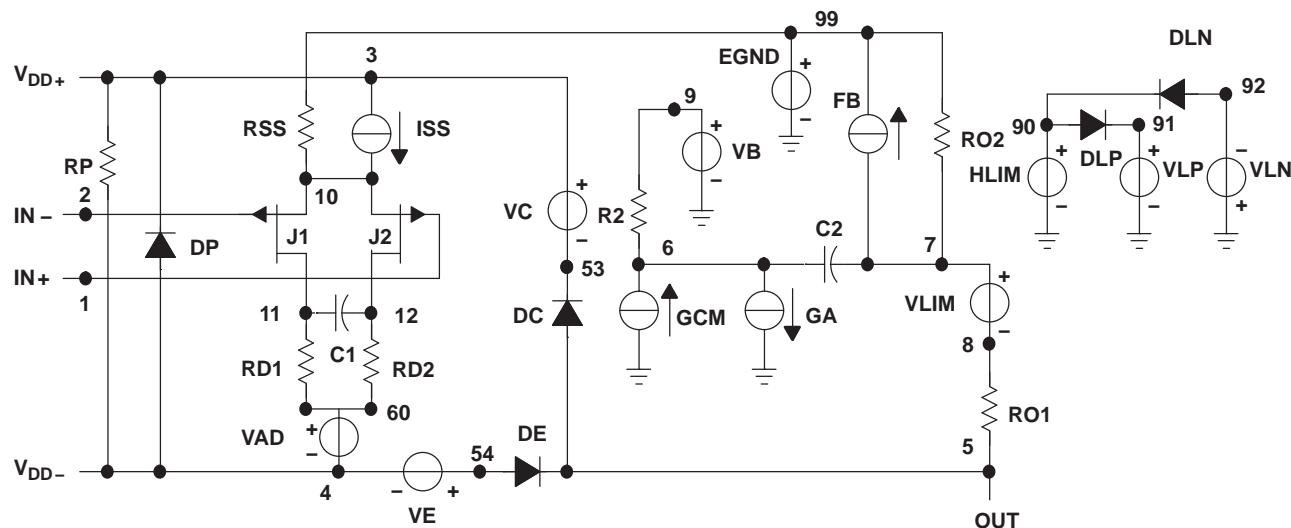
Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

Macromodel Information

Macromodel information provided was derived using MicroSim PartsTM, the model generation software used with MicroSim PSpiceTM. The Boyle macromodel⁽¹⁾ and subcircuit in [Figure 43](#) are generated using the TLC07x typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

(1) G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).



*DEVICE=TLC07X_5V, OPAMP, PJF, INT

* TLC07X – 5V operational amplifier "macromodel" subcircuit
 * created using Parts release 8.0 on 12/16/99 at 08:38
 * Parts is a MicroSim product.

* connections:
 * non-inverting input
 * inverting input
 * positive power supply
 * negative power supply
 * output
 *

.subckt TLC07X_5V 1 2 3 4 5

*

c1	11	12	4.8697E-12
c2	6	7	8.0000E-12
css	10	99	4.0063E-12
dc	5	53	dy
de	54	5	dy
dip	90	91	dx
dln	92	90	dx
dp	4	3	dx
egnd	99	0	poly(2) (3,0) (4,0) 0 .5 .5
fb	7	99	poly(5) vb vc ve vlp vln 0 6.9132E6 -1E3 1E3 6E6 -6E6

ga	6	0	11	12	457.42E-6
gcm	0	6	10	99	1.1293E-6
iss	3	10	dc		183.67E-6
ioff	0	6	dc		.806E-6
hlim	90	0	vlim	1K	
j1	11	2	10		jx1
j2	12	1	10		jx2
r2	6	9			100.00E3
rd1	4	11			2.1862E3
rd2	4	12			2.1862E3
ro1	8	5	10		
ro2	7	99	10		
rp	3	4			2.4728E3
rss	10	99			1.0889E6
vb	9	0	dc		0
vc	3	53	dc		1.5410
ve	54	4	dc		.84403
vlim	7	8	dc		0
vlp	91	0	dc		119
vln	0	92	dc		119
.model	dx	D(Is=800.00E-18)			
.model	dy	D(Is=800.00E-18 Rs=1m Cjo=10p)			
.model	jx1	PJF(Is=117.50E-15 Beta=1.1391E-3 Vto=-1)			
.model	jx2	PJF(Is=117.50E-15 Beta=1.1391E-3 Vto=-1)			
.ends					

Figure 43. Boyle Macromodel and Subcircuit

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TLC072QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF TLC072-Q1 :

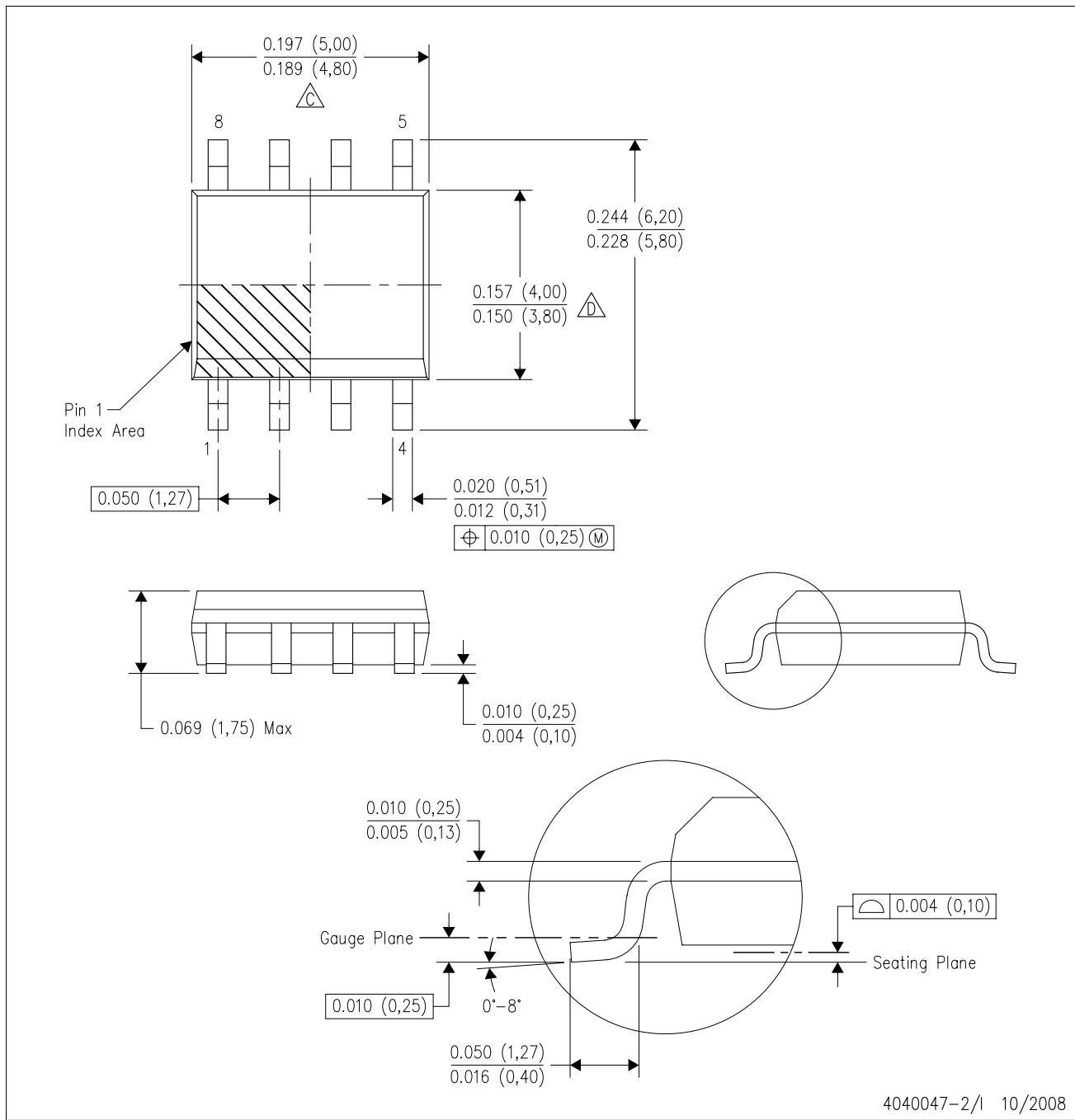
- Catalog: [TLC072](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.

D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.

E. Reference JEDEC MS-012 variation AA.

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