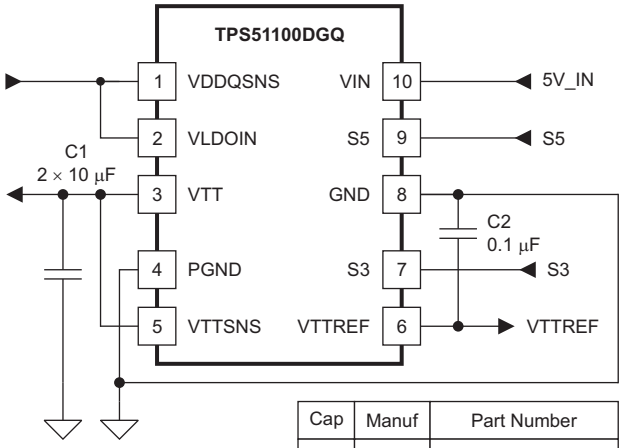
3-A SINK/SOURCE DDR TERMINATION REGULATOR

FEATURES

- **Input Voltage Range: 4.75 V to 5.25 V**
- **VLDOIN Voltage Range: 1.2 V to 3.6 V**
- **3-A Sink/Source Termination Regulator Includes Droop Compensation**
- **Requires Only 20-µF Ceramic Output Capacitance**
- **Supports High-Z in S3 and Soft-Off in S5**
- **1.2-V Input (VLDOIN) Helps Reduce Total Power Dissipation**
- **Integrated Divider Tracks 0.5 VDDQSNS for VTT and VTTREF**
- **Remote Sensing (VTTSNS)**
- **±20-mV Accuracy for VTT and VTTREF**
- **10-mA Buffered Reference (VTTREF)**
- **Built-In Soft-Start, UVLO and OCL**
- **Thermal Shutdown**
- **Supports JEDEC Specifications**

APPLICATIONS

- **DDR, DDR2, DDR3 Memory Termination**
- **SSTL-2, SSTL-18 and HSTL Termination**



Cap	Manuf	Part Number
C1	TDK	C2012JB0J106K
C2	TDK	C1608JB1H104K

B0318-01

The TPS51100 is a 3-A sink/source tracking termination regulator. It is specifically designed for low-cost/low-external component count systems, where space is a premium.

The TPS51100 maintains fast transient response, only requiring 20 µF (2 × 10 µF) of ceramic output capacitance. The TPS51100 supports remote sensing functions and all features required to power the DDR and DDR2 VTT bus termination according to the JEDEC specification. The part also supports DDR3 VTT termination with VDDQ at 1.5 V (typ). In addition, the TPS51100 includes integrated sleep-state controls, placing VTT in high-Z in S3 (suspend to RAM) and soft-off for VTT and VTTREF in S5 (suspend to disk). The TPS51100 is available in the thermally efficient 10-pin MSOP PowerPAD™ package and is specified from –40°C to 85°C.

ORDERING INFORMATION

T_A	PLASTIC MSOP PowerPAD™ PACKAGE (DGQ)(1)
–40°C to 85°C	TPS51100DGQ

(1) The DGQ package is also available taped and reeled. Add an R suffix to the device type (i.e., TPS51100DGQR). See the application section of the data sheet for the PowerPAD package drawing and layout information.

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PowerPAD is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE	UNIT
	Input voltage range(2)	VIN, VLDOIN, VTTSNS, VDDQSNS, S3, S5	–0.3 to 6	V
		PGND	–0.3 to 0.3	
	Output voltage range(2)	VTT, VTTREF	–0.3 to 6	V
T_A	Operating ambient temperature range		–40 to 85	°C
T_{stg}	Storage temperature		–55 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.c
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

DISSIPATION RATINGS

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
10-pin DGQ	1.73 W	17.3 mW/°C	0.694 W

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Supply voltage		4.75	5.25	V
	Voltage range	S3, S5	–0.10	5.25	V
		VLDOIN, VDDQSNS, VTT, VTTSNS	–0.1	3.6	
		VTTREF	–0.1	1.8	
		PGND	–0.1	0.1	
T_A	Operating free-air temperature		–40	85	°C

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C, V_{VIN} = 5 V, VLDOIN and VDDQSNS are connected to 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VIN}	Supply current, VIN	T_A = 25°C, V_{VIN} = 5 V, no load, V_{S3} = V_{S5} = 5 V	0.25	0.5	1	mA
I_{VINSTB}	Standby currrent, VIN	T_A = 25°C, V_{VIN} = 5 V, no load, V_{S3} = 0 V, V_{S5} = 5 V	25	50	80	µA
I_{VINSDN}	Shutdown current, VIN	T_A = 25°C, V_{VIN} = 5 V, no load, V_{S3} = V_{S5} = 0 V, V_{VLDOIN} = $V_{VDDQSNS}$ = 0 V		0.3	1	µA
I_{VLDOIN}	Supply current, VLDOIN	T_A = 25°C, V_{VIN} = 5 V, no load, V_{S3} = V_{S5} = 5 V	0.7	1.2	2	mA
$I_{VLDOINSTB}$	Standby currrent, VLDOIN	T_A = 25°C, V_{VIN} = 5 V, no load,V_{S3} = 0 V, V_{S5} = 5 V		6	10	µA
$I_{VLDOINSDN}$	Shutdown current, VLDOIN	T_A = 25°C, V_{VIN} = 5 V, no load, V_{S3} = V_{S5} = 0 V		0.3	1	µA

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ELECTRICAL CHARACTERISTICS (continued)

T_A = –40°C to 85°C, V_{VIN} = 5 V, VLDOIN and VDDQSNS are connected to 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENT						
$I_{VDDQSNS}$	Input current, VDDQSNS	V_{VIN} = 5 V, V_{S3} = V_{S5} = 5 V	1	3	5	µA
I_{VTTSNS}	Input current, VTTSNS	V_{VIN} = 5 V, V_{S3} = V_{S5} = 5 V	–1	–0.25	1	µA
VTT OUTPUT						
V_{VTTSNS}	Output voltage, VTT	V_{VLDOIN} = $V_{VDDQSNS}$ = 2.5 V		1.25		V
		V_{VLDOIN} = $V_{VDDQSNS}$ = 1.8 V		0.9		
		V_{VLDOIN} = $V_{VDDQSNS}$ = 1.5 V		0.75		
$V_{VTTTOL25}$	Output votlage tolerance to VTTREF, VTT	V_{VLDOIN} = $V_{VDDQSNS}$ = 2.5 V, $\|I_{VTT}\|$ = 0 A	–20		20	mV
		V_{VLDOIN} = $V_{VDDQSNS}$ = 2.5 V, $\|I_{VTT}\|$ = 1.5 A	–30		30	
		V_{VLDOIN} = $V_{VDDQSNS}$ = 2.5 V, $\|I_{VTT}\|$ = 3 A	–40		40	
$V_{VTTTOL18}$		V_{VLDOIN} = $V_{VDDQSNS}$ = 1.8 V, $\|I_{VTT}\|$ = 0 A	–20		20	
		V_{VLDOIN} = $V_{VDDQSNS}$ = 1.8 V, $\|I_{VTT}\|$ = 1 A	–30		30	
		V_{VLDOIN} = $V_{VDDQSNS}$ = 1.8 V, $\|I_{VTT}\|$ = 2 A	–40		40	
$V_{VTTTOL15}$		V_{VLDOIN} = $V_{VDDQSNS}$ = 1.5 V, $\|I_{VTT}\|$ = 0 A	–20		20	
		V_{VLDOIN} = $V_{VDDQSNS}$ = 1.5 V, $\|I_{VTT}\|$ = 1 A	–30		30	
$I_{VTTOCLSRC}$	Source current limit, VTT	$V_{TT} = \left(\frac{V_{VDDQSNS}}{2}\right) \times 0.95$, PGOOD = High	3	3.8	6	A
		V_{VTT} = 0 V	1.5	2.2	3	
$I_{VTTOCLSNK}$	Sink current limit, VTT	$V_{TT} = \left(\frac{V_{VDDQSNS}}{2}\right) \times 1.05$, PGOOD = High	3	3.6	6	A
		V_{VTT} = V_{VDDQ}	1.5	2.2	3	
I_{VTTLK}	Leakage current, VTT	$V_{TT} = \left(\frac{V_{VDDQSNS}}{2}\right) \times 1.25$ V, T_A = 25°C	–1	0.5	10	µA
		V_{S3} = 0 V, V_{S5} = 5 V				
$I_{VTTSNSLK}$	Leakage current, VTTSNS	$V_{TT} = \left(\frac{V_{VDDQSNS}}{2}\right) \times 1.25$ V, T_A = 25°C	–1	0.01	1	µA
I_{DSCHRG}	Discharge current, VTT	T_A = 25°C, V_{S3} = V_{S5} = 0 V, $V_{VDDQSNS}$ = 0 V, V_{VTT} = 0.5 V	10	17		mA
VTTREF OUTPUT						
V_{VTTREF}	Output voltage, VTTREF			$\frac{V_{VDDQSNS}}{2}$		V
$V_{VTTREFTOL25}$	Output voltage tolerance to VDDQSNS/2, VTTREF	V_{VLDOIN} = $V_{VDDQSNS}$ = 2.5 V, I_{VTTREF} < 10 mA	–20		20	mV
$V_{VTTREFTOL18}$		V_{VLDOIN} = $V_{VDDQSNS}$ = 1.8 V, I_{VTTREF} < 10 mA	–17		17	
$V_{VTTREFTOL15}$		V_{VLDOIN} = $V_{VDDQSNS}$ = 1.5 V, I_{VTTREF} < 10 mA	–15		15	
$I_{VTTREFOCL}$	Source current limit, VTTREF	V_{VTTREF} = 0 V	10	20	30	mA
UVLO/LOGIC THRESHOLD						
V_{VINUV}	UVLO threshold voltage, VIN	Wake up	3.4	3.7	4	V
		Hysteresis	0.15	0.25	0.35	
V_{IH}	High-level input voltage	S3, S5	1.6			V
V_{IL}	Low-level input voltage	S3, S5			0.3	V
V_{IHYST}	Hysteresis voltage	S3, S5		0.2		V
I_{ILEAK}	Logic input leakage current	S2, S5, T_A = 25°C	–1		1	µA
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature		160		°C
		Hysteresis		10		

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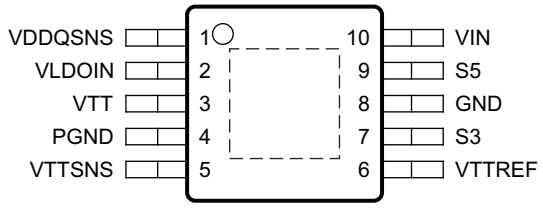
DEVICE INFORMATION

DGQ Package
(Top View)



Actual Size
3,05 mm x 4,98 mm

P0083-01

NOTE: For more information on the DGQ package, see the *PowerPAD Thermally Enhanced Package* application report (SLMA002).

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
GND	8	–	Signal ground. Connect to negative terminal of the output capacitor
PGND	4	–	Power ground output for the VTT LDO
S3	7	I	S3 signal input
S5	9	I	S5 signal input
VDDQSNS	1	I	VDDQ sense input
VIN	10	I	5-V power supply
VLDOIN	2	I	Power supply for the VTT LDO and VTTREF output stage
VTT	3	O	Power output for the VTT LDO
VTTREF	6	O	VTT reference output. Connect to GND through 0.1-µF ceramic capacitor.
VTTSNS	5	I	Voltage sense input for the VTT LDO. Connect to plus terminal of the output capacitor.

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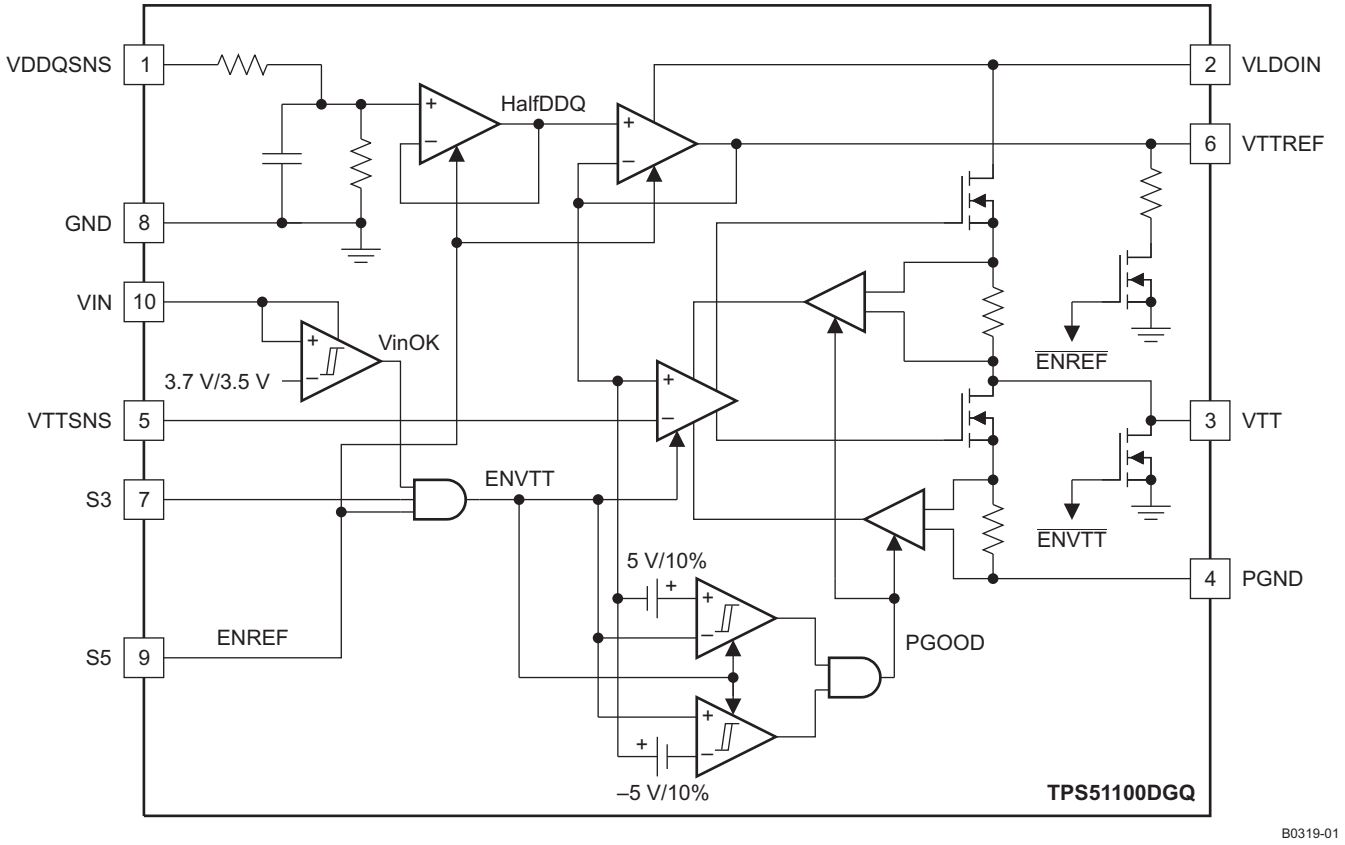
SIMPLIFIED BLOCK DIAGRAM



DETAILED DESCRIPTION

VTT SINK/SOURCE REGULATOR

The TPS51100 is a 3-A sink/source tracking termination regulator designed specially for low-cost, low-external-components systems where space is at premium, such as notebook PC applications. The TPS51100 integrates a high-performance, low-dropout linear regulator that is capable of sourcing and sinking current up to 3 A. This VTT linear regulator employs an ultimate fast-response feedback loop so that small ceramic capacitors are enough to keep tracking to the VTTREF within ±40 mV under all conditions, including fast load transient. To achieve tight regulation with minimum effect of trace resistance, a remote sensing terminal, VTTSNS, should be connected to the positive node of the VTT output capacitor(s) as a separate trace from the high-current line from VTT.

VTTREF Regulator

The VTTREF block consists of an on-chip 1/2 divider, low-pass filter (LPF), and buffer. This regulator can source current up to 10 mA. Bypass VTTREF to GND using a 0.1-µF ceramic capacitor to ensure stable operation.

Soft-Start

The soft-start function of the VTT is achieved via a current clamp, allowing the output capacitors to be charged with low and constant current that gives linear ramp-up of the output voltage. The current-limit threshold is changed in two stages using an internal powergood signal. When VTT is outside the powergood threshold, the current limit level is 2.2 A. When VTT rises above (VTTREF – 5%) or falls below (VTTREF + 5%), the current limit level switches to 3.8 A. The thresholds are typically VTTREF ±5% (from outside regulation to inside) and ±10% (when it falls outside). The soft-start function is completely symmetrical, and it works not only from GND to VTTREF voltage, but also from VDDQ to VTTREF voltage. Note that the VTT output is in a high-impedance state during the S3 state (S3 = low, S5 = high), and its voltage can be up to VDDQ voltage, depending on the external condition. Note that VTT does not start under a full-load condition.

S5 Control and Soft-Off

The S3 and S5 terminals should be connected to SLP_S3 and SLP_S5 signals, respectively. Both VTTREF and VTT are turned on at the S0 state (S3 = high, S5 = high). VTTREF is kept alive while VTT is turned off and left high-impedance in the S3 state (S3 = low, S5 = high). Both VTT and VTTREF outputs are turned off and discharged to ground through internal MOSFETs during S4/S5 state (both S3 and S5 are low).

Table 1. S3 and S5 Control Tabl

STATE	S3	S5	VTTREF	VTT
S0	H	H	1	1
S3(1)	L	H	1	0 (high-Z)
S4/S5(1)	L	L	0 (discharge)	0 (discharge)

(1) In case S3 is forced to H and S5 to L, VTTREF is discharged and VTT is at High-Z state. This condition is NOT recommended.

VTT Current Protection

The LDO has a constant overcurrent limit (OCL) at 3.8 A. This trip point is reduced to 2.2 A before the output voltage comes within ±5% of the target voltage or goes outside of ±10% of the target voltage.

VIN UVLO Protection

For VIN undervoltage lockout (UVLO) protection, the TPS51100 monitors VIN voltage. When the VIN voltage is lower than UVLO threshold voltage, the VTT regulator is shut off. This is a non-latch protection.

Thermal Shutdown

TPS51100 monitors its temperature. If the temperature exceeds the threshold value, typically 160°C, the VTT and VTTREF regulators are shut off. This is also a non-latch protection.

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Output Capacitor

For stable operation, total capacitance of the VTT output terminal can be equal to or greater than 20 µF. Attach two 10-µF ceramic capacitors in parallel to minimize the effect of ESR and ESL. If the ESR is greater than 2 mΩ, insert an R-C filter between the output and the VTTSNS input to achieve loop stability. The R-C filter time constant should be almost the same or slightly lower than the time constant of the output capacitor and its ESR.

Soft-start duration, t_{SS}, is also a function of this output capacitance. Where I_{TTOCL} = 2.2 A (typ), t_{SS} can be calculated as,

$$t_{SS} = \left(\frac{C_{OUT} \times V_{VTT}}{I_{VTTOCL}} \right) \quad (1)$$

Input Capacitor

Depending on the trace impedance between the VLDOIN bulk power supply to the part, transient increase of source current is supplied mostly by the charge from the VLDOIN input capacitor. Use a 10-µF (or more) ceramic capacitor to supply this transient charge. Provide more input capacitance as more output capacitance is used at VTT. In general, use 1/2 C_{OUT} for the input.

VIN Capacitor

Add a ceramic capacitor with a value between 1 µF and 4.7 µF placed close to the VIN pin, to stabilize 5 V from any parasitic impedance from the supply.

Thermal Design

As the TPS51100 is a linear regulator, the VTT current flow in both source and sink directions generates power dissipation from the device. In the source phase, the potential difference between V_{VLDOIN} and V_{VTT} times VTT current becomes the power dissipation, W_{DSRC}.

$$W_{DSRC} = \left(V_{VLDOIN} - V_{VTT}\right) \times I_{VTT} \quad (2)$$

In this case, if VLDOIN is connected to an alternative power supply lower than V_{DDQ} voltage, power loss can be decreased.

For the sink phase, VTT voltage is applied across the internal LDO regulator, and the power dissipation, and W_{DSNK}, is calculated by:

$$W_{DSNK} = V_{VTT} \times I_{VTT} \quad (3)$$

Because the device does not sink and source the current at the same time and I_{VTT} varies rapidly with time, the actual power dissipation that must be considered for thermal design is an average over the thermal relaxation duration of the system. Another power consumption is the current used for internal control circuitry from the VIN supply and VLDOIN supply. This can be estimated as 20 mW or less at normal operational conditions. This power must be effectively dissipated from the package. Maximum power dissipation allowed to the package is calculated by,

$$W_{PKG} = \frac{\left(T_{J(max)} - T_{A(max)}\right)}{\theta_{JA}} \quad (4)$$

where

$T_{J(max)}$ is 125°C

$T_{A(max)}$ is the maximum ambient temperature in the system

θ_{JA} is the thermal resistance from the silicon junction to the ambient

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This thermal resistance strongly depends on the board layout. TPS51100 is assembled in a thermally enhanced PowerPAD package that has an exposed die pad underneath the body. For improved thermal performance, this die pad must be attached to the ground trace via thermal land on the PCB. This ground trace acts as a heat sink/spread. The typical thermal resistance, 57.7°C/W, is achieved based on a 3 mm × 2 mm thermal land with two vias without air flow. It can be improved by using larger thermal land and/or increasing the number of vias. For example, assuming a 3 mm × 3 mm thermal land with four vias without air flow, it is 45.4°C/W. Further information about the PowerPAD package and its recommended board layout is described in the *PowerPAD Thermally Enhanced Package* application report (SLMA002). This document is available at www.ti.com.

LAYOUT CONSIDERATIONS

Consider the following points before the layout of TPS51100 design begins.

- The input bypass capacitor for VLDOIN should be placed to the pin as close as possible with a short and wide connection.
- The output capacitor for VTT should be placed close to the pin with a short and wide connection in order to avoid additional ESR and/or ESL of the trace.
- VTTSNS should be connected to the positive node of VTT output capacitor(s) as a separate trace from the high current power line and is strongly recommended to avoid additional ESR and/or ESL. If it is needed to sense the voltage of the point of the load, it is recommended to attach the output capacitor(s) at that point. Also, it is recommended to minimize any additional ESR and/or ESL of the ground trace between the GND pin and the output capacitor(s).
- Consider adding an LPF at VTTSNS in case the ESR of the VTT output capacitor(s) is larger than 2 mΩ.
- VDDQSNS can be connected separately from VLDOIN. Remember that this sensing potential is the reference voltage of VTTREF. Avoid any noise generative lines.
- The negative node of the VTT output capacitor(s) and the VTTREF capacitor should be tied together, avoiding common impedance to the high-current path of the VTT source/sink current.
- The GND (signal GND) pin node represents the reference potential for the VTTREF and VTT outputs. Connect GND to the negative nodes of the VTT capacitor(s), VTTREF capacitor, and VDDQ capacitor(s) with care to avoid additional ESR and/or ESL. GND and PGND (Power GND) should be isolated, with a single point connection between them.
- In order to remove heat from the package effectively, prepare the thermal land and solder to the package thermal pad. The wide trace of the component-side copper, connected to this thermal land, helps heat spreading. Numerous vias 0.33 mm in diameter connected from the thermal land to the internal/solder-side ground plane(s) should be used to help dissipation.

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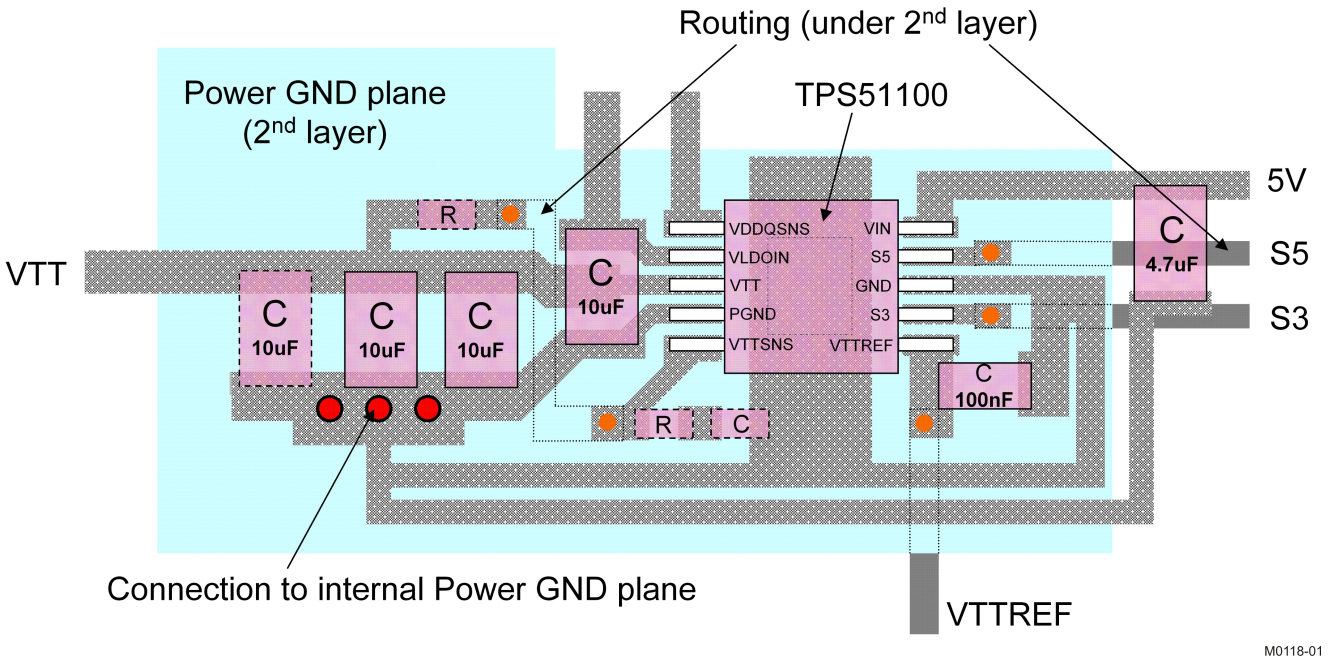


NOTES:

1. The ositive terminal of the output capacitors should be directly connected to VTT of the IC; do not use a VIA.
2. The negative terminal of the output capacitors should be directly connected to GND of the IC; do not use a VIA.
3. VIAs
   - VIA between 1st and 2nd layers
   - VIA between 1st and other layers under 2nd
4. Rs and Cs with dotted outlines are options.

Figure 1. TPS51100 PCB Layout Guideline

TYPICAL CHARACTERISTICS

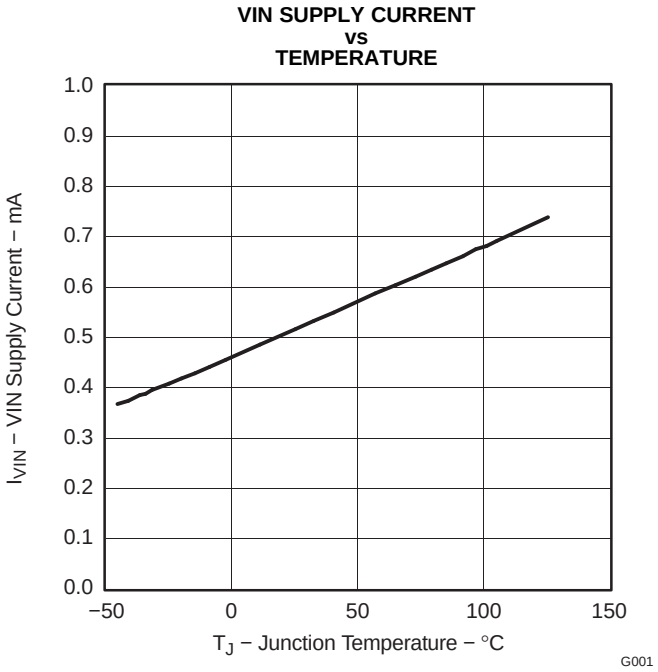
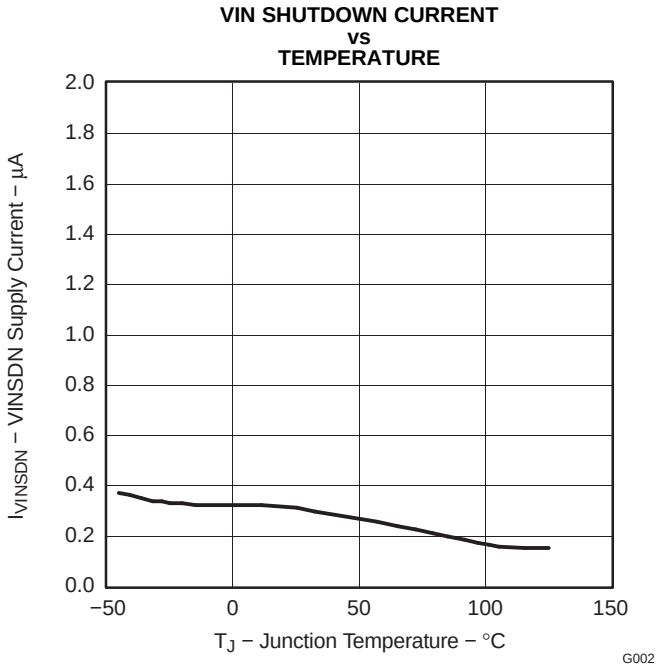


Figure 2.



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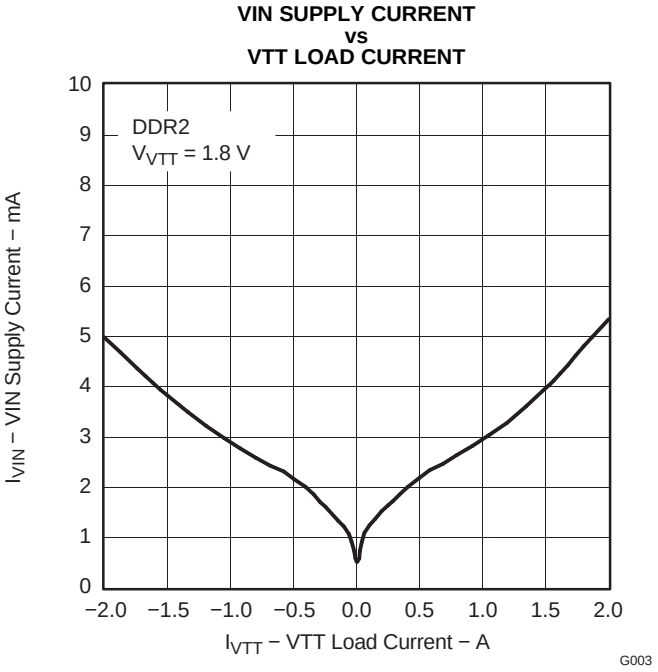

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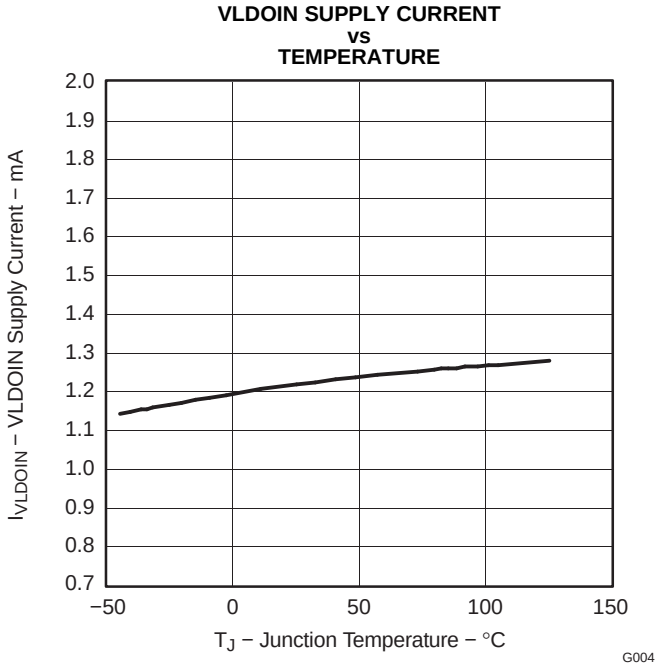

Figure 5.

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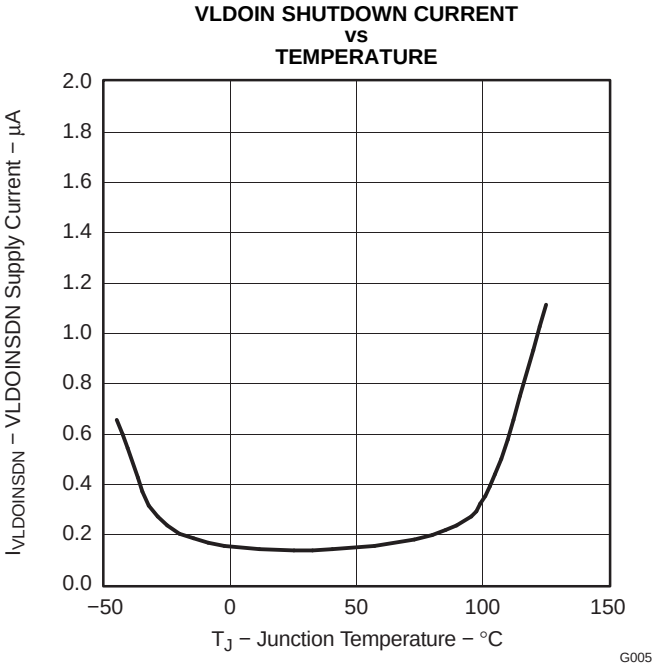
TYPICAL CHARACTERISTICS (continued)



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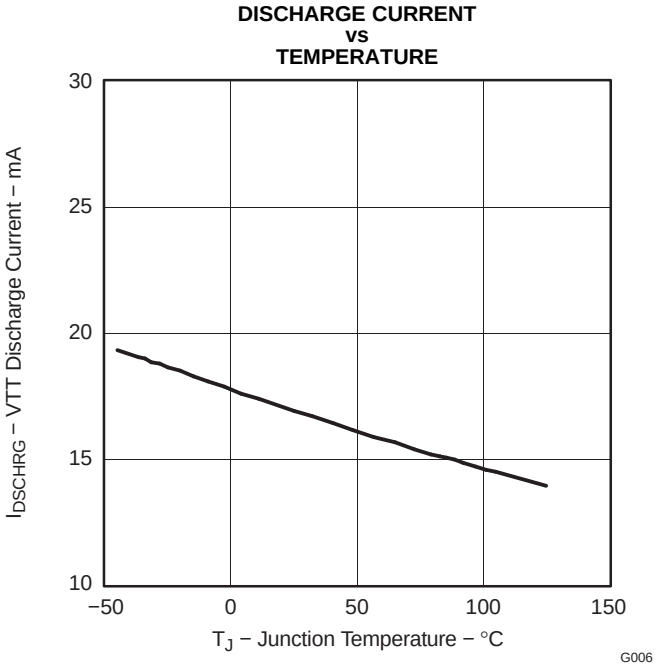
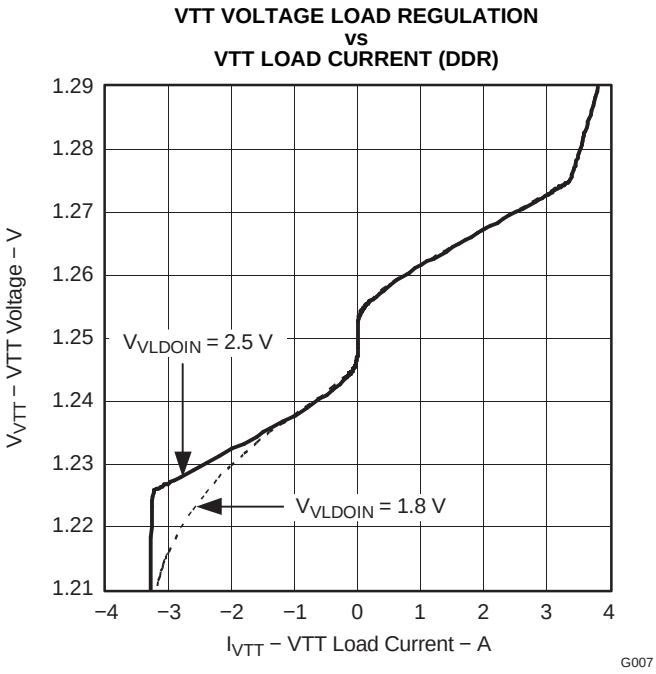


Figure 7.



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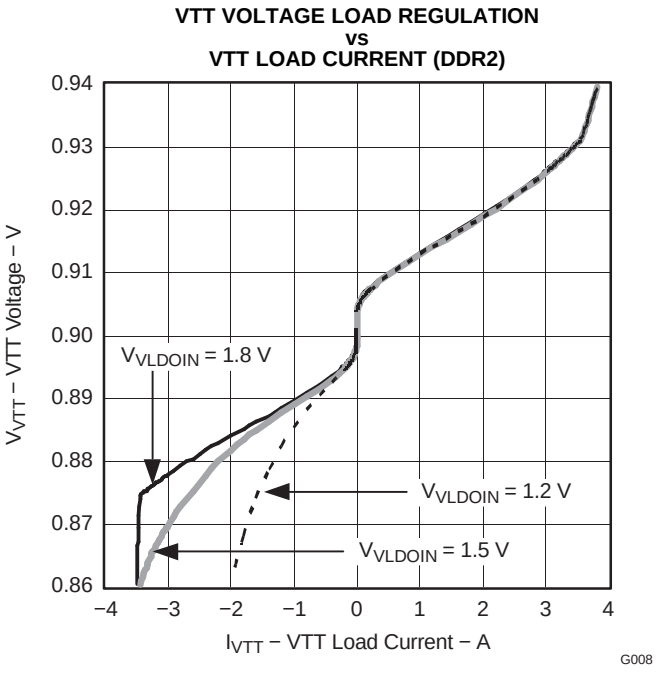

Figure 9.

TYPICAL CHARACTERISTICS (continued)

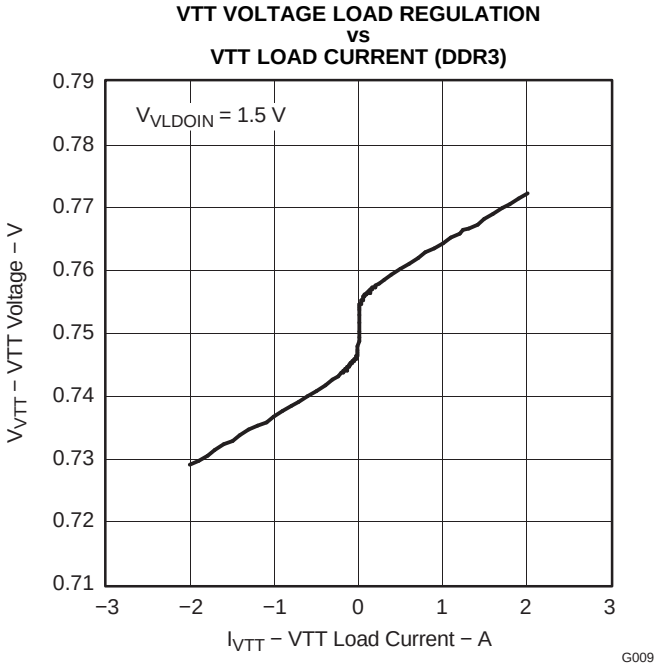

Figure 10.

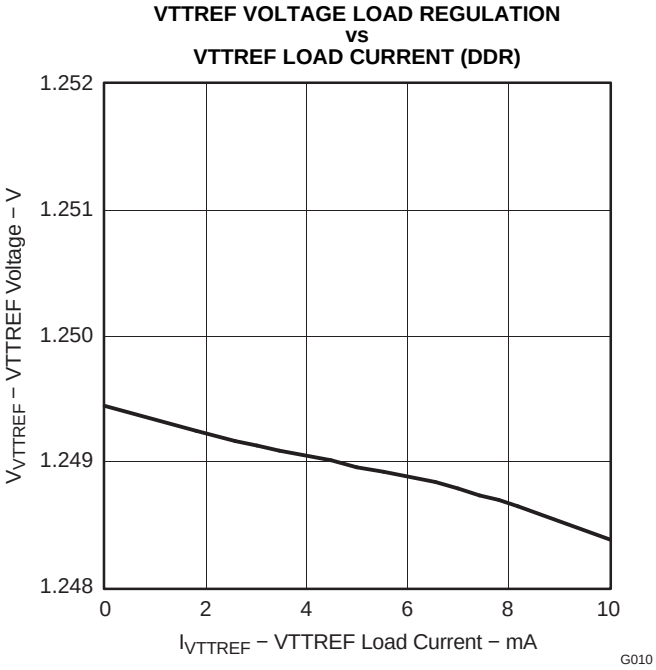

Figure 11.

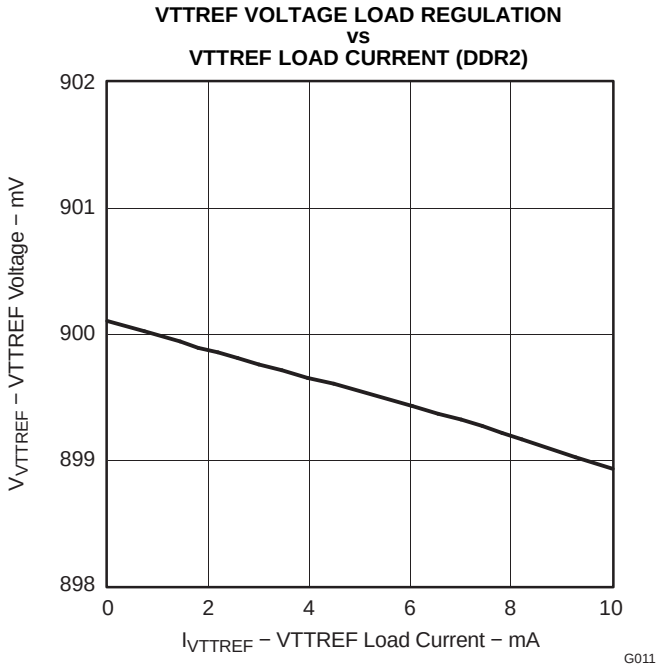

Figure 12.

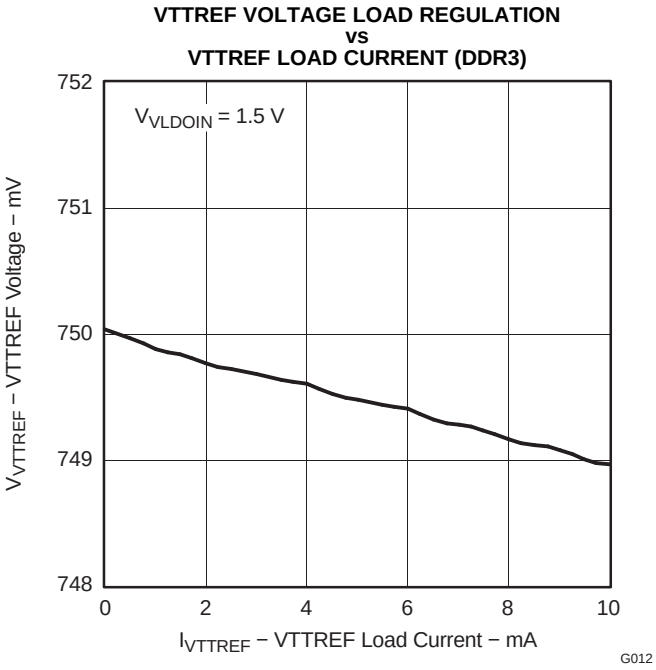

Figure 13.

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TYPICAL CHARACTERISTICS (continued)

VTT VOLTAGE LOAD TRANSIENT RESPONSE

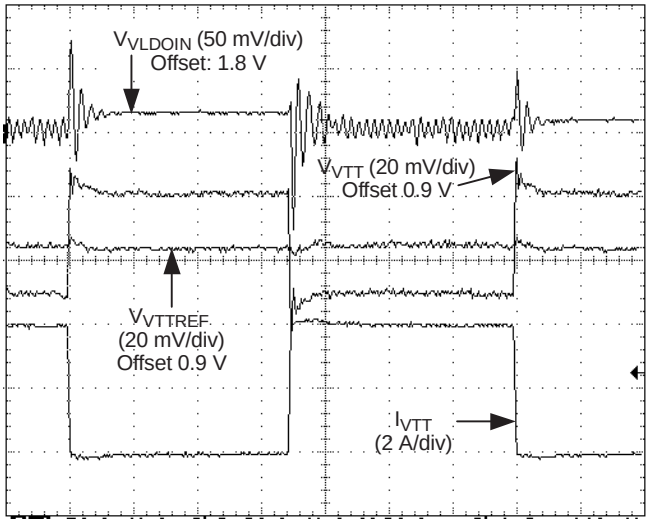

Figure 14.

STARTUP WAVEFORMS S5 LOW-TO-HIGH

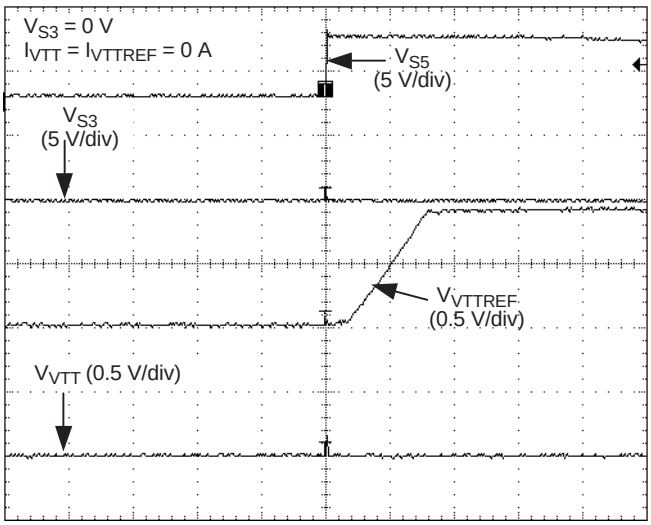

Figure 15.

STARTUP WAVEFORMS S3 LOW-TO-HIGH

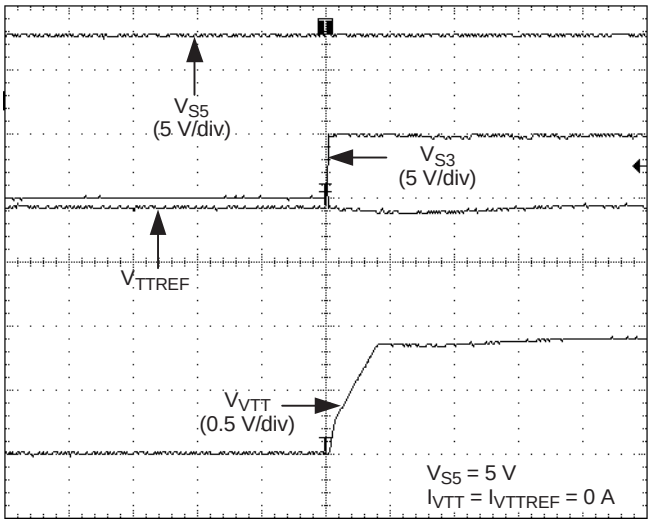

Figure 16.

SHUTDOWN WAVEFORMS S3 HIGH-TO-LOW

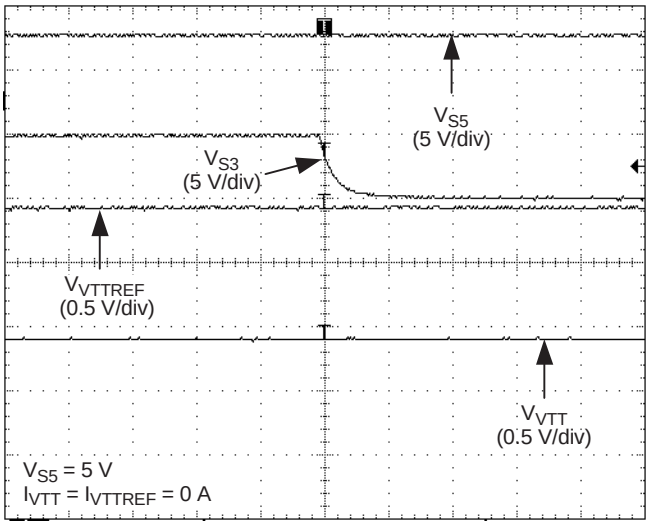

Figure 17.

TYPICAL CHARACTERISTICS (continued)

SHUTDOWN WAVEFORMS S3 AND S5 HIGH-TO-LOW

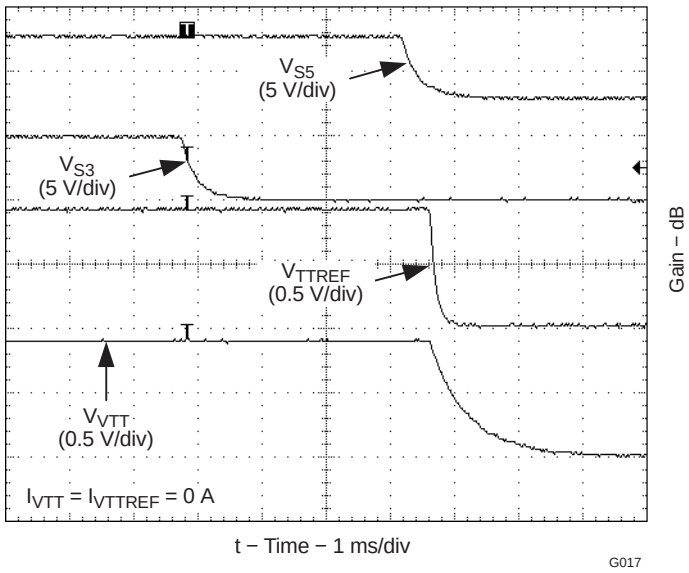

Figure 18.

BODE PLOT DDR SOURCE

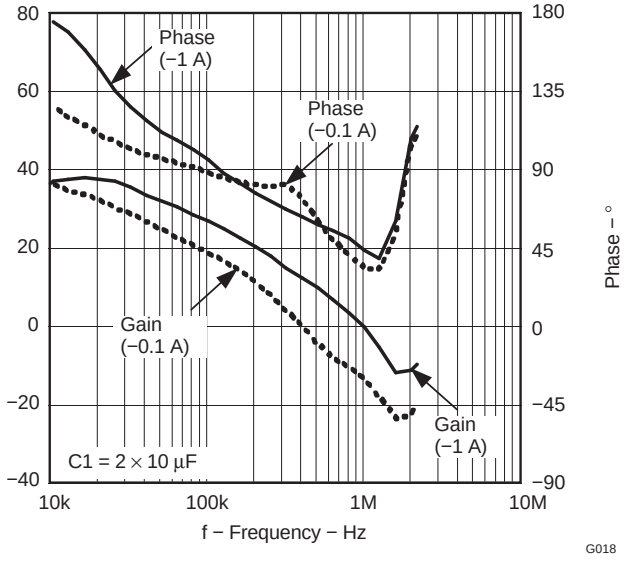

Figure 19.

BODE PLOT DDR SINK

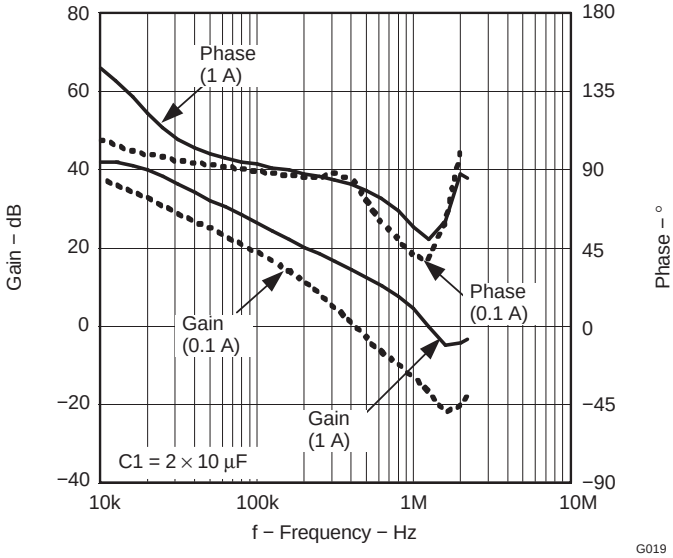

Figure 20.

BODE PLOT DDR2 SOURCE

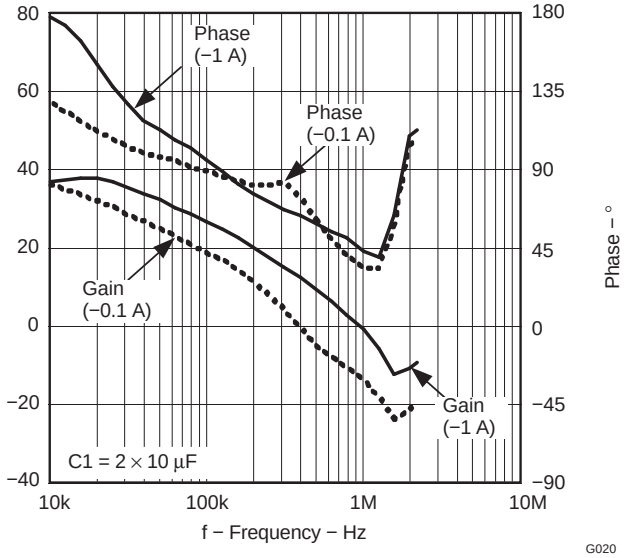

Figure 21.

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TYPICAL CHARACTERISTICS (continued)

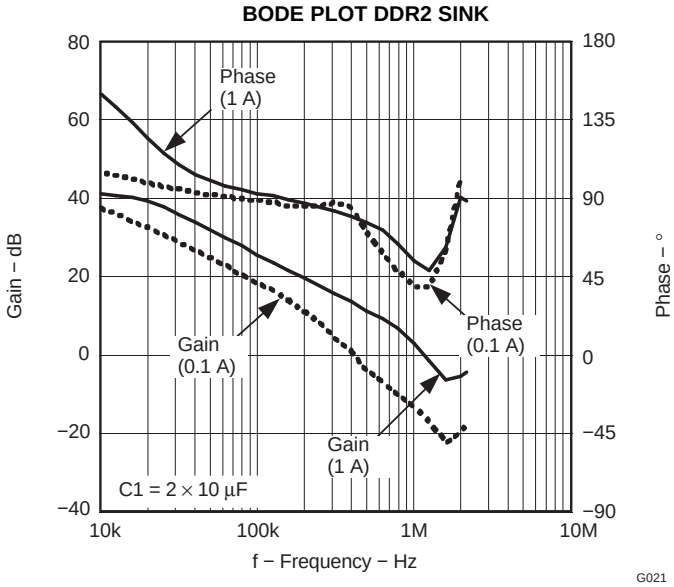

Figure 22.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS51100DGQ	ACTIVE	MSOP-Power PAD	DGQ	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS51100DGQG4	ACTIVE	MSOP-Power PAD	DGQ	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS51100DGQR	ACTIVE	MSOP-Power PAD	DGQ	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS51100DGQRG4	ACTIVE	MSOP-Power PAD	DGQ	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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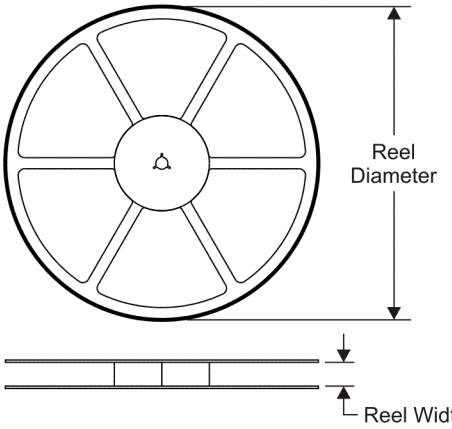
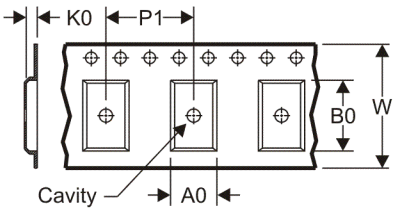
TAPE AND REEL INFORMATION

REEL DIMENSIONS

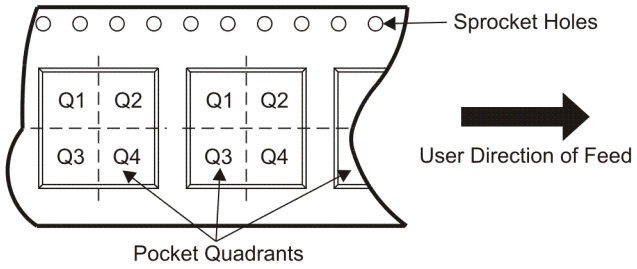


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

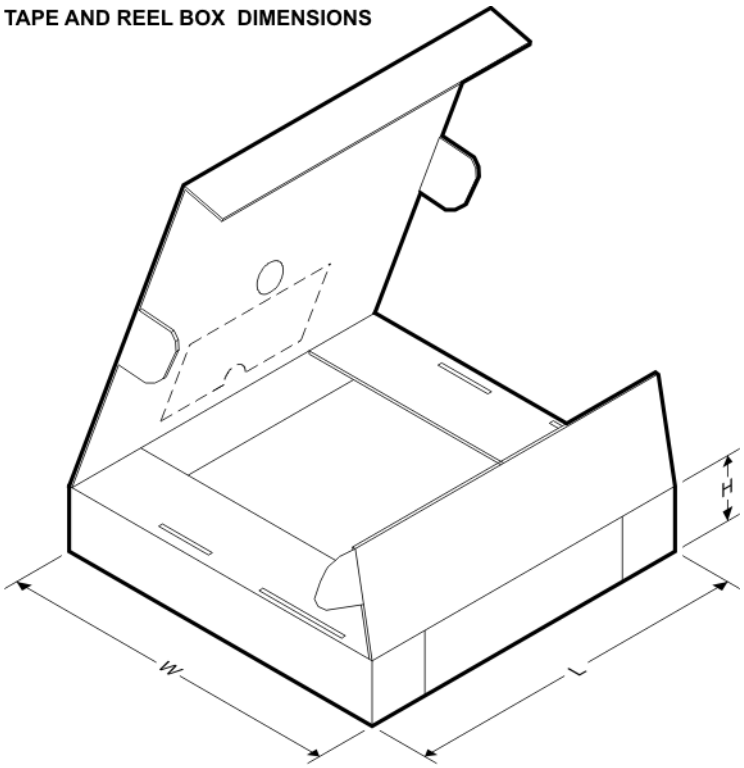
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51100DGQR	MSOP-Power PAD	DGQ	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS51100DGQR	MSOP-Power PAD	DGQ	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

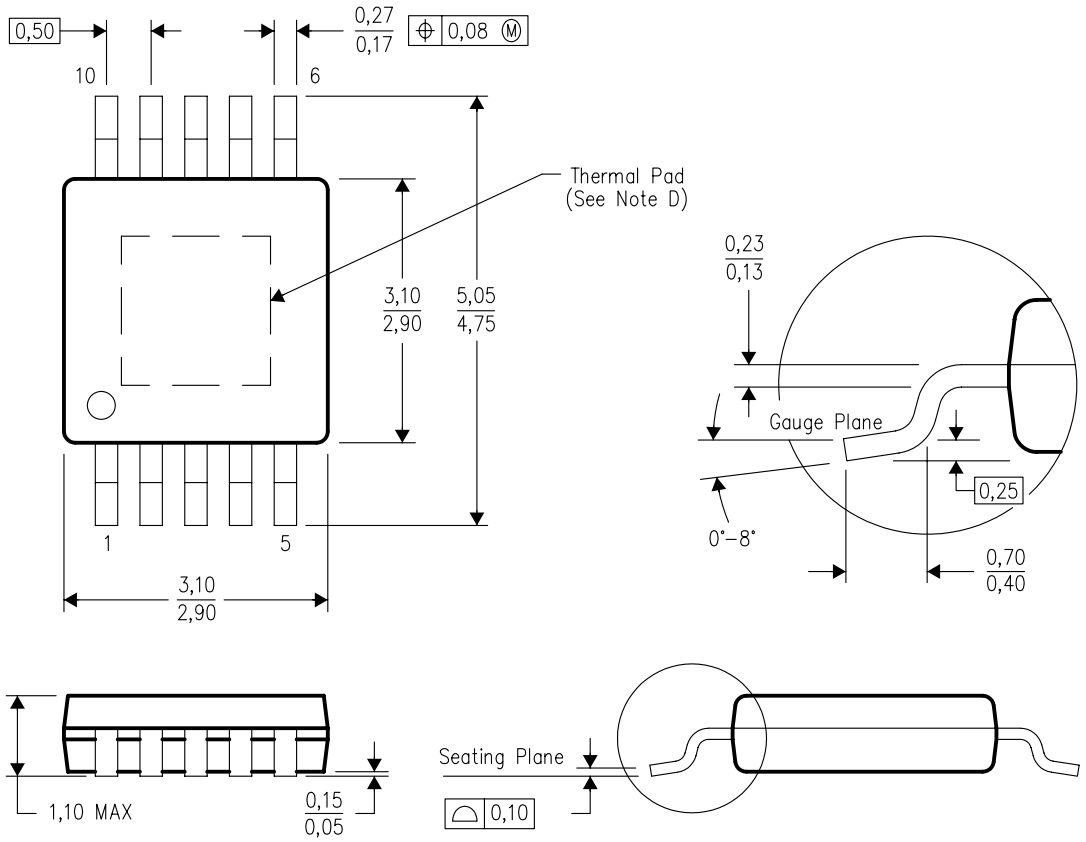
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51100DGQR	MSOP-PowerPAD	DGQ	10	2500	370.0	355.0	55.0
TPS51100DGQR	MSOP-PowerPAD	DGQ	10	2500	346.0	346.0	29.0

DGQ (S–PDSO–G10) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



4073273/D 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–187 variation BA–T.

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

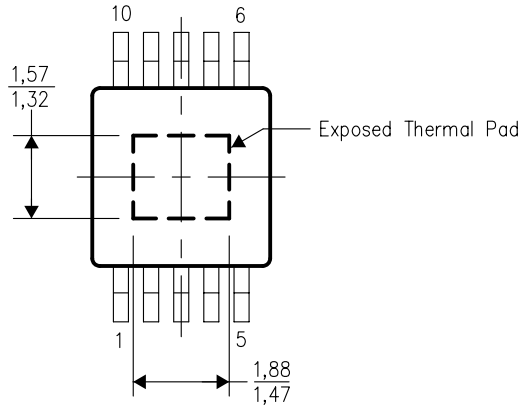
DGQ (S–PDSO–G10)

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

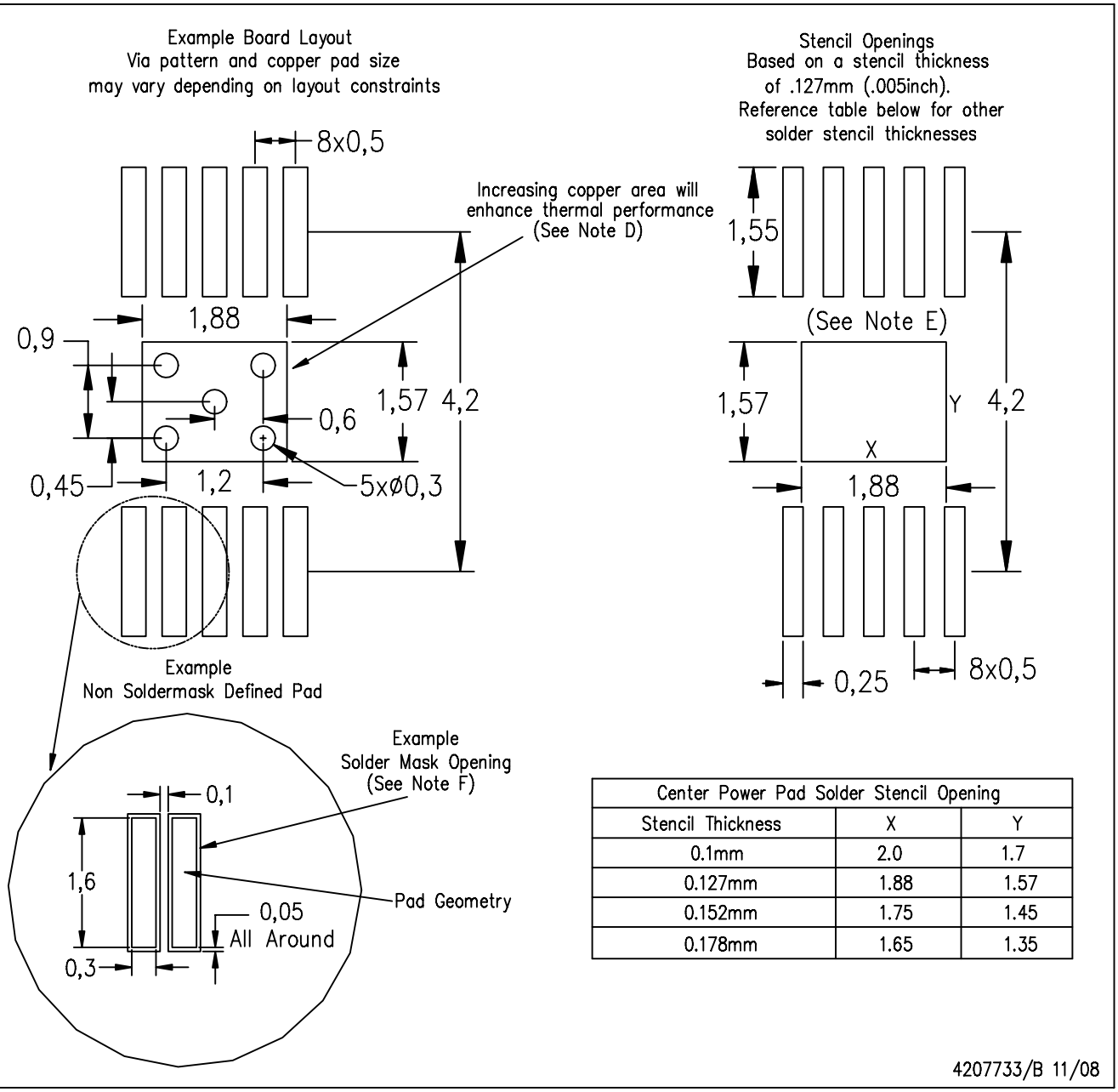


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DGQ (R–PDSO–G10) PowerPAD™



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.88	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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