TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS212D

February 1998 - Revised October 2003

High-Speed CMOS Logic
Quad Analog Switch with Level Translation

Features

- **Wide Analog-Input-Voltage Range**
  V_{CC} - V_{EE} . . . . **0V to 10V**
- **Low "ON" Resistance**
  - **45Ω (Typ)** . . . . **V_{CC} = 4.5V**
  - **35Ω (Typ)** . . . . **V_{CC} = 6V**
  - **30Ω (Typ)** . . . . **V_{CC} - V_{EE} = 9V**
- **Fast Switching and Propagation Delay Times**
- **Low "OFF" Leakage Current**
- **Built-In "Break-Before-Make" Switching**
- **Logic-Level Translation to Enable 5V Logic to Accommodate ±5V Analog Signals**
- **Wide Operating Temperature Range . . . -55°C to 125°C**
- **HC Types**
  - **2V to 10V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Description

The 'HC4316 and CD74HCT4316 contain four independent digitally controlled analog switches that use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

In addition these devices contain logic-level translation circuits that provide for analog signal switching of voltages between ±5V via 5V logic. Each switch is turned on by a high-level voltage on its select input (S) when the common Enable (E) is Low. A High E disables all switches. The digital inputs can swing between V_{CC} and GND; the analog inputs/outputs can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. Voltage ranges are shown in Figures 2 and 3.
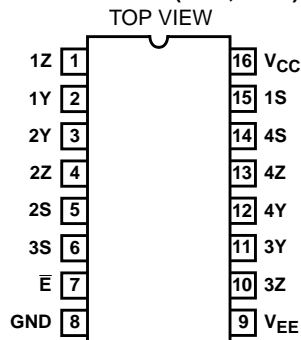
Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE
CD54HC4316F3A	-55 to 125	16 Ld CERDIP
CD74HC4316E	-55 to 125	16 Ld PDIP
CD74HC4316M	-55 to 125	16 Ld SOIC
CD74HC4316MT	-55 to 125	16 Ld SOIC
CD74HC4316M96	-55 to 125	16 Ld SOIC
CD74HC4316NSR	-55 to 125	16 Ld SOP
CD74HC4316PW	-55 to 125	16 Ld TSSOP
CD74HC4316PWR	-55 to 125	16 Ld TSSOP
CD74HC4316PWT	-55 to 125	16 Ld TSSOP
CD74HCT4316E	-55 to 125	16 Ld PDIP
CD74HCT4316M	-55 to 125	16 Ld SOIC
CD74HCT4316MT	-55 to 125	16 Ld SOIC
CD74HCT4316M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

Pinout

CD54HC4316 (CERDIP)
CD74HC4316 (PDIP, SOIC, SOP, TSSOP)
CD74HCT4316 (PDIP, SOIC)
TOP VIEW

1Z	1		16	V_{CC}
1Y	2		15	1S
2Y	3		14	4S
2Z	4		13	4Z
2S	5		12	4Y
3S	6		11	3Y
$\overline{E}$	7		10	3Z
GND	8		9	V_{EE}

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Functional Diagram

TRUTH TABLE

INPUTS		SWITCH
$\overline{E}$	S	
L	L	OFF
L	H	ON
H	X	OFF

H= High Level Voltage
L= Low Level Voltage
X= Don't Care

Logic Diagram

FIGURE 1. ONE SWITCH

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . -0.5V to 7V
DC Supply Voltage, V_{CC} - V_{EE} . . . . -0.5V to 10.5V
DC Supply Voltage, V_{EE} . . . . 0.5V to -7V
DC Input Diode Current, I_{IK}
  For V_I < -0.5V or V_I > V_{CC} 0.5V . . . . ±20mA
DC Switch Diode Current, I_{OK}
  For V_I < V_{EE} -0.5V or V_I < V_{CC} + 0.5V . . . . ±25mA
DC Switch Diode Current
  For V_I > V_{EE} -0.5V or V_I < V_{CC} + 0.5V . . . . ±25mA
DC Output Diode Current, I_{OK}
  For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . ±20mA
DC Output Source or Sink Current per Output Pin, I_O
  For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} . . . . ±50mA

Operating Conditions

Temperature Range, T_A . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
  HC Types . . . . .2V to 6V
  HCT Types . . . . .4.5V to 5.5V
Supply Voltage Range, V_{CC} - V_{EE}
  HC, HCT Types (Figure 2) . . . . .2V to 10V
Supply Voltage Range, V_{EE}
  HC, HCT Types (Figure 3) . . . . 0V to -6V
DC Input or Output Voltage, V_I . . . . GND to V_{CC}
Analog Switch I/O Voltage, V_{IS} . . . . V_{EE} (Min)
 . . . . V_{CC} (Max)
Input Rise and Fall Time, t_r, t_f
  2V . . . . 1000ns (Max)
  4.5V . . . . 500ns (Max)
  6V . . . . 400ns (Max)

Thermal Information

Package Thermal Impedance, θ_{JA} (see Note 1):
  E (PDIP) Package . . . . .67°C/W
  M (SOIC) Package. . . . . .73°C/W
  NS (SOP) Package . . . . .64°C/W
  PW (TSSOP) Package . . . . .108°C/W
Maximum Junction Temperature (Plastic Package) . . . . 150°
Maximum Storage Temperature Range . . . . -65°C to 150°
Maximum Lead Temperature (Soldering 10s) . . . . 300°
  SOIC - Lead Tips Only

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Area as a Function of Supply Voltage
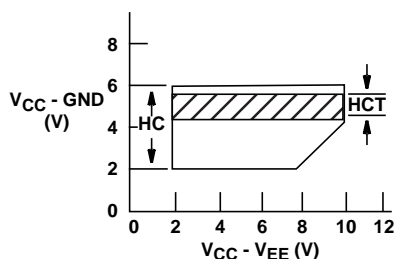
FIGURE 2.
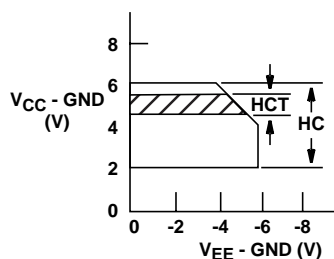
FIGURE 3.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	V_{IS} (V)	V_{EE} (V)	V_{CC} (V)	25°C MIN	TYP	MAX	-40°C TO 85°C MIN	MAX	-55°C TO 125°C MIN	MAX	UNITS
HC TYPES													
High Level Input Voltage	V_{IH}	-	-	-	2	1.5	-	-	1.5	-	1.5	-	V
					4.5	3.15	-	-	3.15	-	3.15	-	V
					6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	-	2	-	-	0.5	-	0.5	-	0.5	V
					4.5	-	-	1.35	-	1.35	-	1.35	V
					6	-	-	1.8	-	1.8	-	1.8	V
"ON" Resistance I_O = 1mA (Figures 4, 5)	R_{ON}	V_{IH} or V_{IL}	V_{CC} or V_{EE}	0	4.5	-	45	180	-	225	-	270	Ω
				0	6	-	35	160	-	200	-	240	Ω
				-4.5	4.5	-	30	135	-	170	-	205	Ω
			V_{CC} to V_{EE}	0	4.5	-	85	320	-	400	-	480	Ω
				0	6	-	55	240	-	300	-	360	Ω
				-4.5	4.5	-	35	170	-	215	-	255	Ω
Maximum "ON" Resistance Between Any Two Channels	ΔR_{ON}	-	-	0	4.5	-	10	-	-	-	-	-	Ω
				0	6	-	8.5	-	-	-	-	-	Ω
				-4.5	4.5	-	5	-	-	-	-	-	Ω
Switch Off Leakage Current	I_{IZ}	V_{IH} or V_{IL}	V_{CC} - V_{EE}	0	6	-	-	±0.1	-	±1	-	±1	µA
				-5	5	-	-	±0.1	-	±1	-	±1	µA
Control Input Leakage Current	I_{IL}	V_{CC} or GND	-	0	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current I_O = 0	I_{CC}	V_{CC} or GND	When V_{IS} = V_{EE}, V_{OS}=V_{CC} When V_{IS}=V_{CC}, V_{OS} =V_{EE}	0	6	-	-	8	-	80	-	160	µA
				-5	5	-	-	16	-	160	-	320	µA
HCT TYPES													
High Level Input Voltage	V_{IH}	-	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
"ON" Resistance I_O = 1mA (Figures 4, 5)	R_{ON}	V_{IH} or V_{IL}	V_{CC} or V_{EE}	0	4.5	-	45	180	-	225	-	270	Ω
				-4.5	4.5	-	30	135	-	170	-	205	Ω
			V_{CC} to V_{EE}	0	4.5	-	85	320	-	400	-	480	Ω
				-4.5	4.5	-	35	170	-	215	-	255	Ω
Maximum "ON" Resistance Between Any Two Channels	ΔR_{ON}	-	-	0	4.5	-	10	-	-	-	-	-	Ω
				-4.5	4.5	-	5	-	-	-	-	-	Ω
Switch Off Leakage Current	I_{IZ}	V_{IH} or V_{IL}	V_{CC} - V_{EE}	0	6	-	-	±0.1	-	±1	-	±1	µA
				-5	5	-	-	±0.1	-	±1	-	±1	µA

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS				25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	V_{IS} (V)	V_{EE} (V)	V_{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Control Input Leakage Current	I_I	V_{CC} or GND	-	0	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current $I_O = 0$	I_{CC}	Any Voltage Between V_{CC} and GND	When $V_{IS} = V_{EE}$, $V_{OS} = V_{CC}$, When $V_{IS} = V_{CC}$, $V_{OS} = V_{EE}$	0	5.5	-	-	8	-	80	-	160	μA
				-4.5	5.5	-	-	16	-	160	-	320	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note 2)	V_{CC} -2.1	-	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

2. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
All	0.5

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360μA max at 25°C.

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{EE} (V)	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
Propagation Delay, Switch In to Out	t_{PLH}, t_{PHL}	C_L = 50pF	0	2	-	-	60	-	75	-	90	ns
			0	4.5	-	-	12	-	15	-	18	ns
			0	6	-	-	10	-	13	-	15	ns
			-4.5	4.5	-	-	8	-	10	-	12	ns
Turn "ON" Time $\overline{E}$ to Out	t_{PZH}, t_{PZL}	C_L = 50pF	0	2	-	-	205	-	255	-	310	ns
			0	4.5	-	-	41	-	51	-	62	ns
			0	6	-	-	35	-	43	-	53	ns
			-4.5	4.5	-	-	37	-	47	-	56	ns
		C_L = 15pF	-	5	-	17	-	-	-	-	-	ns
Turn "ON" Time nS to Out	t_{PZH}, t_{PZL}	C_L = 50pF	0	2	-	-	175	-	220	-	265	ns
			0	4.5	-	-	35	-	44	-	53	ns
			0	6	-	-	30	-	37	-	45	ns
			-4.5	4.5	-	-	34	-	43	-	51	ns
		C_L = 15pF	-	5	-	14	-	-	-	-	-	ns
Turn "OFF" Time $\overline{E}$ to Out	t_{PLZ}, t_{PHZ}	C_L = 50pF	0	2	-	-	205	-	255	-	310	ns
			0	4.5	-	-	41	-	51	-	62	ns
			0	6	-	-	35	-	43	-	53	ns
			-4.5	4.5	-	-	37	-	47	-	56	ns
		C_L = 15pF	-	5	-	17	-	-	-	-	-	ns

Switching Specifications Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{EE} (V)	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Turn "OFF" Time nS to Out	t_{PLZ}, t_{PHZ}	C_L = 50pF	0	2	-	-	175	-	220	-	265	ns
			0	4.5	-	-	35	-	44	-	53	ns
			0	6	-	-	30	-	37	-	45	ns
			-4.5	4.5	-	-	34	-	43	-	51	ns
		C_L = 15pF	-	5	-	14	-	-	-	-	-	ns
Input (Control) Capacitance	C_I	-	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	-	-	5	-	42	-	-	-	-	-	pF
HCT TYPES												
Propagation Delay, Switch In to Switch Out	t_{PLH}, t_{PHL}	C_L = 50pF	0	4.5	-	-	12	-	15	-	18	ns
			-4.5	4.5	-	-	8	-	10	-	12	ns
Turn "ON" Time $\overline{E}$ to Out	t_{PZH}	C_L = 50pF	0	4.5	-	-	44	-	55	-	66	ns
			-4.5	4.5	-	-	42	-	53	-	63	ns
		C_L = 15pF	-	5	-	18	-	-	-	-	-	ns
	t_{PZL}	C_L = 50pF	0	4.5	-	-	56	-	70	-	85	ns
			-4.5	4.5	-	-	42	-	53	-	63	ns
		C_L = 15pF	-	5	-	24	-	-	-	-	-	ns
Turn "ON" Time nS to Out	t_{PZH}	C_L = 50pF	0	4.5	-	-	40	-	53	-	60	ns
			-4.5	4.5	-	-	34	-	43	-	51	ns
		C_L = 15pF	-	5	-	17	-	-	-	-	-	ns
	t_{PZL}	C_L = 50pF	0	4.5	-	-	50	-	63	-	75	ns
			-4.5	4.5	-	-	34	-	43	-	51	ns
		C_L = 15pF	-	5	-	18	-	-	-	-	-	ns
Turn "OFF" Time $\overline{E}$ to Out	t_{PLZ}	C_L = 50pF	0	4.5	-	-	50	-	63	-	75	ns
			-4.5	4.5	-	-	46	-	58	-	69	ns
	t_{PLZ}, t_{PHZ}	C_L = 15pF	-	5	-	21	-	-	-	-	-	ns
Turn "OFF" Time nS to Out	t_{PHZ}	C_L = 50pF	0	4.5	-	-	44	-	55	-	66	ns
			-4.5	4.5	-	-	40	-	50	-	60	ns
	t_{PLZ}, t_{PHZ}	C_L = 15pF	-	5	-	18	-	-	-	-	-	ns
Input (Control) Capacitance	C_I	-	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	-	-	5	-	47	-	-	-	-	-	pF

NOTES:

3. C_{PD} is used to determine the dynamic power consumption, per package.

4. $P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L + C_S) V_{CC}^2 f_o$ where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, C_S = switch capacitance, V_{CC} = supply voltage.

Analog Channel Specifications T_A = 25°C

PARAMETER	TEST CONDITIONS	V_{CC} (V)	HC4316	CD74HCT4316	UNITS
Switch Frequency Response Bandwidth at -3dB (Figure 6)	Figure 9 (Notes 5, 6)	4.5	>200	>200	MHz
Crosstalk Between Any Two Switches (Figure 7)	Figure 8 (Notes 6, 7)	4.5	TBE	TBE	dB

Analog Channel Specifications $T_A = 25^oC$ **(Continued)**

PARAMETER	TEST CONDITIONS	V_{CC} (V)	HC4316	CD74HCT4316	UNITS
Total Harmonic Distortion	1kHz, $V_{IS} = 4V_{P-P}$ (Figure 10)	4.5	0.078	0.078	%
	1kHz, $V_{IS} = 8V_{P-P}$ (Figure 10)	9	0.018	0.018	%
Control to Switch Feedthrough Noise	Figure 11	4.5	TBE	TBE	mV
		9	TBE	TBE	mV
Switch "OFF" Signal Feedthrough (Figure 7)	Figure 12 (Notes 6, 7)	4.5	-62	-62	dB
Switch Input Capacitance, C_S	-	-	5	5	pF

NOTES:

5. Adjust input level for 0dBm at output, f = 1MHz.

6. V_{IS} is centered at $V_{CC}/2$.

7. Adjust input for 0dBm at V_{IS}.

Typical Performance Curves
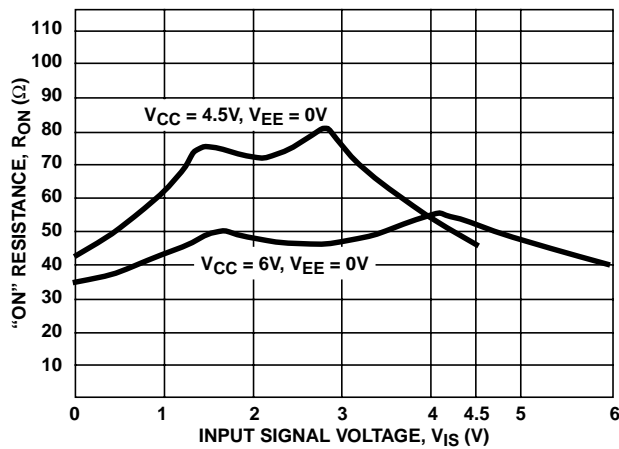
FIGURE 4. TYPICAL "ON" RESISTANCE vs INPUT SIGNAL VOLTAGE
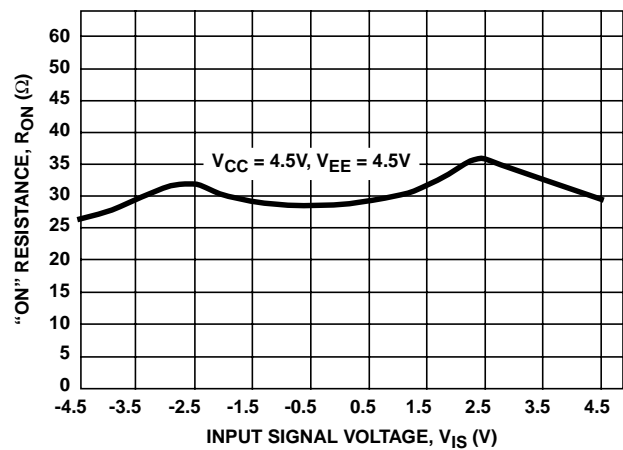
FIGURE 5. TYPICAL "ON" RESISTANCE vs INPUT SIGNAL VOLTAGE
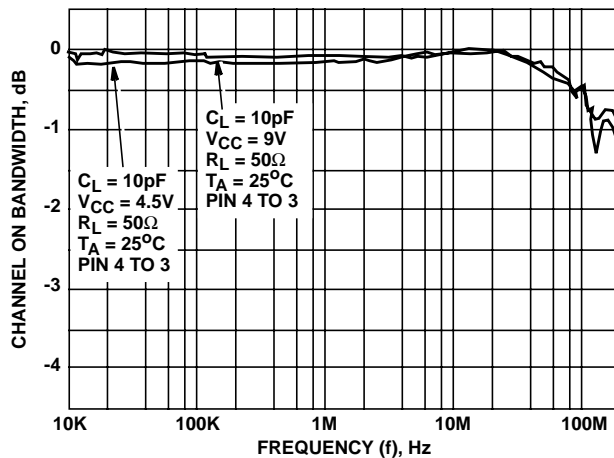
FIGURE 6. SWITCH FREQUENCY RESPONSE
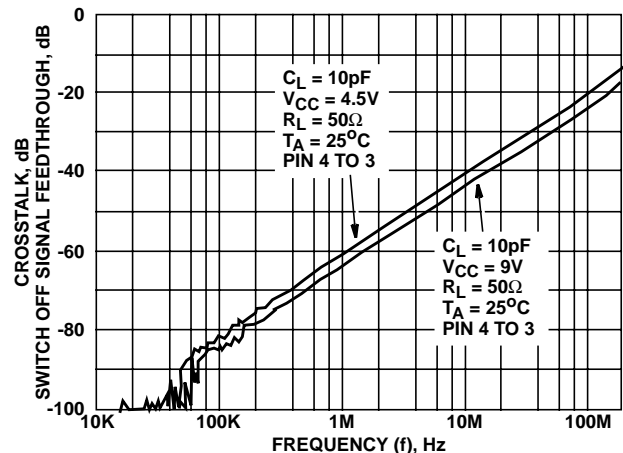
FIGURE 7. SWITCH-OFF SIGNAL FEEDTHROUGH AND CROSSTALK vs FREQUENCY

7

Analog Test Circuits

f_{IS} = 1MHz SINEWAVE
R = 50Ω
C = 10pF
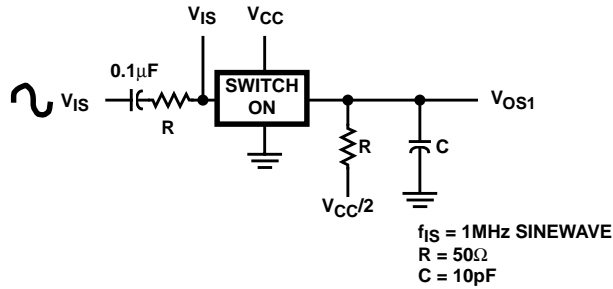
FIGURE 8. CROSSTALK BETWEEN TWO SWITCHES TEST CIRCUIT

FIGURE 9. FREQUENCY RESPONSE TEST CIRCUIT

f_{IS} = 1kHz TO 10kHz
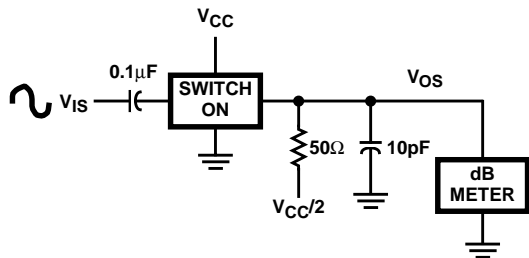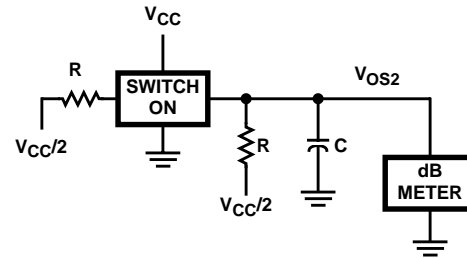
FIGURE 10. TOTAL HARMONIC DISTORTION TEST CIRCUIT
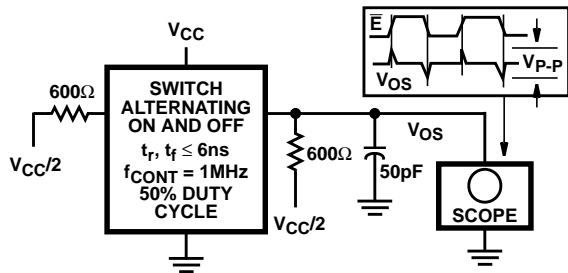
FIGURE 11. CONTROL-TO-SWITCH FEEDTHROUGH NOISE TEST CIRCUIT

$f_{IS} \geq$ 1MHz SINEWAVE
R = 50Ω
C = 10pF
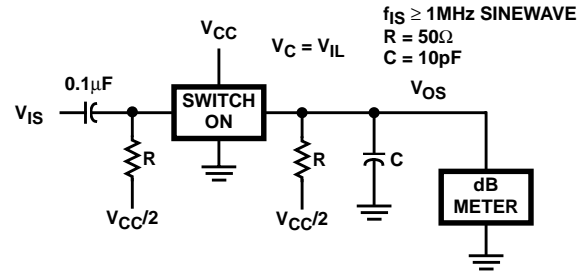
FIGURE 12. SWITCH OFF SIGNAL FEEDTHROUGH

Test Circuits and Waveforms
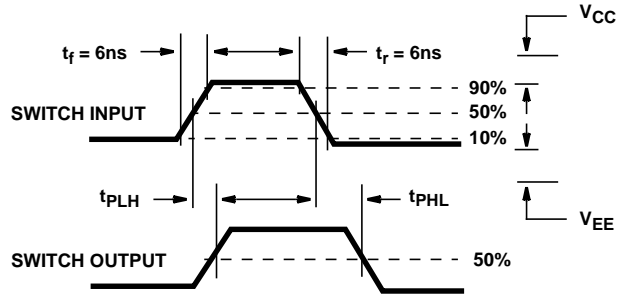
FIGURE 13. SWITCH PROPAGATION DELAY TIMES
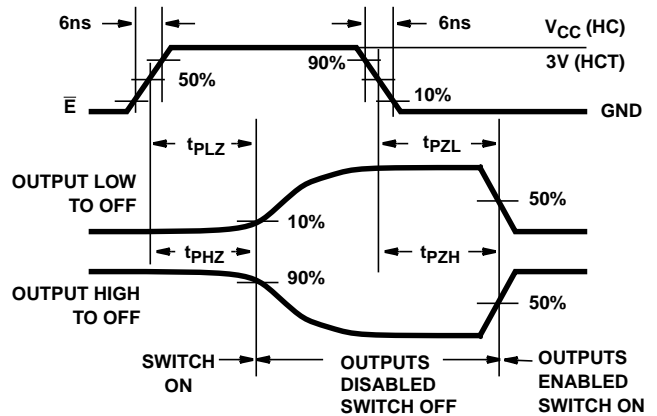
FIGURE 14. SWITCH TURN-ON AND TURN-OFF
PROPAGATION DELAY TIMES WAVEFORMS
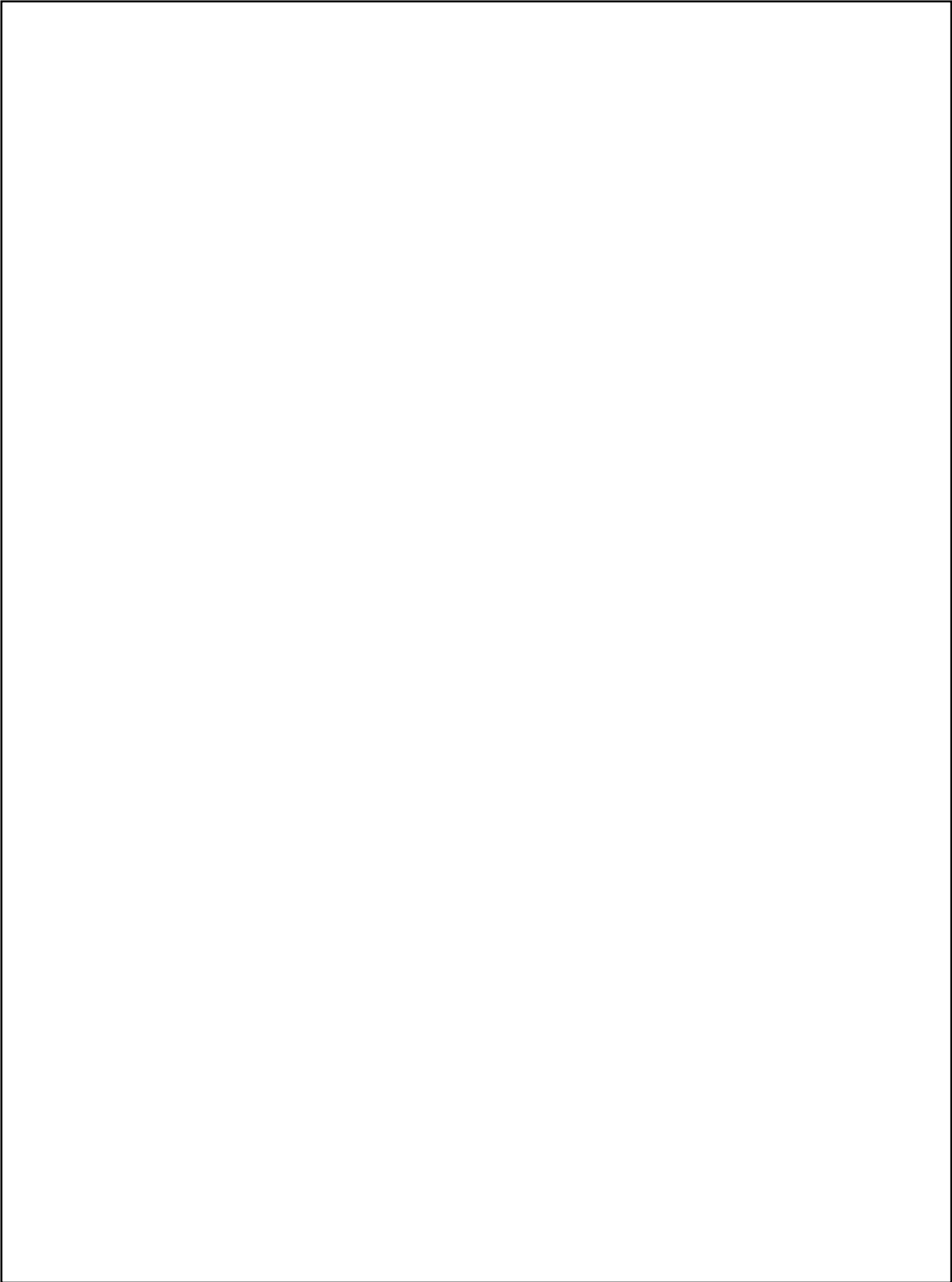
PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
CD54HC4316F3A	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD74HC4316E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC4316EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC4316M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316PWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316PWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4316E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CD74HCT4316EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HCT4316M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4316M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4316M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4316M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4316ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4316MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4316MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4316MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4316MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4316M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4316NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD74HC4316PWR	TSSOP	PW	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
CD74HCT4316M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4316M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HC4316NSR	SO	NS	16	2000	346.0	346.0	33.0
CD74HC4316PWR	TSSOP	PW	16	2000	346.0	346.0	29.0
CD74HCT4316M96	SOIC	D	16	2500	333.2	345.9	28.6

MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

	PINS **	14	16	20	24
DIM					
A MAX		10,50	10,50	12,90	15,30
A MIN		9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

| PINS ** | | | | | | |
DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
        D. Falls within JEDEC MO-153

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

DIM / PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

$\dfrac{0.065\ (1,65)}{0.045\ (1,14)}$

0.005 (0,13) MIN

$\dfrac{0.060\ (1,52)}{0.015\ (0,38)}$

A

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

$\dfrac{0.026\ (0,66)}{0.014\ (0,36)}$

0.100 (2,54)

$\dfrac{0.014\ (0,36)}{0.008\ (0,20)}$

0°–15°

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

D (R−PDSO−G16) PLASTIC SMALL−OUTLINE PACKAGE
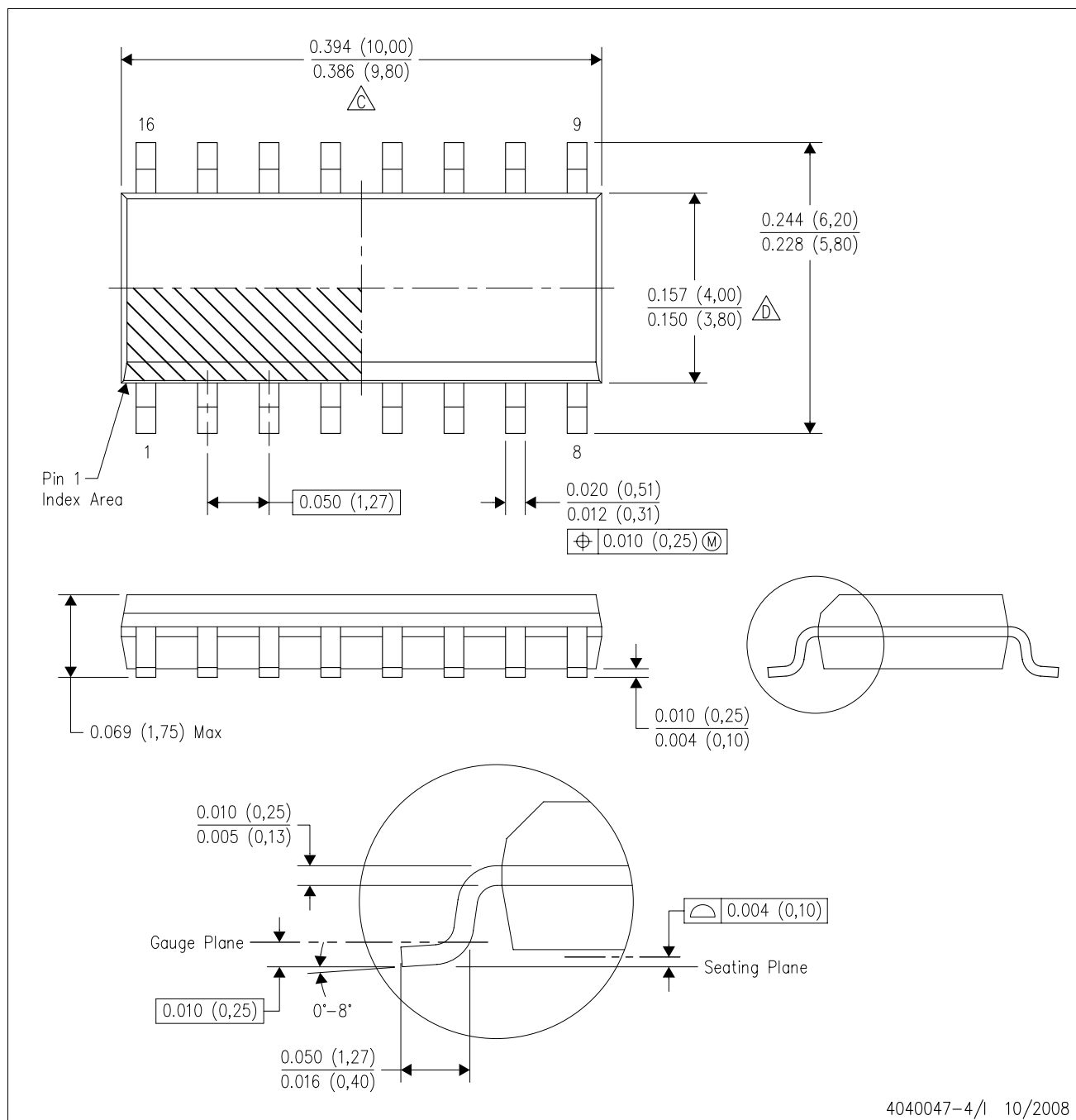
0.394 (10,00)
0.386 (9,80)
⟨C⟩

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) ⟨D⟩

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−4/I 10/2008

NOTES: A. All linear dimensions are in inches (millimeters).
  B. This drawing is subject to change without notice.
  ⟨C⟩ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  ⟨D⟩ Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  E. Reference JEDEC MS−012 variation AC.

N (R-PDIP-T**)
16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

0.260 (6,60)
0.240 (6,10)

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
        D. The 20 pin end lead shoulder width is a vendor option, either half or full width.