

Data sheet acquired from Harris Semiconductor SCHS212D

February 1998 - Revised October 2003

# High-Speed CMOS Logic Quad Analog Switch with Level Translation

### **Features**

- Fast Switching and Propagation Delay Times
- Low "OFF" Leakage Current
- · Built-In "Break-Before-Make" Switching
- Logic-Level Translation to Enable 5V Logic to Accommodate ±5V Analog Signals
- Wide Operating Temperature Range ... -55°C to 125°C
- HC Types
  - 2V to 10V Operation
  - High Noise Immunity:  $N_{IL}$  = 30%,  $N_{IH}$  = 30% of  $V_{CC}$  at  $V_{CC}$  = 5V
- HCT Types
  - Direct LSTTL Input Logic Compatibility,
    V<sub>IL</sub>= 0.8V (Max), V<sub>IH</sub> = 2V (Min)
  - CMOS Input Compatibility,  $I_I \le 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Description

The 'HC4316 and CD74HCT4316 contain four independent digitally controlled analog switches that use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

In addition these devices contain logic-level translation circuits that provide for analog signal switching of voltages between  $\pm 5 \text{V}$  via 5V logic. Each switch is turned on by a high-level voltage on its select input (S) when the common Enable (E) is Low. A High E disables all switches. The digital inputs can swing between VCC and GND; the analog inputs/outputs can swing between VCC as a positive limit and VEE as a negative limit. Voltage ranges are shown in Figures 2 and 3.

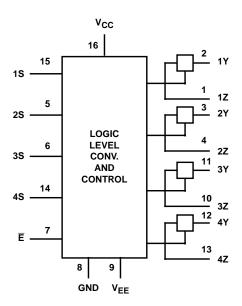
### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC4316F3A	-55 to 125	16 Ld CERDIP
CD74HC4316E	-55 to 125	16 Ld PDIP
CD74HC4316M	-55 to 125	16 Ld SOIC
CD74HC4316MT	-55 to 125	16 Ld SOIC
CD74HC4316M96	-55 to 125	16 Ld SOIC
CD74HC4316NSR	-55 to 125	16 Ld SOP
CD74HC4316PW	-55 to 125	16 Ld TSSOP
CD74HC4316PWR	-55 to 125	16 Ld TSSOP
CD74HC4316PWT	-55 to 125	16 Ld TSSOP
CD74HCT4316E	-55 to 125	16 Ld PDIP
CD74HCT4316M	-55 to 125	16 Ld SOIC
CD74HCT4316MT	-55 to 125	16 Ld SOIC
CD74HCT4316M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

**Pinout** CD54HC4316 (CERDIP) CD74HC4316 (PDIP, SOIC, SOP, TSSOP) CD74HCT4316 (PDIP, SOIC) TOP VIEW 16 V<sub>CC</sub> 1Z 1 15 1S 14 4S 2Y 3 13 4Z 2Z T4 2S 5 12 4Y 11 3Y 3S 6 E 7 10 3Z GND 8 9 V<sub>EE</sub>

# Functional Diagram



**TRUTH TABLE** 

INP	UTS	
Ē	S	SWITCH
L	L	OFF
L	Н	ON
Н	Х	OFF

H= High Level Voltage L= Low Level Voltage

X= Don't Care

# Logic Diagram

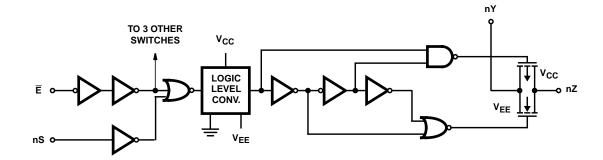


FIGURE 1. ONE SWITCH

### **Absolute Maximum Ratings**

DC Supply Voltage, V <sub>CC</sub> 0.5V to 7V
DC Supply Voltage, V <sub>CC</sub> - V <sub>EE</sub> 0.5V to 10.5V
DC Supply Voltage, V <sub>EE</sub> 0.5V to -7V
DC Input Diode Current, I <sub>IK</sub>
For $V_I < -0.5V$ or $V_I > V_{CC} \ 0.5V$ ±20mA
DC Switch Diode Current, IOK
For V <sub>I</sub> < V <sub>EE</sub> -0.5V or V <sub>I</sub> < V <sub>CC</sub> + 0.5V±25mA
DC Switch Diode Current
For $V_I > V_{EE}$ -0.5V or $V_I < V_{CC} + 0.5V$ ±25mA
DC Output Diode Current, IOK
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ ±20mA
DC Output Source or Sink Current per Output Pin, IO
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ ±25mA
DC V <sub>CC</sub> or Ground Current, I <sub>CC</sub>

### **Thermal Information**

Package Thermal Impedance, θ <sub>JA</sub> (see Note 1):	
E (PDIP) Package67°C	C/W
M (SOIC) Package73°C	C/W
NS (SOP) Package64°C	C/W
PW (TSSOP) Package108°C	C/W
Maximum Junction Temperature (Plastic Package) 1	50 <sup>0</sup>
Maximum Storage Temperature Range65°C to 1	50 <sup>0</sup>
Maximum Lead Temperature (Soldering 10s)	00°
SOIC - Lead Tips Only	

### **Operating Conditions**

Temperature Range, T <sub>A</sub>	-55°C to 125°C
Supply Voltage Range, V <sub>CC</sub>	
HC Types	2V to 6V
HCT Types	4.5V to 5.5V
Supply Voltage Range, V <sub>CC -</sub> V <sub>EE</sub>	
HC, HCT Types (Figure 2)	2V to 10V
Supply Voltage Range, VEE	
HC, HCT Types (Figure 3)	0V to -6V
DC Input or Output Voltage, V <sub>1</sub>	GND to V <sub>CC</sub>
Analog Switch I/O Voltage, V <sub>IS</sub>	V <sub>EE</sub> (Min)
Input Rise and Fall Time, t <sub>r</sub> , t <sub>f</sub>	
2V	. 1000ns (Max)
4.5V	500ns (Max)
6V	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

#### NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

# **Recommended Operating Area as a Function of Supply Voltage**

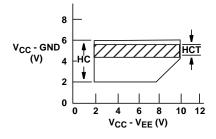


FIGURE 2.

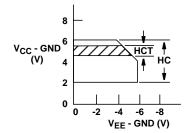


FIGURE 3.

# **DC Electrical Specifications**

			TEST CO	NDITIONS			25°C			C TO C	-55°C TO 125°C		
PARAMETER	SYMBOL	V <sub>I</sub> (V)	V <sub>IS</sub> (V)	V <sub>EE</sub> (V)	V <sub>CC</sub> (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES													
High Level Input	V <sub>IH</sub>	-	-	-	2	1.5	-	-	1.5	-	1.5	-	V
Voltage					4.5	3.15	-	-	3.15	-	3.15	-	V
					6	4.2	-	-	4.2	-	4.2	-	٧
Low Level Input	V <sub>IL</sub>	-	-	-	2	-	-	0.5	-	0.5	-	0.5	V
Voltage					4.5	-	-	1.35	-	1.35	-	1.35	٧
					6	-	-	1.8	-	1.8	-	1.8	٧
"ON" Resistance	R <sub>ON</sub>	V <sub>IH</sub> or	V <sub>CC</sub> or	0	4.5	-	45	180	-	225	-	270	Ω
I <sub>O</sub> = 1mA (Figures 4, 5)		V <sub>IL</sub>	V <sub>EE</sub>	0	6	-	35	160	-	200	-	240	Ω
				-4.5	4.5	-	30	135	-	170	-	205	Ω
			V <sub>CC</sub> to	0	4.5	-	85	320	-	400	-	480	Ω
			V <sub>EE</sub>	0	6	-	55	240	-	300	-	360	Ω
				-4.5	4.5	-	35	170	-	215	-	255	Ω
Maximum "ON"	ΔR <sub>ON</sub>	-	-	0	4.5	-	10	-	-	-	-	-	Ω
Resistance Between Any Two Channels				0	6	-	8.5	-	-	-	-	-	Ω
,				-4.5	4.5	-	5	-	-	-	-	-	Ω
Switch Off Leakage	I <sub>IZ</sub>	V <sub>IH</sub> or	V <sub>CC</sub> -	0	6	-	-	±0.1	-	±1	-	±1	μΑ
Current		V <sub>IL</sub>	V <sub>EE</sub>	-5	5	-	-	±0.1	-	±1	-	±1	μΑ
Control Input Leakage Current	I <sub>IL</sub>	V <sub>CC</sub> or GND	-	0	6	-	-	±0.1	-	±1	-	±1	μА
Quiescent Device	Icc	V <sub>CC</sub> or	When	0	6	-	-	8	1	80	-	160	μА
Current I <sub>O</sub> = 0		GND	V <sub>IS</sub> = V <sub>EE</sub> , V <sub>OS</sub> =V <sub>CC</sub>	-5	5	-	-	16	-	160	-	320	μА
			When V <sub>IS</sub> =V <sub>CC</sub> , V <sub>OS</sub> =V <sub>EE</sub>										
HCT TYPES													
High Level Input Voltage	V <sub>IH</sub>	-	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	٧
"ON" Resistance	R <sub>ON</sub>	V <sub>IH</sub> or	V <sub>CC</sub> or	0	4.5	-	45	180	-	225	-	270	Ω
I <sub>O</sub> = 1mA (Figures 4, 5)		V <sub>IL</sub>	V <sub>EE</sub>	-4.5	4.5	-	30	135	-	170	-	205	Ω
, , , ,			V <sub>CC</sub> to	0	4.5	-	85	320	-	400	-	480	Ω
			V <sub>EE</sub>	-4.5	4.5	-	35	170	-	215	-	255	Ω
Maximum "ON"	ΔR <sub>ON</sub>	-	-	0	4.5	-	10	-	-	-	-	-	Ω
Resistance Between Any Two Channels				-4.5	4.5	-	5	-	-	-	-	-	Ω
Switch Off Leakage	I <sub>IZ</sub>	V <sub>IH</sub> or	V <sub>CC</sub> -	0	6	-	-	±0.1	-	±1	-	±1	μА
Current		V <sub>IL</sub>	VEE	-5	5	-	-	±0.1	-	±1	-	±1	μΑ

# DC Electrical Specifications (Continued)

		TEST CONDITIONS				25°C			-40°C TO 85°C		-55°C TO 125°C		
PARAMETER	SYMBOL	V <sub>I</sub> (V)	V <sub>IS</sub> (V)	V <sub>EE</sub> (V)	V <sub>CC</sub> (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
Control Input Leakage Current	lį	V <sub>CC</sub> or GND	-	0	5.5	-	-	±0.1	-	±1	-	±1	μА
Quiescent Device	I <sub>CC</sub>	Any	When	0	5.5	-	-	8	-	80	-	160	μΑ
Current I <sub>O</sub> = 0		Be- tween V <sub>CC</sub> and GND	$\begin{array}{l} V_{IS} = V_{EE}, \\ V_{OS} = \\ V_{CC}, \\ When \\ V_{IS} = V_{CC}, \\ V_{OS} = V_{EE} \end{array}$	-4.5	5.5	•	-	16	-	160	-	320	μА
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	$\Delta I_{CC}$ (Note 2)	V <sub>CC</sub> -2.1	-	-	4.5 to 5.5		100	360	ı	450	ı	490	μА

#### NOTE:

# **HCT Input Loading Table**

INPUT	UNIT LOADS
All	0.5

NOTE: Unit Load is  $\Delta I_{CC}$  limit specified in DC Electrical Table, e.g., 360 $\mu$ A max at 25°C.

# **Switching Specifications** Input t<sub>r</sub>, t<sub>f</sub> = 6ns

		TEST	V <sub>EE</sub>	V <sub>CC</sub> 25°C			C TO °C		C TO 5°C			
PARAMETER	SYMBOL	CONDITIONS	(V)	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES												
Propagation Delay,	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	0	2	-	-	60	ı	75	-	90	ns
Switch In to Out			0	4.5	-	-	12	i	15	ı	18	ns
			0	6	-	-	10	i	13	ı	15	ns
			-4.5	4.5	-	-	8	ı	10	-	12	ns
Turn "ON" Time $\overline{E}$ to Out	t <sub>PZH</sub> , t <sub>PZL</sub>	C <sub>L</sub> = 50pF	0	2	-	-	205	ı	255	-	310	ns
			0	4.5	-	-	41	i	51	ı	62	ns
			0	6	-	-	35	-	43	-	53	ns
			-4.5	4.5	-	-	37	-	47	-	56	ns
		C <sub>L</sub> = 15pF	-	5	-	17	-	-	-	-	-	ns
Turn "ON" Time nS to Out	t <sub>PZH</sub> , t <sub>PZL</sub>	C <sub>L</sub> = 50pF	0	2	-	-	175	-	220	-	265	ns
			0	4.5	-	-	35	-	44	-	53	ns
			0	6	-	-	30	-	37	-	45	ns
			-4.5	4.5	-	-	34	-	43	-	51	ns
		C <sub>L</sub> = 15pF	-	5	-	14	-	-	-	-	-	ns
Turn "OFF" Time E to Out	t <sub>PLZ</sub> , t <sub>PHZ</sub>	C <sub>L</sub> = 50pF	0	2	-	-	205	-	255	-	310	ns
			0	4.5	-	-	41	-	51	-	62	ns
			0	6	-	-	35	-	43	-	53	ns
			-4.5	4.5	-	-	37	-	47	-	56	ns
		C <sub>L</sub> = 15pF	-	5	-	17	-	-	-	-	-	ns

<sup>2.</sup> For dual-supply systems theoretical worst case ( $V_I$  = 2.4V,  $V_{CC}$  = 5.5V) specification is 1.8mA.

# Switching Specifications Input $t_r$ , $t_f$ = 6ns (Continued)

		TEST	V <sub>EE</sub>	v <sub>cc</sub>		25°C			С ТО °С		C TO 5°C	
PARAMETER	SYMBOL	CONDITIONS	(V)	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
Turn "OFF" Time nS to Out	t <sub>PLZ</sub> , t <sub>PHZ</sub>	C <sub>L</sub> = 50pF	0	2	-	-	175	-	220	-	265	ns
			0	4.5	-	-	35	1	44	-	53	ns
			0	6	-	-	30	ı	37	-	45	ns
			-4.5	4.5	-	-	34	1	43	-	51	ns
		C <sub>L</sub> = 15pF	-	5	-	14	-	ı	-	-	ı	ns
Input (Control) Capacitance	C <sub>I</sub>	-	-	-	-	-	10	ı	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C <sub>PD</sub>	-	-	5	-	42	-	-	-	-	-	pF
HCT TYPES												
Propagation Delay,	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	0	4.5	-	-	12	-	15	-	18	ns
Switch In to Switch Out			-4.5	4.5	-	-	8	-	10	-	12	ns
Turn "ON" Time E to Out	t <sub>PZH</sub>	C <sub>L</sub> = 50pF	0	4.5	-	-	44	-	55	-	66	ns
			-4.5	4.5	-	-	42	-	53	-	63	ns
		C <sub>L</sub> = 15pF	-	5	-	18	-	-	-	-	-	ns
	t <sub>PZL</sub>	C <sub>L</sub> = 50pF	0	4.5	-	-	56	-	70	-	85	ns
			-4.5	4.5	-	-	42	-	53	-	63	ns
		C <sub>L</sub> = 15pF	-	5	-	24	-	-	-	-	-	ns
Turn "ON" Time nS to Out	t <sub>PZH</sub>	C <sub>L</sub> = 50pF	0	4.5	-	-	40	-	53	-	60	ns
			-4.5	4.5	-	-	34	ı	43	-	51	ns
		C <sub>L</sub> = 15pF	-	5	-	17	-	-	-	-	ı	ns
	t <sub>PZL</sub>	C <sub>L</sub> = 50pF	0	4.5	-	-	50	1	63	-	75	ns
			-4.5	4.5	-	-	34	1	43	-	51	ns
		C <sub>L</sub> = 15pF	-	5	-	18	-	ı	-	-	ı	ns
Turn "OFF" Time E to Out	t <sub>PLZ</sub>	C <sub>L</sub> = 50pF	0	4.5	-	-	50	ı	63	-	75	ns
			-4.5	4.5	-	-	46	ı	58	-	69	ns
	t <sub>PLZ</sub> , t <sub>PHZ</sub>	C <sub>L</sub> = 15pF	-	5	-	21	-	-	-	-	-	ns
Turn "OFF" Time nS to Out	t <sub>PHZ</sub>	C <sub>L</sub> = 50pF	0	4.5	-	-	44	-	55	-	66	ns
			-4.5	4.5	-	-	40	-	50	-	60	ns
	t <sub>PLZ</sub> , t <sub>PHZ</sub>	C <sub>L</sub> = 15pF	-	5	-	18	-	-	-	-	-	ns
Input (Control) Capacitance	C <sub>I</sub>	-	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C <sub>PD</sub>	-	-	5	-	47	-	-	-	-	-	pF

#### NOTES:

- 3.  $\ensuremath{\text{C}_{\text{PD}}}$  is used to determine the dynamic power consumption, per package.
- 4.  $P_D = C_{PD} \ V_{CC}^2 \ f_i + \Sigma \ (C_L + C_S) \ V_{CC}^2 \ f_o$  where  $f_i$  = input frequency,  $f_o$  = output frequency,  $C_L$  = output load capacitance,  $C_S$  = switch capacitance,  $V_{CC}$  = supply voltage.

# Analog Channel Specifications $T_A = 25^{\circ}C$

PARAMETER	TEST CONDITIONS	V <sub>CC</sub> (V)	HC4316	CD74HCT4316	UNITS
Switch Frequency Response Bandwidth at -3dB (Figure 6)	Figure 9 (Notes 5, 6)	4.5	>200	>200	MHz
Crosstalk Between Any Two Switches (Figure 7)	Figure 8 (Notes 6, 7)	4.5	TBE	TBE	dB

### Analog Channel Specifications $T_A = 25^{\circ}C$ (Continued)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub> (V)	HC4316	CD74HCT4316	UNITS
Total Harmonic Distortion	1kHz, V <sub>IS</sub> = 4V <sub>P-P</sub> (Figure 10)	4.5	0.078	0.078	%
	1kHz, V <sub>IS</sub> = 8V <sub>P-P</sub> (Figure 10)	9	0.018	0.018	%
Control to Switch Feedthrough Noise	Figure 11	4.5	TBE	TBE	mV
		9	TBE	TBE	mV
Switch "OFF" Signal Feedthrough (Figure 7)	Figure 12 (Notes 6, 7)	4.5	-62	-62	dB
Switch Input Capacitance, C <sub>S</sub>	-	-	5	5	pF

#### NOTES:

- 5. Adjust input level for 0dBm at output, f = 1MHz.
- 6.  $V_{IS}$  is centered at  $V_{CC}/2$ .
- 7. Adjust input for 0dBm at  $V_{IS}$ .

# **Typical Performance Curves**

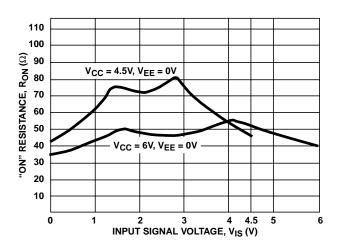


FIGURE 4. TYPICAL "ON" RESISTANCE vs INPUT SIGNAL VOLTAGE

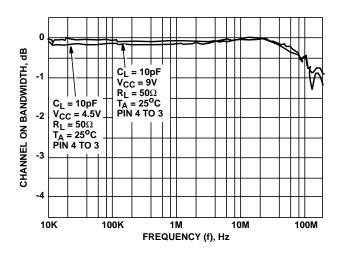


FIGURE 6. SWITCH FREQUENCY RESPONSE

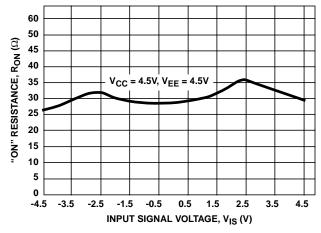


FIGURE 5. TYPICAL "ON" RESISTANCE vs INPUT SIGNAL VOLTAGE

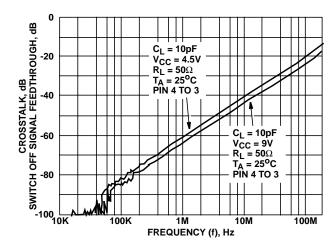
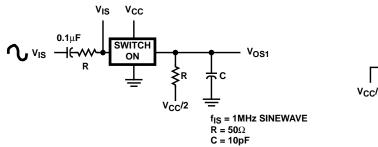


FIGURE 7. SWITCH-OFF SIGNAL FEEDTHROUGH AND CROSSTALK vs FREQUENCY

# **Analog Test Circuits**



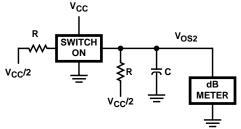


FIGURE 8. CROSSTALK BETWEEN TWO SWITCHES TEST CIRCUIT

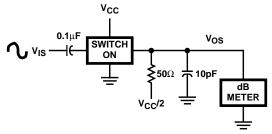


FIGURE 9. FREQUENCY RESPONSE TEST CIRCUIT

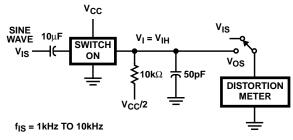


FIGURE 10. TOTAL HARMONIC DISTORTION TEST CIRCUIT

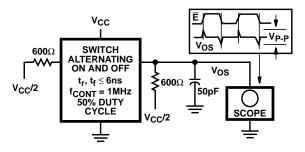


FIGURE 11. CONTROL-TO-SWITCH FEEDTHROUGH NOISE TEST CIRCUIT

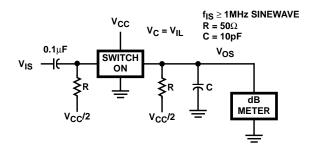


FIGURE 12. SWITCH OFF SIGNAL FEEDTHROUGH

# Test Circuits and Waveforms

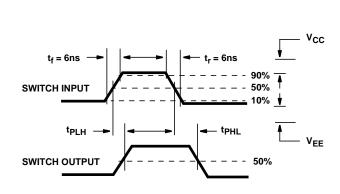


FIGURE 13. SWITCH PROPAGATION DELAY TIMES

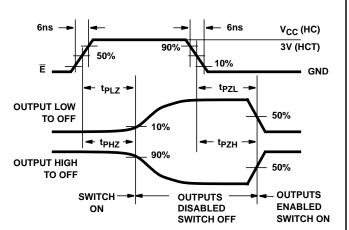
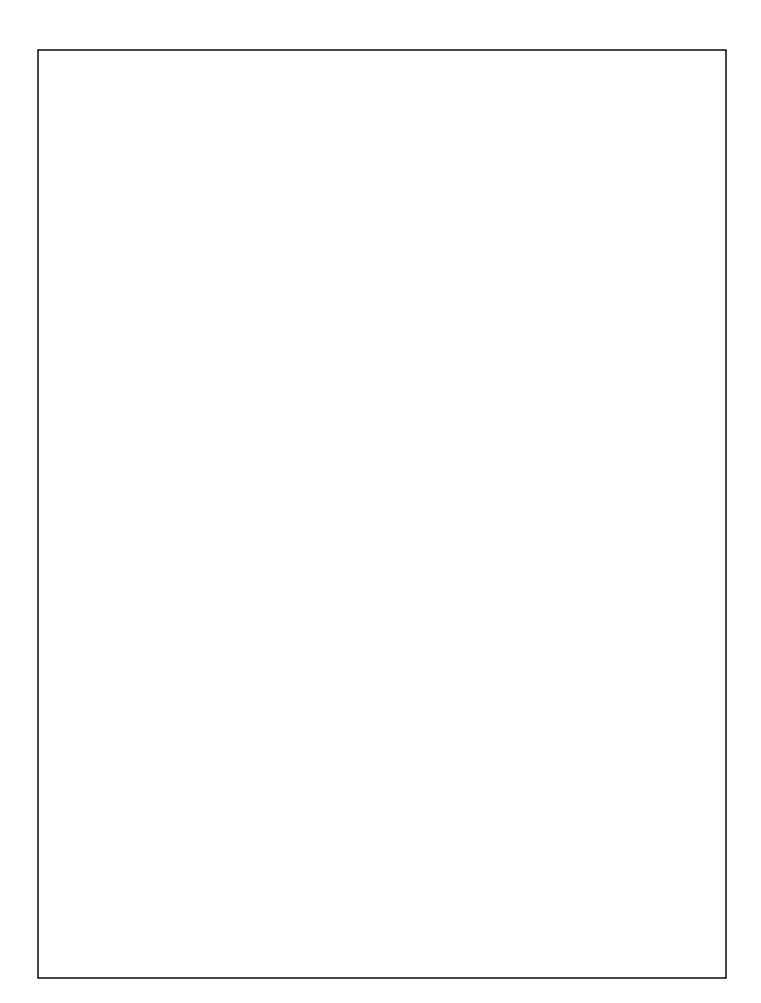


FIGURE 14. SWITCH TURN-ON AND TURN-OFF PROPAGATION DELAY TIMES WAVEFORMS





# **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp (3)
CD54HC4316F3A	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD74HC4316E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC4316EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC4316M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316PWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4316PWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4316E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type





com 18-Sep-2008

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD74HCT4316EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HCT4316M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4316M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4316M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4316M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4316ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4316MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4316MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4316MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4316MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <a href="http://www.ti.com/productcontent">http://www.ti.com/productcontent</a> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

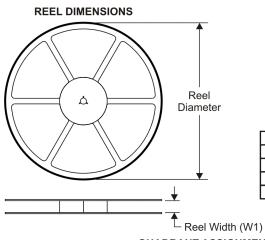
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

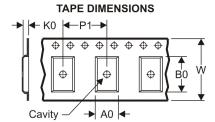
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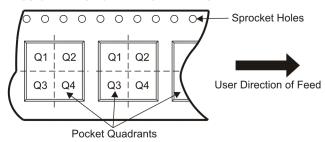
### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

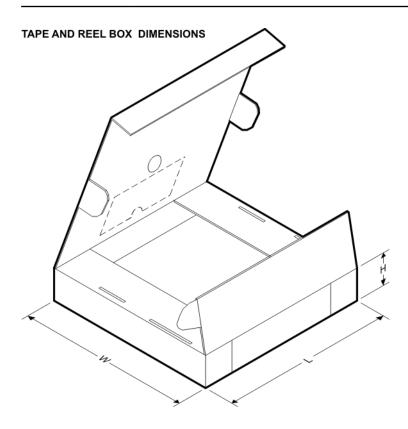
# QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4316M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4316NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD74HC4316PWR	TSSOP	PW	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
CD74HCT4316M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1





\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4316M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HC4316NSR	SO	NS	16	2000	346.0	346.0	33.0
CD74HC4316PWR	TSSOP	PW	16	2000	346.0	346.0	29.0
CD74HCT4316M96	SOIC	D	16	2500	333.2	345.9	28.6

# **MECHANICAL DATA**

# NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

### PLASTIC SMALL-OUTLINE PACKAGE



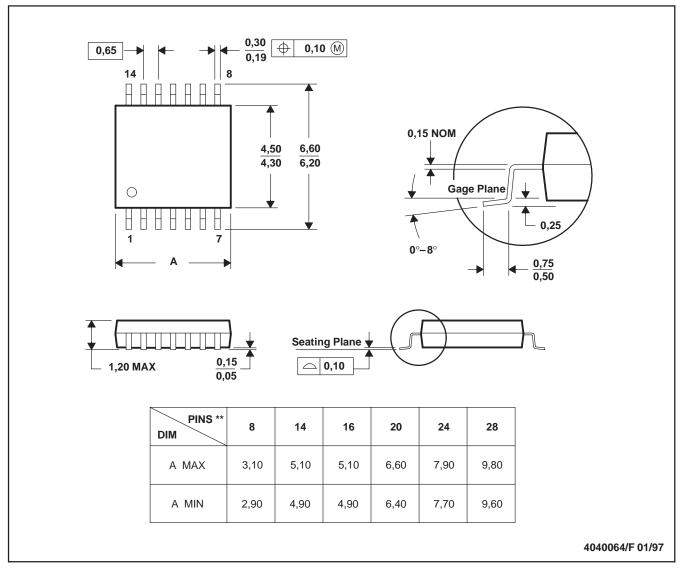
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



# PW (R-PDSO-G\*\*)

### 14 PINS SHOWN

# PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

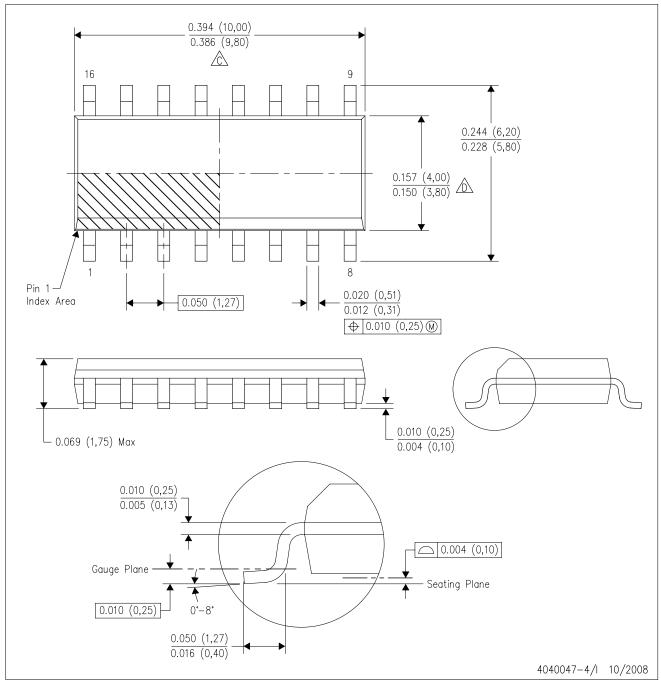
### 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# D (R-PDSO-G16)

# PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AC.



# N (R-PDIP-T\*\*)

# PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



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