

F

E

D

C

B

A

F

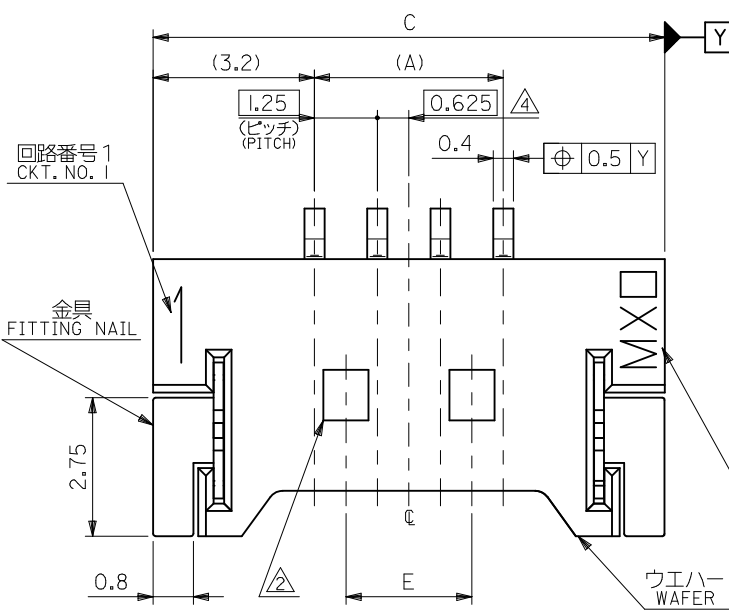
E

D

C

B

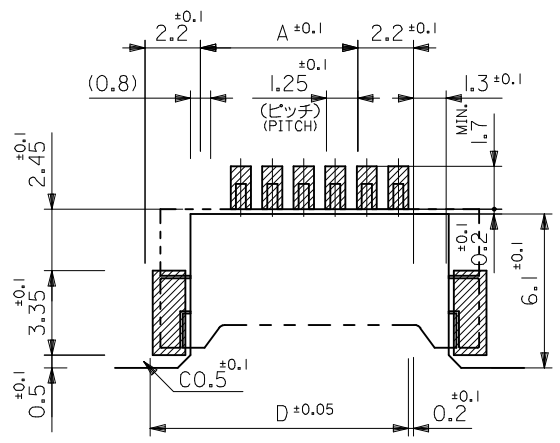
A



注記 NOTES

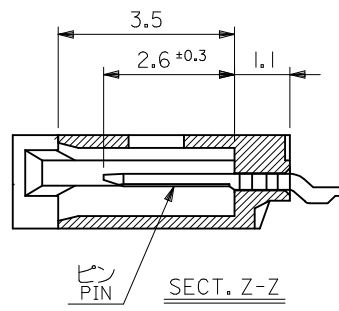
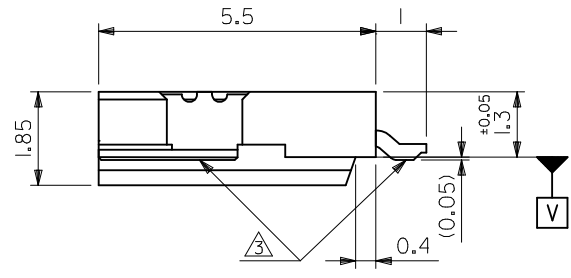
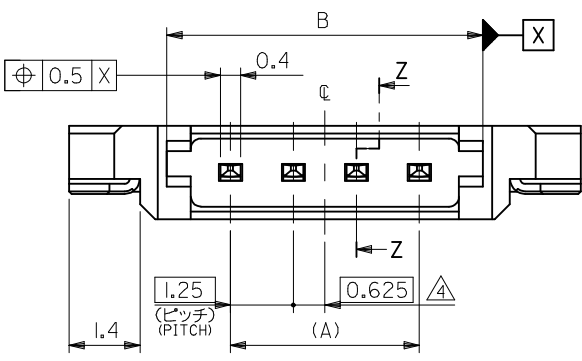
1. 嵌合相手: 51146 シリーズ
MATES WITH: 51146 SERIES
2. ロック窓は2、3極品は1箇所、4極品以上は2箇所とする。
LOCKING WINDOW: ONE PLACE FOR 2 AND 3 CIRCUIT PRODUCTS
AND TWO PLACES FOR MORE THAN 3 CIRCUIT PRODUCTS.
3. 基準面 ∇ からのソルダーテールと金具の半田付け面のズレ量は、
上方に 0.05MAX. 下方に 0.15MAX. とし、
相互のパラッキ量は 0.1MAX. とする。
MISALIGNMENT OF SOLDER TAIL AND FITTING NAIL FROM ∇
: UPPER DIRECTION 0.05MAX.
: LOWER DIRECTION 0.15MAX.
: OFFSET BETWEEN UPPER AND LOWER 0.1MAX.
4. 偶数極の製品に適用。
APPLY EVEN CIRCUIT PRODUCTS.
5. 材質 MATERIAL
ウエハー: WAFER: PPHS, UL94V-0
ピン: リン青銅 (コンタクト部: 金メッキ、テール部: 半田メッキ)
PIN: PHOS-BRO (CONTACT: Au PLATING, TAIL: Sn-Pb PLATING)
金具: リン青銅 (半田メッキ)
FITTING NAIL: PHOS-BRO (Sn-Pb PLATING)

トレードマーク
TRADE MARK

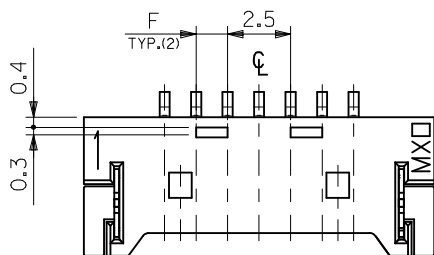


参考基板レイアウト
RECOMMENDED P.C.BOARD PATTERN DIM. (REF.)

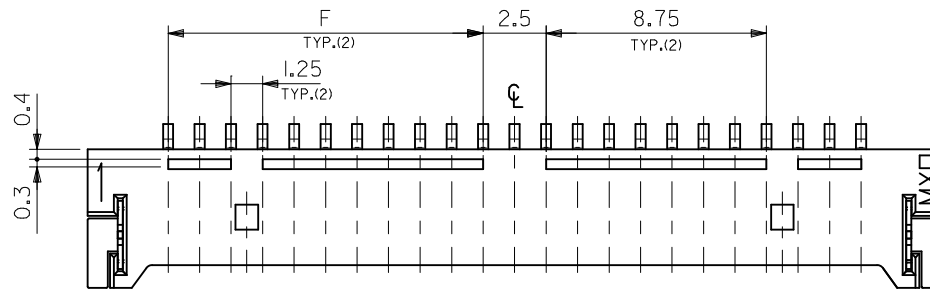
16.25	22.5	40.25	42.65	38.77	36.25	53779-3010	30
15	22.5	37.75	40.15	36.27	33.75	-2810	28
13.75	22.5	35.25	37.65	33.77	31.25	-2610	26
12.5	22.5	32.75	35.15	31.27	28.75	-2410	24
11.25	22.5	30.25	32.65	28.77	26.25	-2210	22
8.75	22.5	27.75	30.15	26.27	23.75	-2010	20
7.5	20	25.25	27.65	23.77	21.25	-1810	18
6.25	17.5	22.75	25.15	21.27	18.75	-1610	16
6.25	16.25	21.5	23.9	20.02	17.5	-1510	15
5	15	20.25	22.65	18.77	16.25	-1410	14
3.75	12.5	17.75	20.15	16.27	13.75	-1210	12
2.5	8.75	14	16.4	12.52	10	-0910	9
1.25	7.5	12.75	15.15	11.27	8.75	-0810	8
--	5	10.25	12.65	8.77	6.25	-0610	6
--	3.75	9	11.4	7.52	5	-0510	5
--	2.5	7.75	10.15	6.27	3.75	-0410	4
--	--	6.5	8.9	5.02	2.5	-0310	3
--	--	5.25	7.65	3.77	1.25	53779-0210	2
F	E	D	C	B	A	MATERIAL NO.	CKT. 極数



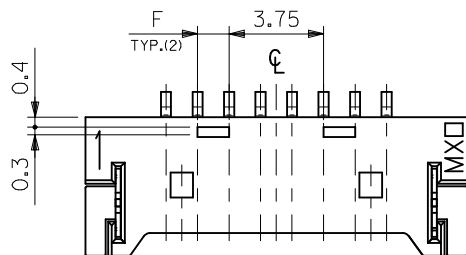
REVISED EC NO: J2008-4402 DRWN: MAKURAA CHKD: T. HARIYAMA APPR: NUKITA REV	DESCRIPTION 2008/07/01 2008/07/01 2008/11/18	GENERAL TOLERANCES (UNLESS SPECIFIED)		DIMENSION STYLE MM ONLY		SCALE ---	DESIGN UNITS METRIC	MODEL NO. 53779-**10	
		10 UNDER ±0.2		DRAWN BY S. MATSUZAKI DATE '01/05/11		TITLE		THIRD ANGLE PROJECTION	
		10 OVER 30 UNDER ±0.25		CHECKED BY T. YAMAGUCHI DATE '01/05/11		7.125 WIRE TO BOARD CONN. WAFER ASSY FOR SMT. (SHEET 1 OF 2)			
		30 OVER ±0.3		APPROVED BY T. YAMAGUCHI DATE '01/05/11		MOLEX INCORPORATED			
		ANGULAR ±3 °		MATERIAL NO.		DOCUMENT NO.		SHEET NO.	
DRAFT WHERE APPLICABLE MUST REMAIN WITHIN DIMENSIONS		SIZE A3		SEE TABLE		SD-53779-003		1 OF 2	
				THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO MOLEX INCORPORATED AND SHOULD NOT BE USED WITHOUT WRITTEN PERMISSION					



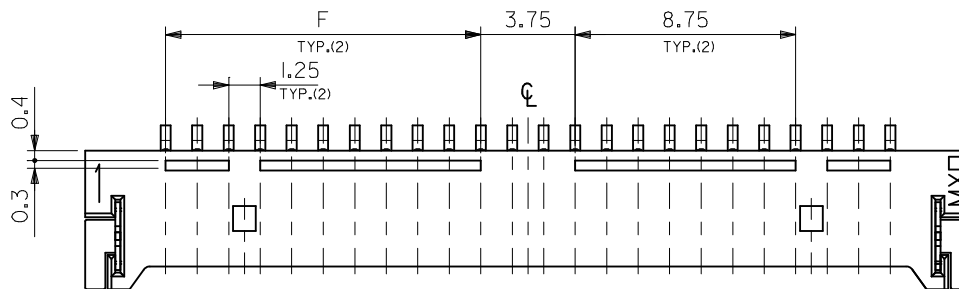
7~19極の奇数極に適用
APPLY FOR ODD CIRCUITS OF 7~19



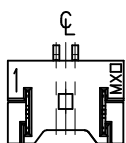
21極以上の奇数極に適用
APPLY FOR ODD CIRCUITS 21~29



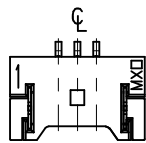
8~20極の偶数極に適用
APPLY FOR EVEN CIRCUITS OF 8~20



22極以上の偶数極に適用
APPLY FOR EVEN CIRCUITS 22~30



2 CKT.



3 CKT.

ロック形状図
LOCK CONFIGURATION

REVISED EC NO: J2008-4402 DRWN: NAKAMURA 2008/07/01 CHKD: T. HARUYAMA 2008/07/01 APPR: NUKITA 2008/11/18	DESCRIPTION	GENERAL TOLERANCES (UNLESS SPECIFIED)		DIMENSION STYLE MM ONLY		SCALE ---	DESIGN UNITS METRIC	THIRD ANGLE PROJECTION
		10 UNDER	± 0.2	DRAWN BY S. MAYSUZAKI	DATE '01/05/11	TITLE 1.25 WIRE TO BOARD CONN. WAFER ASS FOR S.M.T. (SHEET 2 OF 2)		
		10 OVER 30 UNDER	± 0.25	CHECKED BY T. YAMAGUCHI	DATE '01/05/11			
		30 OVER	± 0.3	APPROVED BY T. YAMAGUCHI	DATE '01/05/11	MOLEX INCORPORATED		
		ANGULAR ±3 °		MATERIAL NO.				
	DRAFT WHERE APPLICABLE MUST REMAIN WITHIN DIMENSIONS		SEE TABLE		SD-53779-003		2 OF 2	
	REV	THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO MOLEX INCORPORATED AND SHOULD NOT BE USED WITHOUT WRITTEN PERMISSION						