

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

## TC4017BP, TC4017BF

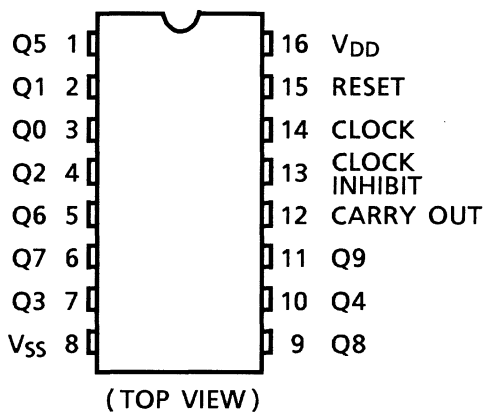
### TC4017BP/TC4017BF Decade Counter/Divider

TC4017BP/BF is decimal Johnson counter consisting of 5 stage D-type flip-flop equipped with the decoder to convert the output to decimal.

Depending on the number of count pulses fed to CLOCK or CLOCK INHIBIT one output among 10 output lines "Q0" through "Q9" becomes "H" level.

The counter advances its state at rising edge of CLOCK (CLOCK INHIBIT = "L") or falling edge of CLOCK INHIBIT (CLOCK = "H"). RESET input to "H" level resets the counter to Q0 = "H" and Q1 through Q9 = "L" regardless of CLOCK and CLOCK INHIBIT.

### Pin Assignment



### Truth Table

Inputs			Selected Output
CLOCK $\Delta$	CLOCK INHIBIT $\Delta$	RESET	
*	*	H	Q0
*	H	L	Qn (NC)
L	*	L	Qn (NC)
$\uparrow$	L	L	Qn + 1
$\downarrow$	L	L	Qn (NC)
H	$\uparrow$	L	Qn (NC)
H	$\downarrow$	L	Qn + 1

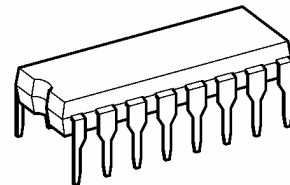
$\Delta$ : Level change

\*: Don't care

NC: No change

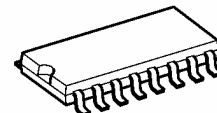
carry out  $\left\{ \begin{array}{l} \text{"H"} \dots \dots \dots \text{Q0} \sim \text{Q4} = \text{"H"} \\ \text{"L"} \dots \dots \dots \text{Q5} \sim \text{Q9} = \text{"H"} \end{array} \right.$

TC4017BP

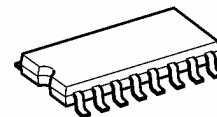


DIP16-P-300-2.54A

TC4017BF



SOP16-P-300-1.27A



SOP16-P-300-1.27

### Weight

DIP16-P-300-2.54A	: 1.00 g (typ.)
SOP16-P-300-1.27A	: 0.18 g (typ.)
SOP16-P-300-1.27	: 0.18 g (typ.)

The logic diagram illustrates a 5-bit ripple-carry adder implemented with D flip-flops. The circuit features five D flip-flops, each with inputs D, S, Q, and Q-bar, and a clock input CK. The flip-flops are arranged in a row, with their Q outputs connected to the D inputs of the next flip-flop in the sequence, creating a ripple effect. The carry-in is provided by the CK input of the first flip-flop. The carry-out of the fifth flip-flop is connected to the CK input of the first flip-flop, forming a feedback loop. The circuit includes several control inputs: CK (13), INHIBIT (14), and RESET (15). The outputs are labeled Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, and CARRY OUT (12). The diagram shows the internal logic of the flip-flops and the connections between them, including the ripple-carry mechanism.

Timing diagram for a 10-bit ripple-carry counter. The diagram shows the waveforms for RESET, CLOCK, CLOCK INHIBIT, and the outputs Q0 through Q9 and CARRY OUT. The counter is initialized to 0000000000. It counts up to 1011111111 (decimal 1023) and then resets to 0000000000. The timing diagram shows that the outputs change at the falling edge of the clock signal. The carry out signal is high when the counter is at 1023 and resets to low when the counter resets to 0.

**Absolute Maximum Ratings (Note)**

Characteristics	Symbol	Rating	Unit
DC supply voltage	$V_{DD}$	$V_{SS} - 0.5 \sim V_{SS} + 20$	V
Input voltage	$V_{IN}$	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
Output voltage	$V_{OUT}$	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
DC input current	$I_{IN}$	$\pm 10$	mA
Power dissipation	$P_D$	300 (DIP)/180 (SOIC)	mW
Operating ambient temperature range	$T_{opr}$	$-40 \sim 85$	$^{\circ}\text{C}$
Storage temperature range	$T_{stg}$	$-65 \sim 150$	$^{\circ}\text{C}$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

**Recommended Operating Conditions ( $V_{SS} = 0\text{ V}$ ) (Note)**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
DC supply voltage	$V_{DD}$	—	3	—	18	V
Input voltage	$V_{IN}$	—	0	—	$V_{DD}$	V

Note: The recommended operating conditions are required to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

**Static Electrical Characteristics ( $V_{SS} = 0$  V)**

Characteristics	Sym- bol	Test Condition	$V_{DD}$ (V)	-40°C		25°C			85°C		Unit
				Min	Max	Min	Typ.	Max	Min	Max	
High-level output voltage	$V_{OH}$	$ I_{OUT}  < 1 \mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	4.95	—	4.95	5.00	—	4.95	—	V
			10	9.95	—	9.95	10.00	—	9.95	—	
			15	14.95	—	14.95	15.00	—	14.95	—	
Low-level output voltage	$V_{OL}$	$ I_{OUT}  < 1 \mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	—	0.05	—	0.00	0.05	—	0.05	V
			10	—	0.05	—	0.00	0.05	—	0.05	
			15	—	0.05	—	0.00	0.05	—	0.05	
Output high current	$I_{OH}$	$V_{OH} = 4.6$ V	5	-0.61	—	-0.51	-1.0	—	-0.42	—	mA
		$V_{OH} = 2.5$ V	5	-2.50	—	-2.10	-4.0	—	-1.70	—	
		$V_{OH} = 9.5$ V	10	-1.50	—	-1.30	-2.2	—	-1.10	—	
		$V_{OH} = 13.5$ V	15	-4.00	—	-3.40	-9.0	—	-2.80	—	
		$V_{IN} = V_{SS}, V_{DD}$									
Output low current	$I_{OL}$	$V_{OL} = 0.4$ V	5	0.61	—	0.51	1.5	—	0.42	—	mA
		$V_{OL} = 0.5$ V	10	1.50	—	1.30	3.8	—	1.10	—	
		$V_{OL} = 1.5$ V	15	4.00	—	3.40	15.0	—	2.80	—	
		$V_{IN} = V_{SS}, V_{DD}$									
Input high voltage	$V_{IH}$	$V_{OUT} = 0.5$ V, 4.5 V	5	3.5	—	3.5	2.75	—	3.5	—	V
		$V_{OUT} = 1.0$ V, 9.0 V	10	7.0	—	7.0	5.50	—	7.0	—	
		$V_{OUT} = 1.5$ V, 13.5 V	15	11.0	—	11.0	8.25	—	11.0	—	
		$ I_{OUT}  < 1 \mu A$									
Input low voltage	$V_{IL}$	$V_{OUT} = 0.5$ V, 4.5 V	5	—	1.5	—	2.25	1.5	—	1.5	V
		$V_{OUT} = 1.0$ V, 9.0 V	10	—	3.0	—	4.50	3.0	—	3.0	
		$V_{OUT} = 1.5$ V, 13.5 V	15	—	4.0	—	6.75	4.0	—	4.0	
		$ I_{OUT}  < 1 \mu A$									
Input current	"H" level	$I_{IH}$	$V_{IH} = 18$ V	18	—	0.1	—	$10^{-5}$	0.1	—	$\mu A$
	"L" level	$I_{IL}$	$V_{IL} = 0$ V	18	—	-0.1	—	$-10^{-5}$	-0.1	—	
Quiescent supply current	$I_{DD}$	$V_{IN} = V_{SS}, V_{DD}$ (Note)	5	—	5	—	0.005	5	—	150	$\mu A$
			10	—	10	—	0.010	10	—	300	
			15	—	15	—	0.015	20	—	600	

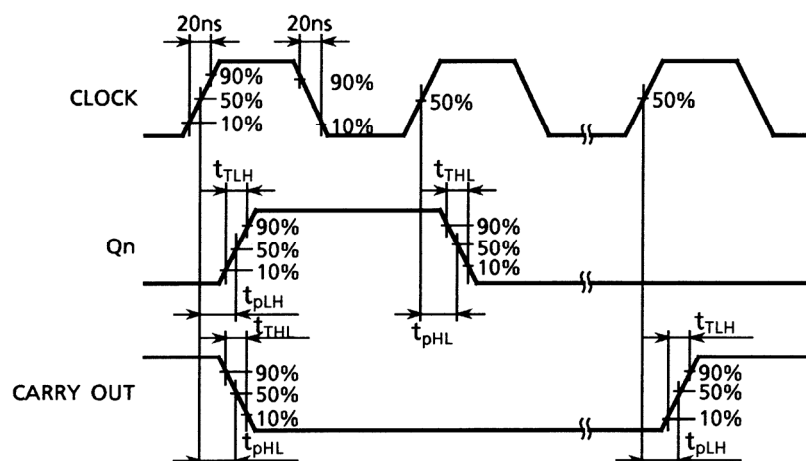
Note: All valid input combinations.

**Dynamic Electrical Characteristics (Ta = 25°C, V<sub>SS</sub> = 0 V, C<sub>L</sub> = 50 pF)**

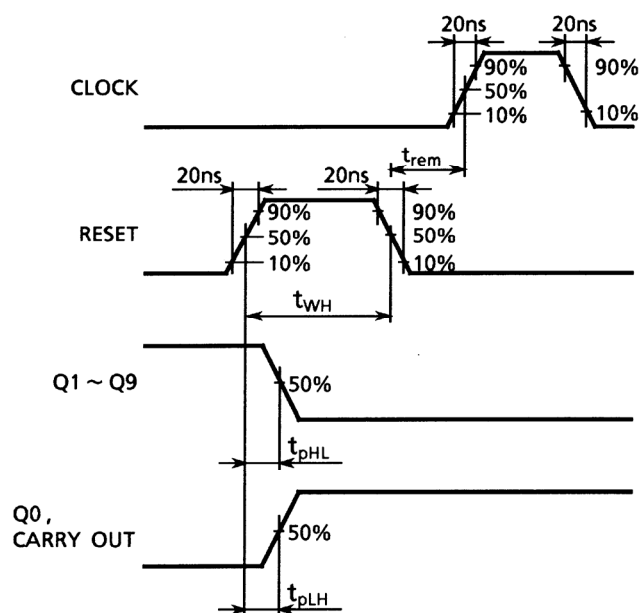
Characteristics	Symbol	Test Condition	V <sub>DD</sub> (V)	Min	Typ.	Max	Unit
Output transition time (low to high)	t <sub>TLH</sub>	—	5	—	80	200	ns
			10	—	50	100	
			15	—	40	80	
Output transition time (high to low)	t <sub>THL</sub>	—	5	—	80	200	ns
			10	—	50	100	
			15	—	40	80	
Propagation delay time (CLOCK-Qn)	t <sub>pLH</sub> t <sub>pHL</sub>	—	5	—	325	650	ns
			10	—	135	270	
			15	—	85	170	
Propagation delay time (CLOCK-CARRY OUT)	t <sub>pLH</sub> t <sub>pHL</sub>	—	5	—	280	600	ns
			10	—	110	250	
			15	—	75	160	
Propagation delay time (RESET-Qn) (RESET-CARRY OUT)	t <sub>pLH</sub> t <sub>pHL</sub>	—	5	—	265	530	ns
			10	—	115	230	
			15	—	85	170	
Max clock frequency	f <sub>CL</sub>	—	5	2.5	6.0	—	MHz
			10	5.0	12.0	—	
			15	6.7	13.5	—	
Min clock pulse width	t <sub>W</sub>	—	5	—	85	200	ns
			10	—	40	90	
			15	—	35	60	
Min pulse width (RESET)	t <sub>WH</sub>	—	5	—	50	260	ns
			10	—	20	110	
			15	—	15	60	
Max clock rise time Max clock fall time	t <sub>rCL</sub> t <sub>fCL</sub>	—	5	No limit			μs
			10				
			15				
Min set-up time (CLOCK INHIBIT-CLOCK)	t <sub>SU</sub>	—	5	—	30	230	ns
			10	—	15	100	
			15	—	10	70	
Min removal time (RESET-CLOCK)	t <sub>rem</sub>	—	5	—	-55	400	ns
			10	—	-20	275	
			15	—	-15	150	
Input capacitance	C <sub>IN</sub>	—		—	5	7.5	pF

## Waveforms for Measurement of Dynamic Characteristics

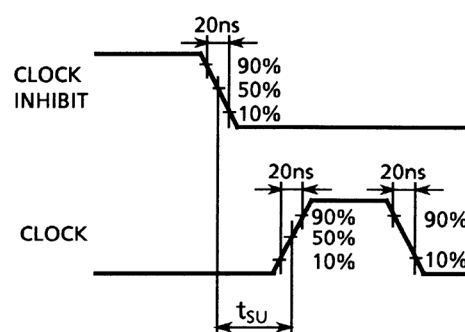
Waveform 1



Waveform 2



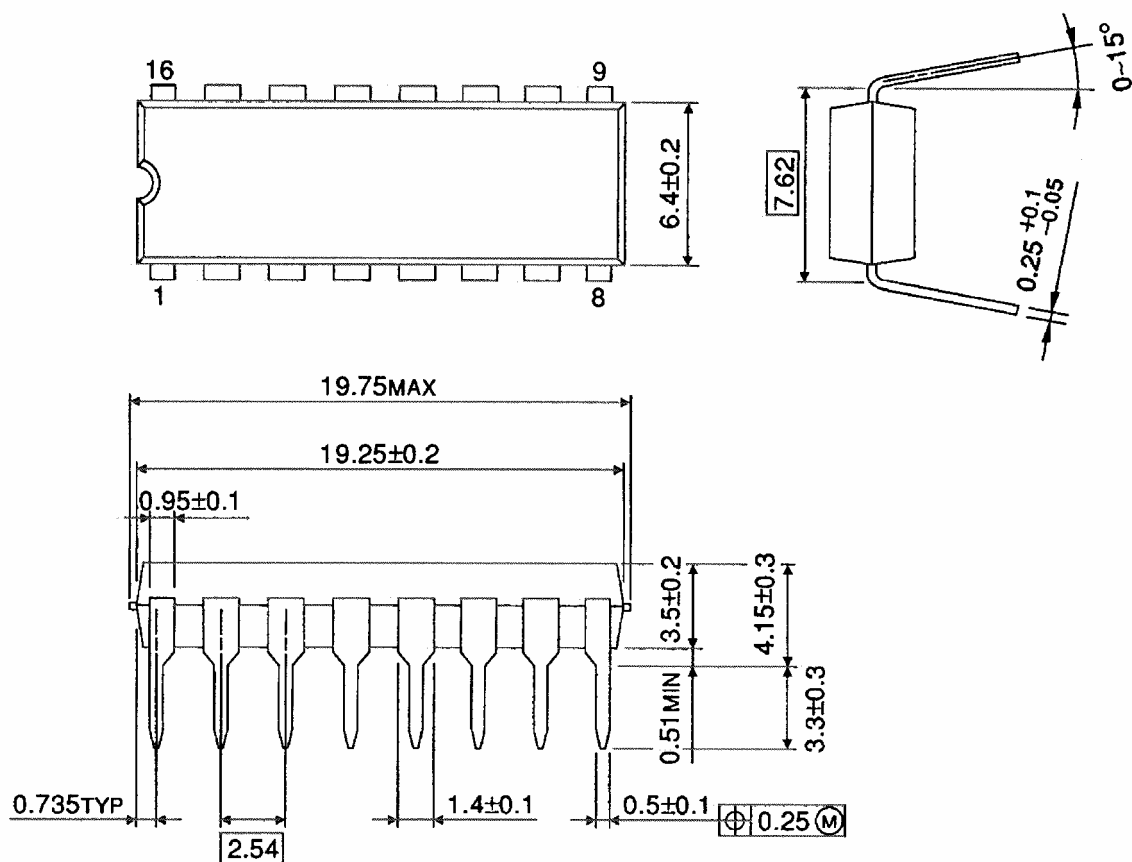
Waveform 3



## Package Dimensions

DIP16-P-300-2.54A

Unit : mm

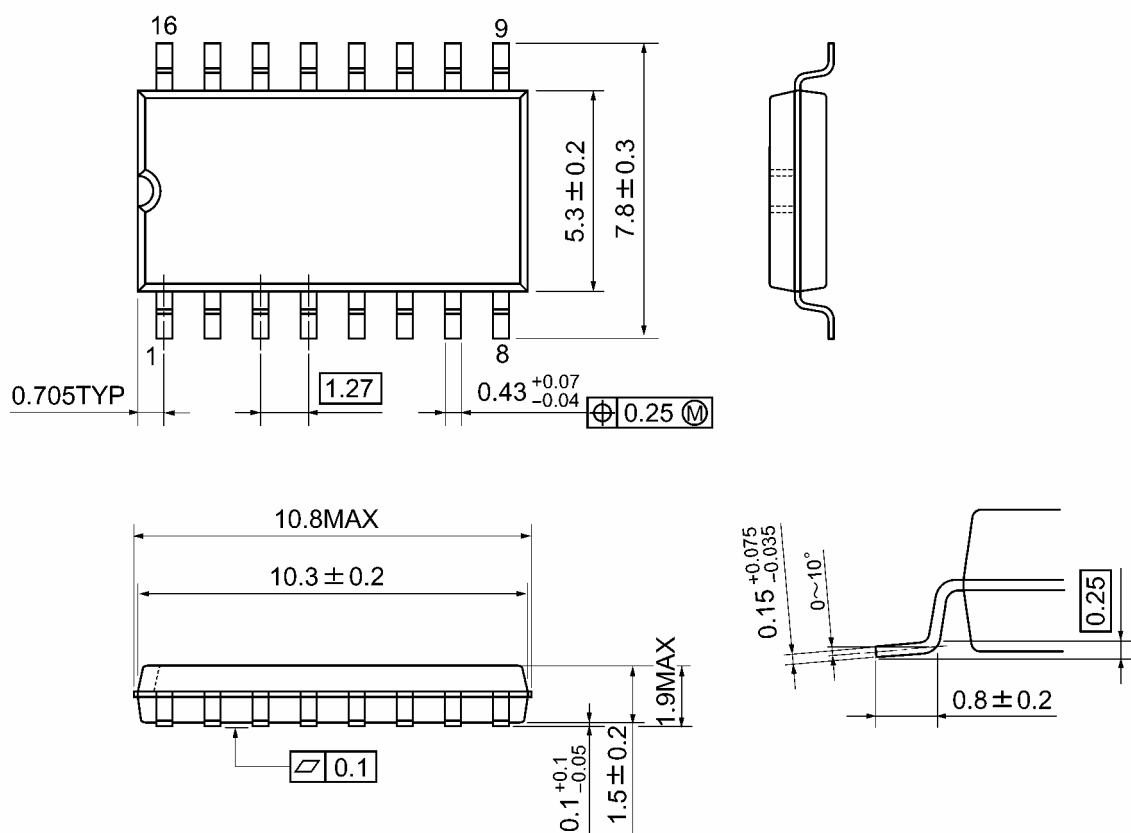


Weight: 1.00 g (typ.)

## Package Dimensions

SOP16-P-300-1.27A

Unit: mm



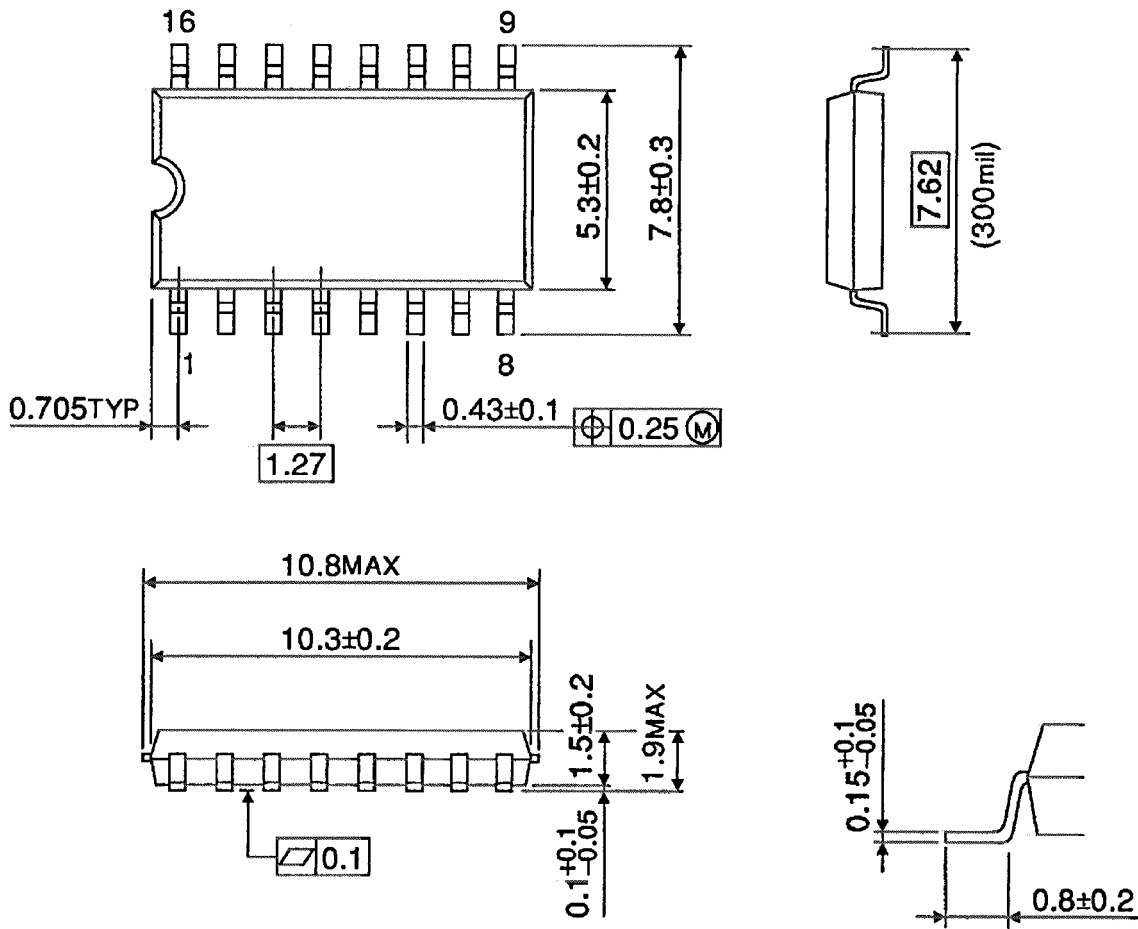
Weight: 0.18 g (typ.)



Package Dimensions

SOP16-P-300-1.27

Unit : mm



Weight: 0.18 g (typ.)

**Note: Lead (Pb)-Free Packages**

**DIP16-P-300-2.54A SOP16-P-300-1.27A**

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