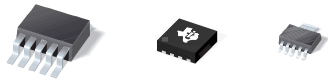


ULTRALOW-NOISE, HIGH PSRR, FAST, RF, 1A LOW-DROPOUT LINEAR REGULATORS

FEATURES

- **1A Low-Dropout Regulator With Enable**
- **Available in Fixed and Adjustable (1.2V to 5.5V) Versions**
- **High PSRR (53dB at 10kHz)**
- **Ultralow-Noise (40μV_{RMS}, TPS79630)**
- **Fast Start-Up Time (50μs)**
- **Stable With a 1μF Ceramic Capacitor**
- **Excellent Load/Line Transient Response**
- **Very Low Dropout Voltage (250mV at Full Load, TPS79630)**
- **3 × 3 SON PowerPAD™, SOT223-6, and DDPAK-5 Packages**

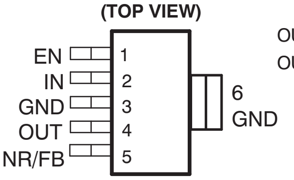
APPLICATIONS

- **RF: VCOs, Receivers, ADCs**
- **Audio**
- **Bluetooth™, Wireless LAN**
- **Cellular and Cordless Telephones**
- **Handheld Organizers, PDAs**

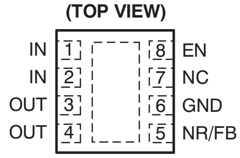
DESCRIPTION

The TPS796xx family of low-dropout (LDO) low-power linear voltage regulators features high power supply rejection ratio (PSRR), ultralow-noise, fast start-up, and excellent line and load transient responses in small outline, 3 × 3 SON, SOT223-6, and DDPAK-5 packages. Each device in the family is stable with a small 1μF ceramic capacitor on the output. The family uses an advanced, proprietary BiCMOS fabrication process to yield extremely low dropout voltages (for example, 250mV at 1A). Each device achieves fast start-up times (approximately 50μs with a 0.001μF bypass capacitor) while consuming very low quiescent current (265 μA typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1μA. The TPS79630 exhibits approximately 40μV_{RMS} of output voltage noise at 3.0V output, with a 0.1μF bypass capacitor. Applications with analog components that are noise sensitive, such as portable RF electronics, benefit from the high PSRR, low noise features, and the fast response time.

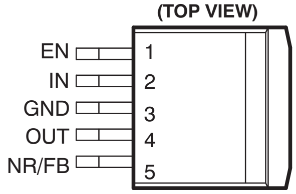
DQC PACKAGE
SOT223-6
(TOP VIEW)



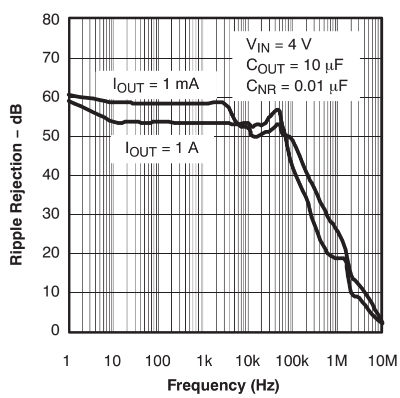
DRB PACKAGE
3mm x 3mm SON
(TOP VIEW)



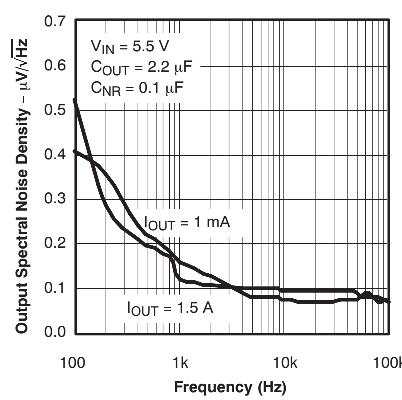
KTT (DDPAK) PACKAGE
(TOP VIEW)



TPS79630
RIPPLE REJECTION
vs
FREQUENCY



TPS79630
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT} (2)
TPS796**xx*yyy*z**	**XX** is nominal output voltage (for example, 28 = 2.8V, 01 = Adjustable). **YYY** is package designator. **Z** is package quantity.

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Output voltages from 1.3V to 4.9V in 100mV increments are available; minimum order quantities may apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating temperature range (unless otherwise noted).

	UNIT
V_{IN} range	–0.3V to 6V
V_{EN} range	–0.3V to V_{IN} + 0.3V
V_{OUT} range	6V
Peak output current	Internally limited
ESD rating, HBM	2kV
ESD rating, CDM	500V
Continuous total power dissipation	See Dissipation Ratings Table
Junction temperature range, T_J	–40°C to +150°C
Storage temperature range, T_{stg}	–65°C to +150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PACKAGE DISSIPATION RATINGS

PACKAGE	BOARD	$R_{\theta JC}$	$R_{\theta JA}$
DDPAK	High-K(1)	2°C/W	23°C/W
SOT223	Low-K(2)	15°C/W	53°C/W
3 × 3 SON	High-K(1)	1.2°C/W	40°C/W

(1) The JEDEC high-K (2s2p) board design used to derive this data was a 3-inch × 3-inch (7,5-cm × 7,5-cm), multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.
(2) The JEDEC low-K (1s) board design used to derive this data was a 3-inch × 3-inch (7,5-cm × 7,5-cm), two-layer board with 2-ounce copper traces on top of the board.

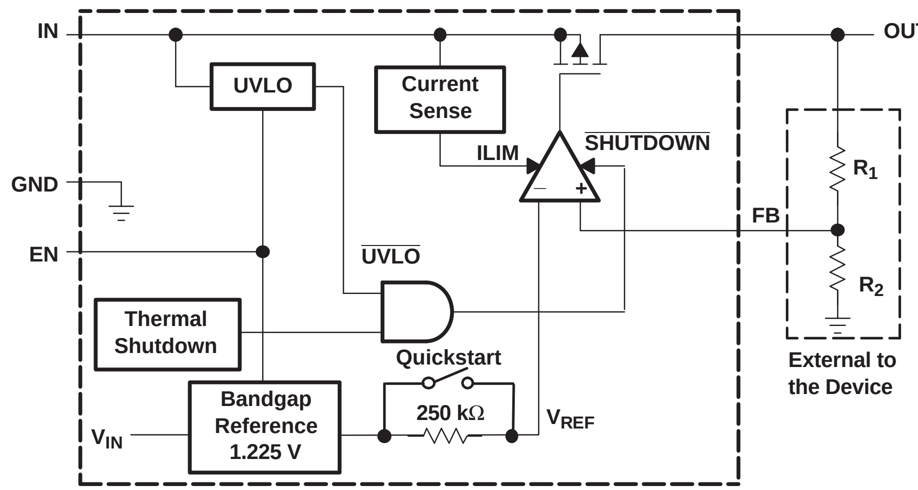
ELECTRICAL CHARACTERISTICS

Over recommended operating temperature range (T_J = –40°C to +125°C), $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)}$ + 1 V(1), I_{OUT} = 1mA, C_{OUT} = 10μF, and C_{NR} = 0.01μF, unless otherwise noted. Typical values are at +25°C.

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} Input voltage(1)					2.7		5.5	V
V_{FB} Internal reference (TPS79601)					1.200	1.225	1.250	V
I_{OUT} Continuous output current					0		1	A
Output voltage	Output voltage range	TPS79601			1.225		5.5 – V_{DD}	V
	Accuracy	TPS79601(2)	0μA ≤ I_{OUT} ≤ 1A, V_{OUT} + 1V ≤ V_{IN} ≤ 5.5V(1)		0.98V_{OUT}	V_{OUT}	1.02V_{OUT}	V
		Fixed V_{OUT} < 5V	0μA ≤ I_{OUT} ≤ 1A, V_{OUT} + 1V ≤ V_{IN} ≤ 5.5V(1)		–2.0		+2.0	%
		Fixed V_{OUT} = 5V	0μA ≤ I_{OUT} ≤ 1A, V_{OUT} + 1V ≤ V_{IN} ≤ 5.5V(1)		–3.0		+3.0	%
Output voltage line regulation ($\Delta V_{OUT}\%/V_{IN}$)(1)			V_{OUT} + 1V ≤ V_{IN} ≤ 5.5V			0.05	0.12	%/V
Load regulation ($\Delta V_{OUT}\%/\Delta I_{OUT}$)			0μA ≤ I_{OUT} ≤ 1A			5		mV
Dropout voltage(3) ($V_{IN} = V_{OUT\ (nom)}$ – 0.1V)		TPS79628	I_{OUT} = 1A			270	365	mV
		TPS79628DRB	I_{OUT} = 250mA			52	90	
		TPS79630	I_{OUT} = 1A			250	345	
		TPS79633	I_{OUT} = 1A			220	325	
		TPS79650	I_{OUT} = 1A			200	300	
Output current limit			V_{OUT} = 0V		2.4		4.2	A
Ground pin current			0μA ≤ I_{OUT} ≤ 1A			265	385	μA
Shutdown current(4)			V_{EN} = 0V, 2.7V ≤ V_{IN} ≤ 5.5V			0.07	1	μA
FB pin current			V_{FB} = 1.225V				1	μA
Power-supply ripple rejection		TPS79630	f = 100Hz, I_{OUT} = 10mA			59		dB
			f = 100Hz, I_{OUT} = 1A			54		
			f = 10Hz, I_{OUT} = 1A			53		
			f = 100Hz, I_{OUT} = 1A			42		
Output noise voltage (TPS79630)			BW = 100Hz to 100kHz, I_{OUT} = 1A	C_{NR} = 0.001μF		54		μV_{RMS}
				C_{NR} = 0.0047μF		46		
				C_{NR} = 0.01μF		41		
				C_{NR} = 0.1μF		40		
Time, start-up (TPS79630)			R_L = 3Ω, C_{OUT} = 1μF	C_{NR} = 0.001μF		50		μs
				C_{NR} = 0.0047μF		75		
				C_{NR} = 0.01μF		110		
EN pin current			V_{EN} = 0V		–1		1	μA
UVLO threshold			V_{CC} rising		2.25		2.65	V
UVLO hysteresis						100		mV
High-level enable input voltage			2.7V ≤ V_{IN} ≤ 5.5V		1.7		V_{IN}	V
Low-level enable input voltage			2.7V ≤ V_{IN} ≤ 5.5V		0		0.7	V

(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 2.7V, whichever is greater. TPS79650 is tested at V_{IN} = 5.5V.
(2) Tolerance of external resistors not included in this specification.
(3) V_{DO} is not measured for TPS79618 and TPS79625 because minimum V_{IN} = 2.7V.
(4) For adjustable version, this applies only after V_{IN} is applied; then V_{EN} transitions high to low.

FUNCTIONAL BLOCK DIAGRAM—ADJUSTABLE VERSION



FUNCTIONAL BLOCK DIAGRAM—FIXED VERSION

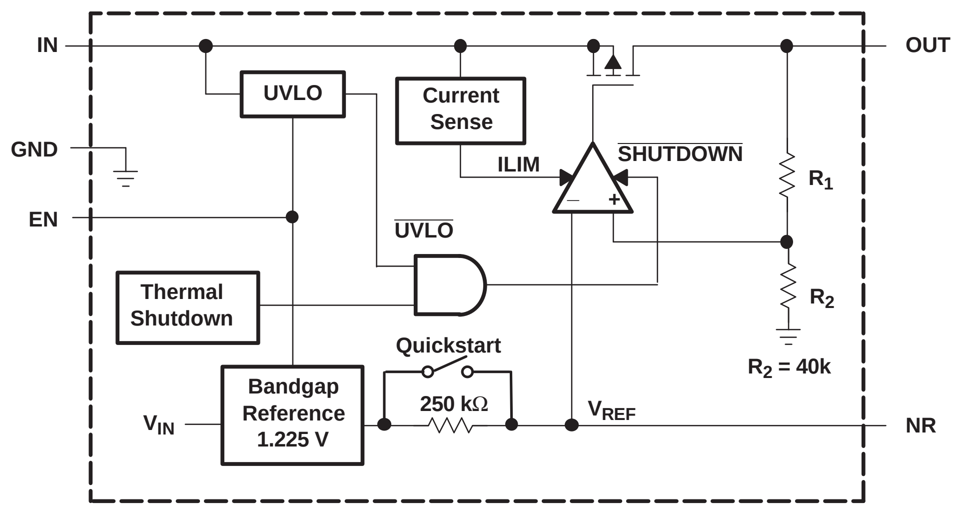


Table 1. Terminal Functions

TERMINAL			DESCRIPTION
NAME	SOT223 (DCQ) DDPAK (KTT)	SON (DRB)	
NR	5	5	Connecting an external capacitor to this pin bypasses noise generated by the internal bandgap. This improves power-supply rejection and reduces output noise.
FB	5	5	This terminal is the feedback input voltage for the adjustable device.
EN	1	8	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
GND	3, Tab	6, PowerPAD	Regulator ground
IN	2	1, 2	Unregulated input to the device.
OUT	4	3, 4	Output of the regulator.

TYPICAL CHARACTERISTICS

TPS79630
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

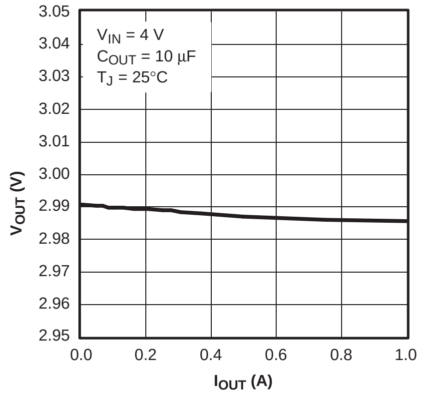


Figure 1.

TPS79628
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

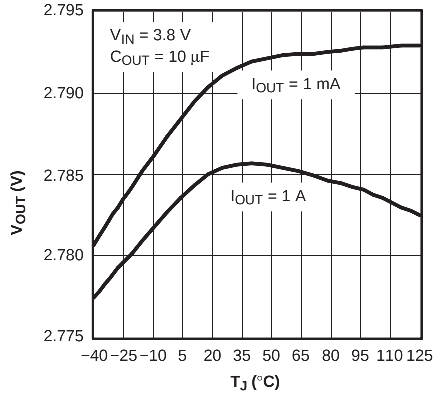


Figure 2.

TPS79628
GROUND CURRENT
vs
JUNCTION TEMPERATURE

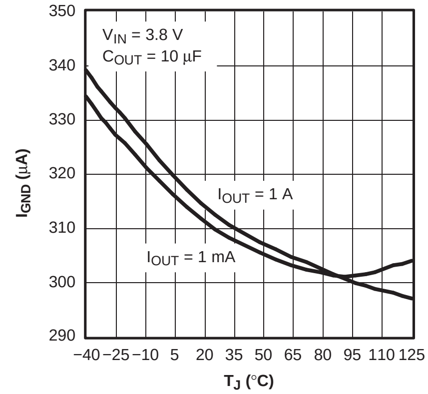


Figure 3.

TPS79630
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

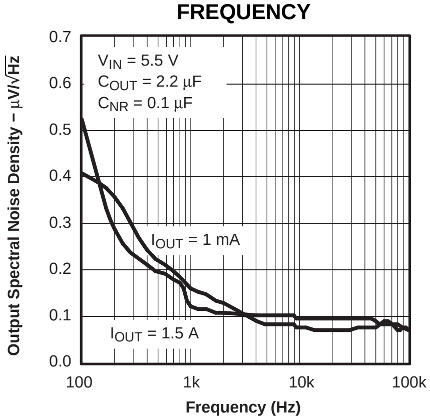


Figure 4.

TPS79630
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

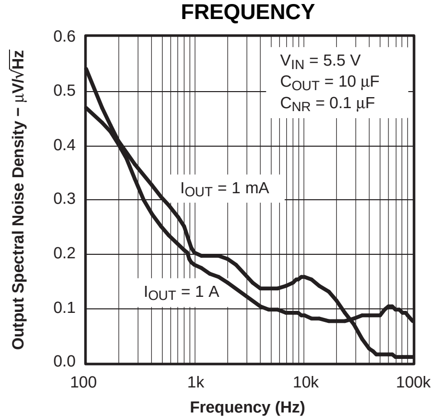


Figure 5.

TPS79630
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

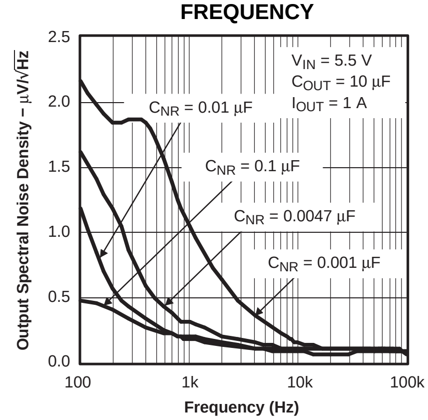


Figure 6.

TPS79630
ROOT MEAN SQUARED OUTPUT NOISE
vs
BYPASS CAPACITANCE

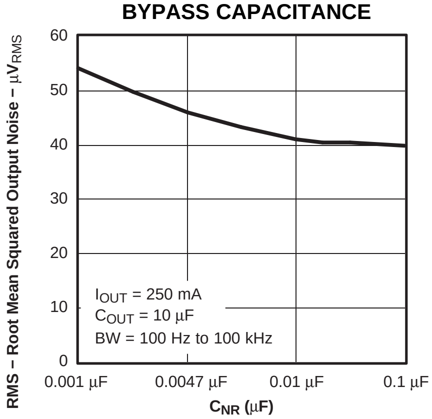


Figure 7.

TPS79628
DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE

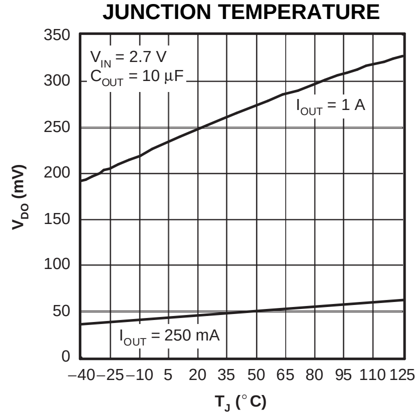


Figure 8.

TPS79630
RIPPLE REJECTION
vs
FREQUENCY

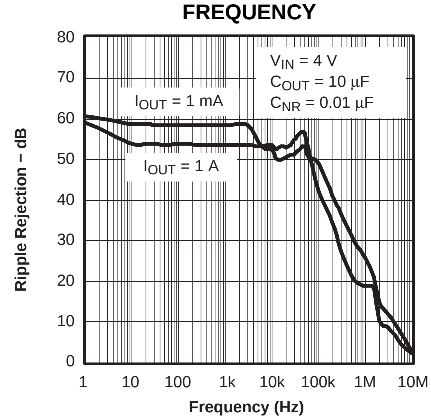


Figure 9.

TYPICAL CHARACTERISTICS (continued)

TPS79630
RIPPLE REJECTION
vs
FREQUENCY

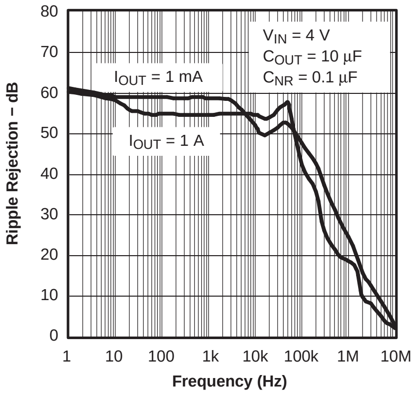


Figure 10.

TPS79630
RIPPLE REJECTION
vs
FREQUENCY

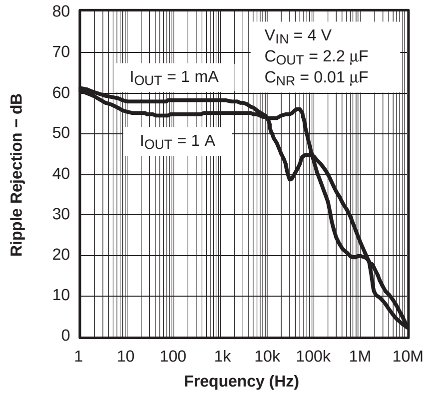


Figure 11.

START-UP TIME

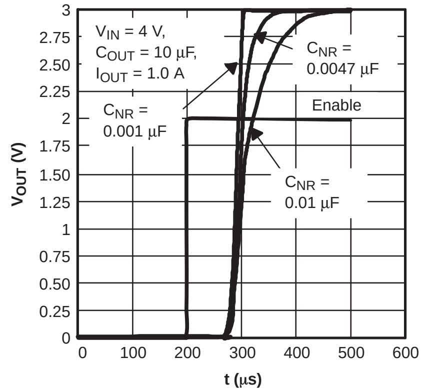


Figure 12.

TPS79618
LINE TRANSIENT RESPONSE

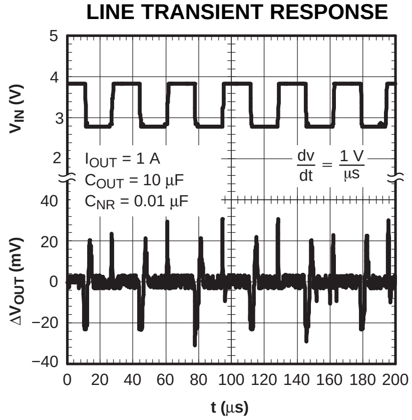


Figure 13.

TPS79630
LINE TRANSIENT RESPONSE

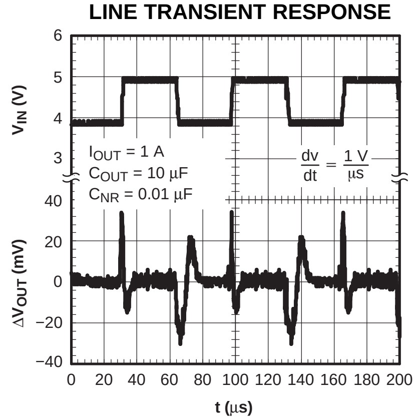


Figure 14.

TPS79628
LOAD TRANSIENT RESPONSE

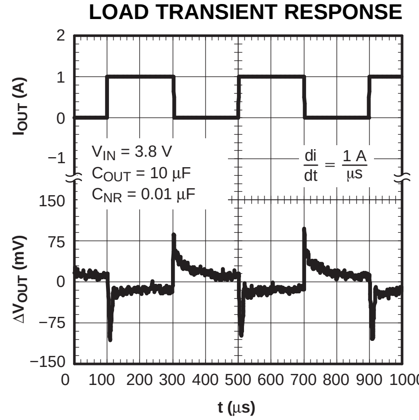


Figure 15.

TPS79625
POWER UP/POWER DOWN

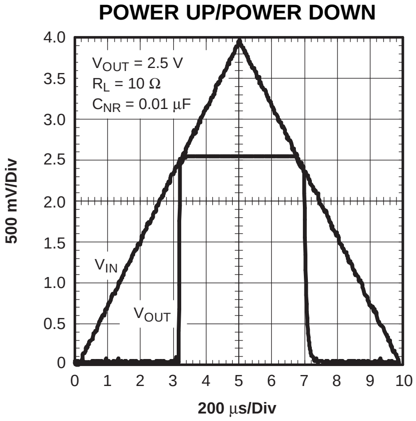


Figure 16.

TPS79630
DROPOUT VOLTAGE
vs
OUTPUT CURRENT

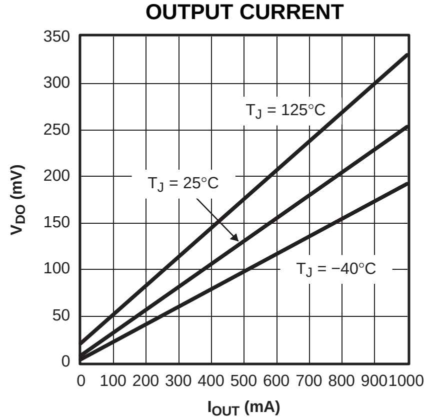


Figure 17.

TPS79601
DROPOUT VOLTAGE
vs
INPUT VOLTAGE

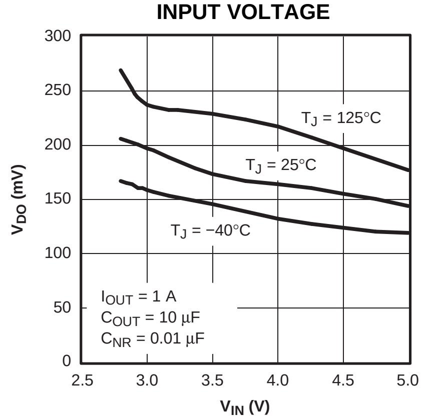


Figure 18.

TYPICAL CHARACTERISTICS (continued)

TPS79630
TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE (ESR)
vs
OUTPUT CURRENT

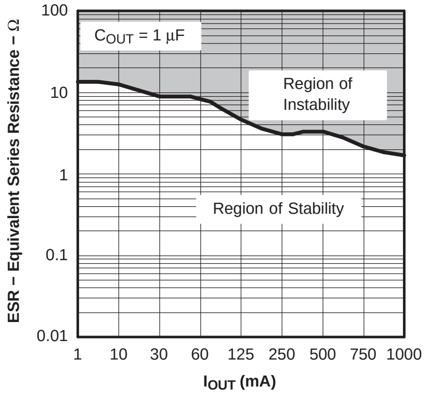


Figure 19.

TPS79630
TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE (ESR)
vs
OUTPUT CURRENT

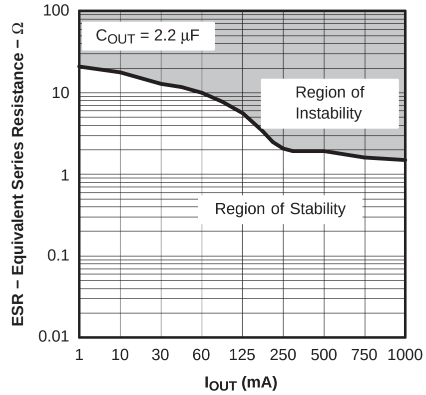


Figure 20.

TPS79630
TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE (ESR)
vs
OUTPUT CURRENT

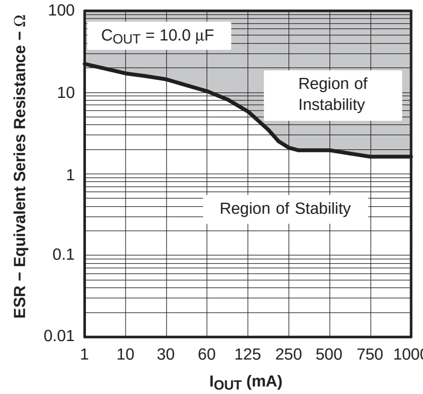


Figure 21.

APPLICATION INFORMATION

The TPS796xx family of low-dropout (LDO) regulators has been optimized for use in noise-sensitive equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (265µA typically), and enable input to reduce supply currents to less than 1µA when the regulator is turned off.

A typical application circuit is shown in Figure 22.

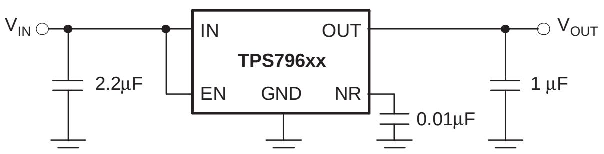


Figure 22. Typical Application Circuit

External Capacitor Requirements

Although not required, it is good analog design practice to place a 0.1µF to 2.2µF capacitor near the input of the regulator to counteract reactive input sources. A 2.2µF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS796xx, is required for stability and improves transient response, noise rejection, and ripple rejection. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like most low dropout regulators, the TPS796xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitor is 1µF. Any 1µF or larger ceramic capacitor is suitable.

The internal voltage reference is a key source of noise in an LDO regulator. The TPS796xx has an NR pin which is connected to the voltage reference through a 250kΩ internal resistor. The 250kΩ internal resistor, in conjunction with an external bypass capacitor connected to the NR pin, creates a low-pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. In order for the regulator to operate properly, the current flow out of the NR pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor, thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current. The bypass capacitor should be no more than 0.1µF in order to ensure that it is fully charged during the quickstart time provided by the internal switch shown in the functional block diagram.

For example, the TPS79630 exhibits 40µV_{RMS} of output voltage noise using a 0.1µF ceramic bypass capacitor and a 10µF ceramic output capacitor. Note that the output starts up slower as the bypass capacitance increases due to the RC time constant at the bypass pin that is created by the internal 250kΩ resistor and external capacitor.

Board Layout Recommendation to Improve PSRR and Noise Performance

To improve ac measurements like PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the ground pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the ground pin of the device.

Regulator Mounting

The tab of the SOT223-6 package is electrically connected to ground. For best thermal performance, the tab of the surface-mount version should be soldered directly to a circuit-board copper area. Increasing the copper area improves heat dissipation.

Solder pad footprint recommendations for the devices are presented in an application bulletin *Solder Pad Recommendations for Surface-Mount Devices*, literature number AB-132, available for download from the TI web site (www.ti.com).

Programming the TPS79601 Adjustable LDO Regulator

The output voltage of the TPS79601 adjustable regulator is programmed using an external resistor divider as shown in Figure 28. The output voltage is calculated using Equation 1:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) \qquad (1)$$

where:

- V_{REF} = 1.2246V typ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 40µA divider current. Lower value resistors can be used for improved noise performance, but the device wastes more power. Higher values should be avoided, as leakage current at FB increases the output voltage error.

The recommended design procedure is to choose R2 = 30.1kΩ to set the divider current at 40μA, C1 = 15pF for stability, and then calculate R1 using Equation 2:

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R2 \quad (2)$$

In order to improve the stability of the adjustable version, it is suggested that a small compensation capacitor be placed between OUT and FB. The approximate value of this capacitor can be calculated as Equation 3:

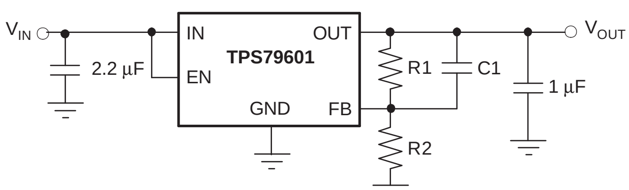
$$C1 = \frac{(3 \times 10^{-7}) \times (R1 + R2)}{(R1 \times R2)} \quad (3)$$

The suggested value of this capacitor for several resistor ratios is shown in the table below (see Figure 23). If this capacitor is not used (such as in a unity-gain configuration) then the minimum recommended output capacitor is 2.2μF instead of 1μF.

Regulator Protection

The TPS796xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power-down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS796xx features internal current limiting and thermal protection. During normal operation, the TPS796xx limits output current to approximately 2.8A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds approximately +165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately +140°C, regulator operation resumes.



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	C1
1.8 V	14.0 kΩ	30.1 kΩ	33 pF
3.6V	57.9 kΩ	30.1 kΩ	15 pF

Figure 23. TPS79601 Adjustable LDO Regulator Programming

THERMAL INFORMATION

The amount of heat that an LDO linear regulator generates is directly proportional to the amount of power it dissipates during operation. All integrated circuits have a maximum allowable junction temperature ($T_J$max) above which normal operation is not assured. A system designer must design the operating environment so that the operating junction temperature (T_J) does not exceed the maximum junction temperature ($T_J$max). The two main environmental variables that a designer can use to improve thermal performance are air flow and external heatsinks. The purpose of this information is to aid the designer in determining the proper operating environment for a linear regulator that is operating at a specific power level.

In general, the maximum expected power ($P_{D(max)}$) consumed by a linear regulator is computed as Equation 4:

$$P_D max = \left(V_{IN(avg)} - V_{OUT(avg)}\right) \times I_{OUT(avg)} + V_{IN(avg)} \times I_{(Q)} \quad (4)$$

where:

- $V_{IN(avg)}$ is the average input voltage.
- $V_{OUT(avg)}$ is the average output voltage.
- $I_{OUT(avg)}$ is the average output current.
- $I_{(Q)}$ is the quiescent current.

For most TI LDO regulators, the quiescent current is insignificant compared to the average output current; therefore, the term $V_{IN(avg)} \times I_{(Q)}$ can be neglected. The operating junction temperature is computed by adding the ambient temperature (T_A) and the increase in temperature due to the regulator's power dissipation. The temperature rise is computed by multiplying the maximum expected power dissipation by the sum of the thermal resistances between the junction and the case ($R_{\theta JC}$), the case to heatsink ($R_{\theta CS}$), and the heatsink to ambient ($R_{\theta SA}$). Thermal resistances are measures of how effectively an object dissipates heat. Typically, the larger the device, the more surface area available for power dissipation and the lower the object's thermal resistance.

Figure 24 illustrates these thermal resistances for **(a)** a SOT223 package mounted in a JEDEC low-K board, and **(b)** a DDPAK package mounted on a JEDEC high-K board.

Equation 5 summarizes the computation:

$$T_J = T_A + P_D max \times \left(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}\right) \quad (5)$$

The $R_{\theta JC}$ is specific to each regulator as determined by its package, lead frame, and die size provided in the regulator data sheet. The $R_{\theta SA}$ is a function of the type and size of heatsink. For example, *black body radiator* type heatsinks can have $R_{\theta CS}$ values ranging from 5°C/W for very large heatsinks to 50°C/W for very small heatsinks. The $R_{\theta CS}$ is a function of how the package is attached to the heatsink. For example, if a thermal compound is used to attach a heatsink to a SOT223 package, $R_{\theta CS}$ of 1°C/W is reasonable.

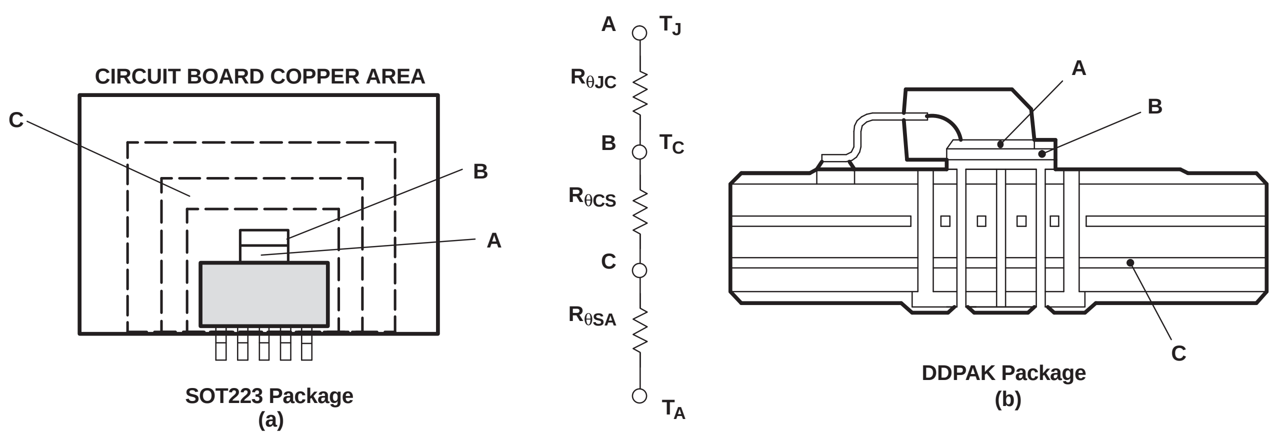


Figure 24. Thermal Resistances

Even if no external *black body radiator* type heatsink is attached to the package, the board on which the regulator is mounted provides some heatsinking through the pin solder connections. Some packages, like the DDPAK and SOT223 packages, use a copper plane underneath the package or the circuit board's ground plane for additional heatsinking to improve their thermal performance. Computer-aided thermal modeling can be used to compute very accurate approximations of an integrated circuit thermal performance in different operating environments (for example., different types of circuit boards, different types and sizes of heatsinks, and different air flows, etc.). Using these models, the three thermal resistances can be combined into one thermal resistance between junction and ambient ($R_{\theta JA}$). This $R_{\theta JA}$ is valid only for the specific operating environment used in the computer model.

Equation 5 simplifies into Equation 6:

$$T_J = T_A + P_D max \times R_{\theta JA} \quad (6)$$

Rearranging Equation 6 gives Equation 7:

$$R_{\theta JA} = \frac{T_J - T_A}{P_D max} \quad (7)$$

Using Equation 6 and the computer model generated curves shown in Figure 25 and Figure 28, a designer can quickly compute the required heatsink thermal resistance/board area for a given ambient temperature, power dissipation, and operating environment.

DDPAK Power Dissipation

The DDPAK package provides an effective means of managing power dissipation in surface mount applications. The DDPAK package dimensions are provided in the *Mechanical Data* section at the end of the data sheet. The addition of a copper plane directly underneath the DDPAK package enhances the thermal performance of the package.

To illustrate, the TPS72525 in a DDPAK package was chosen. For this example, the average input voltage is 5V, the output voltage is 2.5V, the average output current is 1A, the ambient temperature +55°C, the air flow is 150 LFM, and the operating environment is the same as documented below. Neglecting the quiescent current, the maximum average power is calculated as Equation 8:

$$P_D max = (5 - 2.5)\ V \times 1\ A = 2.5\ W \quad (8)$$

Substituting $T_J$max for T_J into Equation 6 gives Equation 9:

$$R_{\theta JA} max = (125 - 55)°C/2.5\ W = 28°C/W \quad (9)$$

From Figure 25, DDPAK Thermal Resistance vs Copper Heatsink Area, the ground plane needs to be 1cm^2 for the part to dissipate 2.5W. The operating environment used in the computer model to construct Figure 25 consisted of a standard JEDEC High-K board (2S2P) with a 1-oz. internal copper plane and ground plane. The package is soldered to a 2-oz. copper pad. The pad is tied through thermal vias to the 1-oz. ground plane. Figure 26 shows the side view of the operating environment used in the computer model.

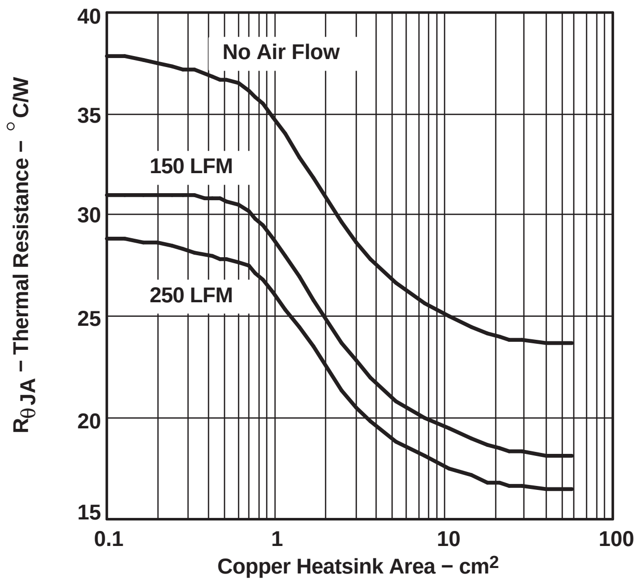


Figure 25. DDPAK Thermal Resistance vs Copper Heatsink Area

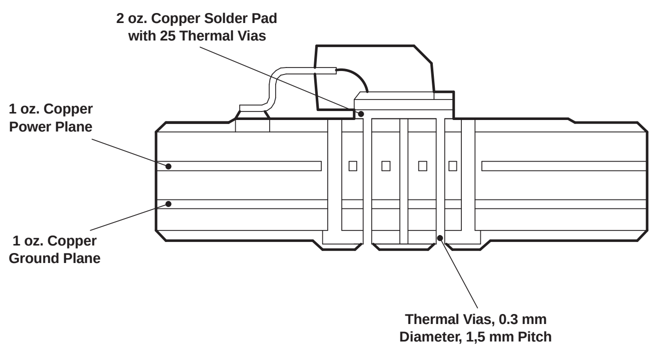


Figure 26. DDPAK Thermal Resistance

From the data in Figure 27 and rearranging Equation 6, the maximum power dissipation for a different ground plane area and a specific ambient temperature can be computed.

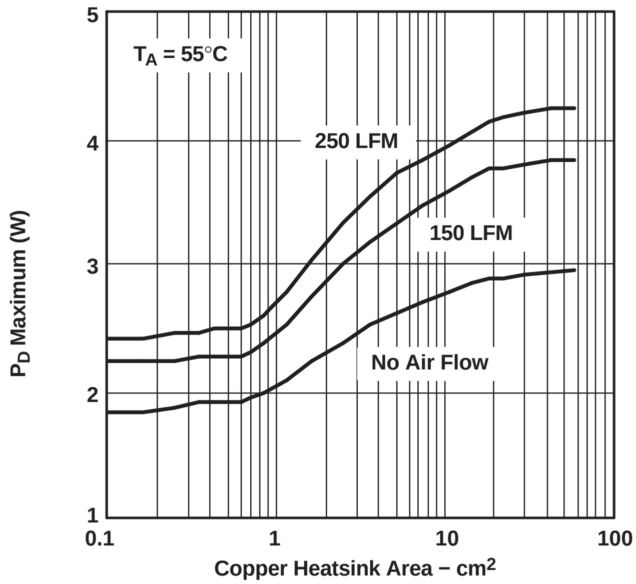


Figure 27. Maximum Power Dissipation vs Copper Heatsink Area

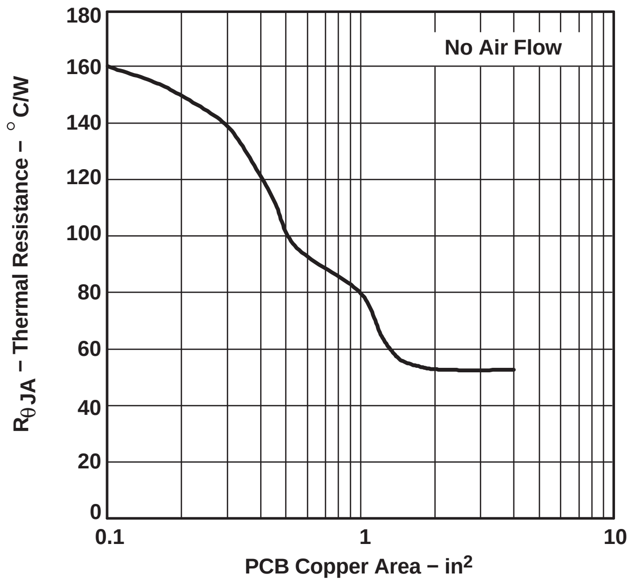


Figure 28. SOT223 Thermal Resistance vs PCB Area

SOT223 Power Dissipation

The SOT223 package provides an effective means of managing power dissipation in surface mount applications. The SOT223 package dimensions are provided in the *Mechanical Data* section at the end of the data sheet. The addition of a copper plane directly underneath the SOT223 package enhances the thermal performance of the package.

To illustrate, the TPS72525 in a SOT223 package was chosen. For this example, the average input voltage is 3.3V, the output voltage is 2.5V, the average output current is 1A, the ambient temperature +55°C, no air flow is present, and the operating environment is the same as documented below. Neglecting the quiescent current, the maximum average power is calculated as Equation 10:

$$P_D max = (3.3 - 2.5)\ V \times 1\ A = 800\ mW \quad (10)$$

Substituting $T_J$max for T_J into Equation 6 gives Equation 11:

$$R_{\theta JA} max = (125 - 55)°C/800\ mW = 87.5°C/W \quad (11)$$

From Figure 28, $R_{\theta JA}$ vs PCB Copper Area, the ground plane needs to be 0.55in^2 for the part to dissipate 800mW. The operating environment used to construct Figure 28 consisted of a board with 1-oz. copper planes. The package is soldered to a 1-oz. copper pad on the top of the board. The pad is tied through thermal vias to the 1-oz. ground plane.

From the data in Figure 28 and rearranging Equation 6, the maximum power dissipation for a different ground plane area and a specific ambient temperature can be computed (see Figure 29).

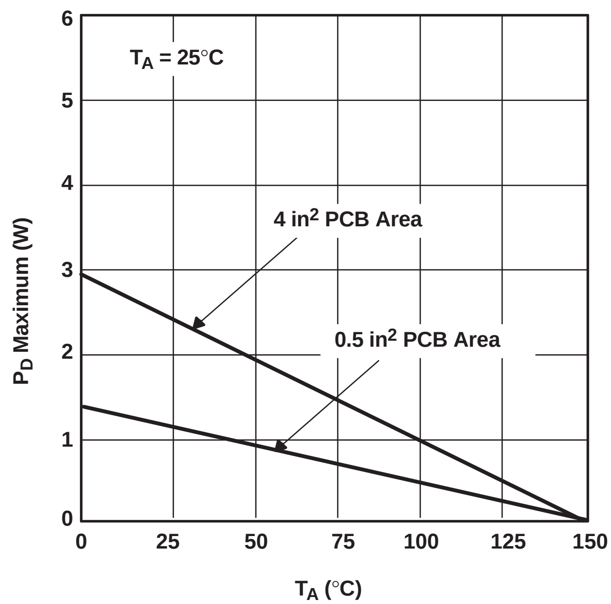


Figure 29. SOT223 Power Dissipation

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPS79601DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79601DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79601DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79601DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79601DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79601DRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79601DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79601DRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79601KTT	OBSOLETE	DDPAK/ TO-263	KTT	5		TBD	Call TI	Call TI
TPS79601KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS79601KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS79601KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS79601KTTTG3	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS79613DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79613DRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79613DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79613DRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79618DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79618DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79618DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79618DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79618KTT	OBSOLETE	DDPAK/ TO-263	KTT	5		TBD	Call TI	Call TI
TPS79618KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS79618KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS79618KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPS79618KTTTG3	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS79625DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79625DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79625DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79625DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79625KTT	OBSOLETE	DDPAK/ TO-263	KTT	5		TBD	Call TI	Call TI
TPS79625KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS79625KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS79625KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS79625KTTTG3	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS79628DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79628DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79628DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79628DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79628DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79628DRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79628DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79628DRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79628KTT	OBSOLETE	DDPAK/ TO-263	KTT	5		TBD	Call TI	Call TI
TPS79628KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS79628KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS79628KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS79628KTTTG3	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS79630DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79630DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79630DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS79630DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79630KTT	OBSOLETE	DDPAK/ TO-263	KTT	5		TBD	Call TI	Call TI
TPS79630KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS79630KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS79630KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS79630KTTTG3	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS79633DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79633DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79633DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79633DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79633KTT	OBSOLETE	DDPAK/ TO-263	KTT	5		TBD	Call TI	Call TI
TPS79633KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS79633KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS79633KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS79633KTTTG3	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS79650DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79650DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79650DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79650DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79650DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79650DRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79650DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79650DRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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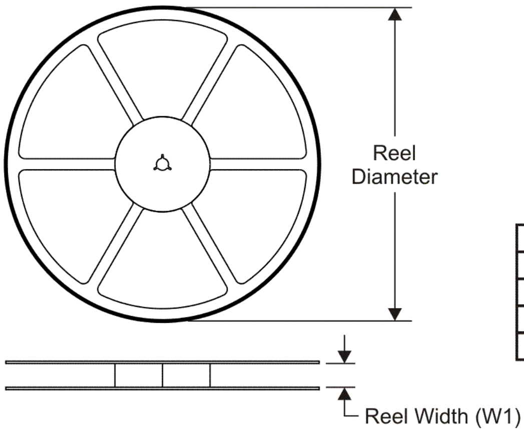
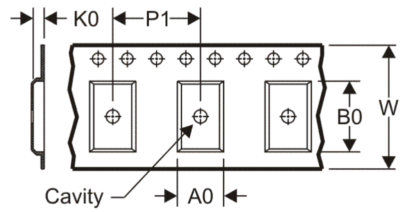
TAPE AND REEL INFORMATION

REEL DIMENSIONS

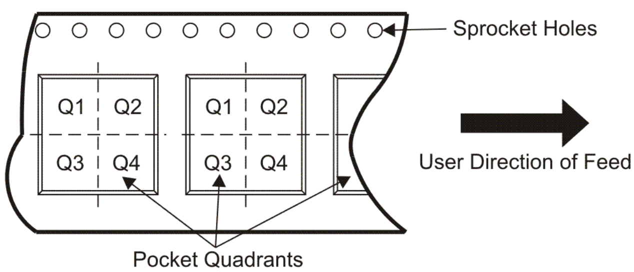


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

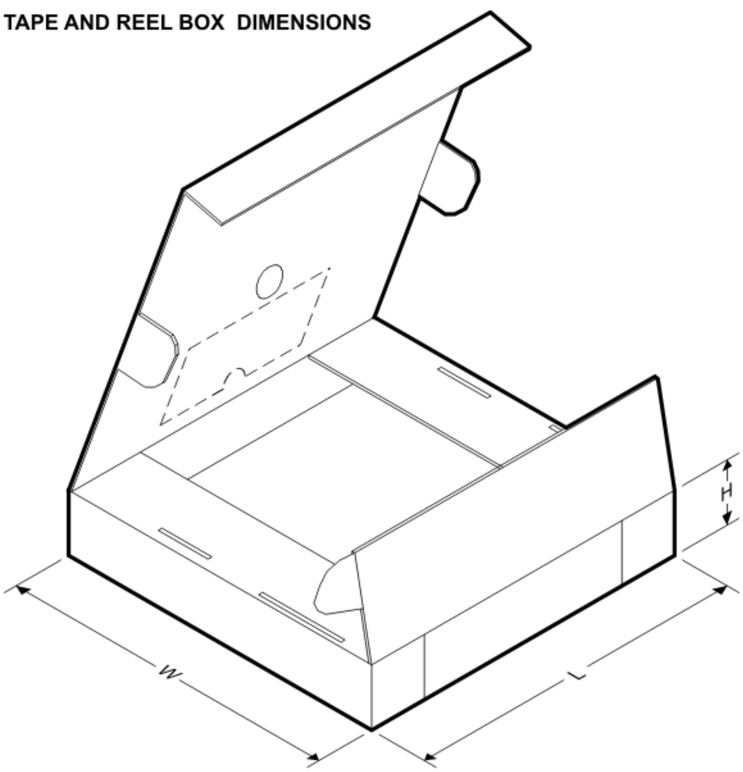


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79601DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.8	7.3	1.88	8.0	12.0	Q3
TPS79601DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS79601DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS79601KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS79601KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS79613DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS79613DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS79618DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.8	7.3	1.88	8.0	12.0	Q3
TPS79618KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS79618KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS79625DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.8	7.3	1.88	8.0	12.0	Q3
TPS79625KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS79625KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS79628DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.8	7.3	1.88	8.0	12.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79628DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS79628DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS79628KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS79628KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS79630DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.8	7.3	1.88	8.0	12.0	Q3
TPS79630KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS79630KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS79633DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.8	7.3	1.88	8.0	12.0	Q3
TPS79633KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS79633KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS79650DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.8	7.3	1.88	8.0	12.0	Q3
TPS79650DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS79650DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

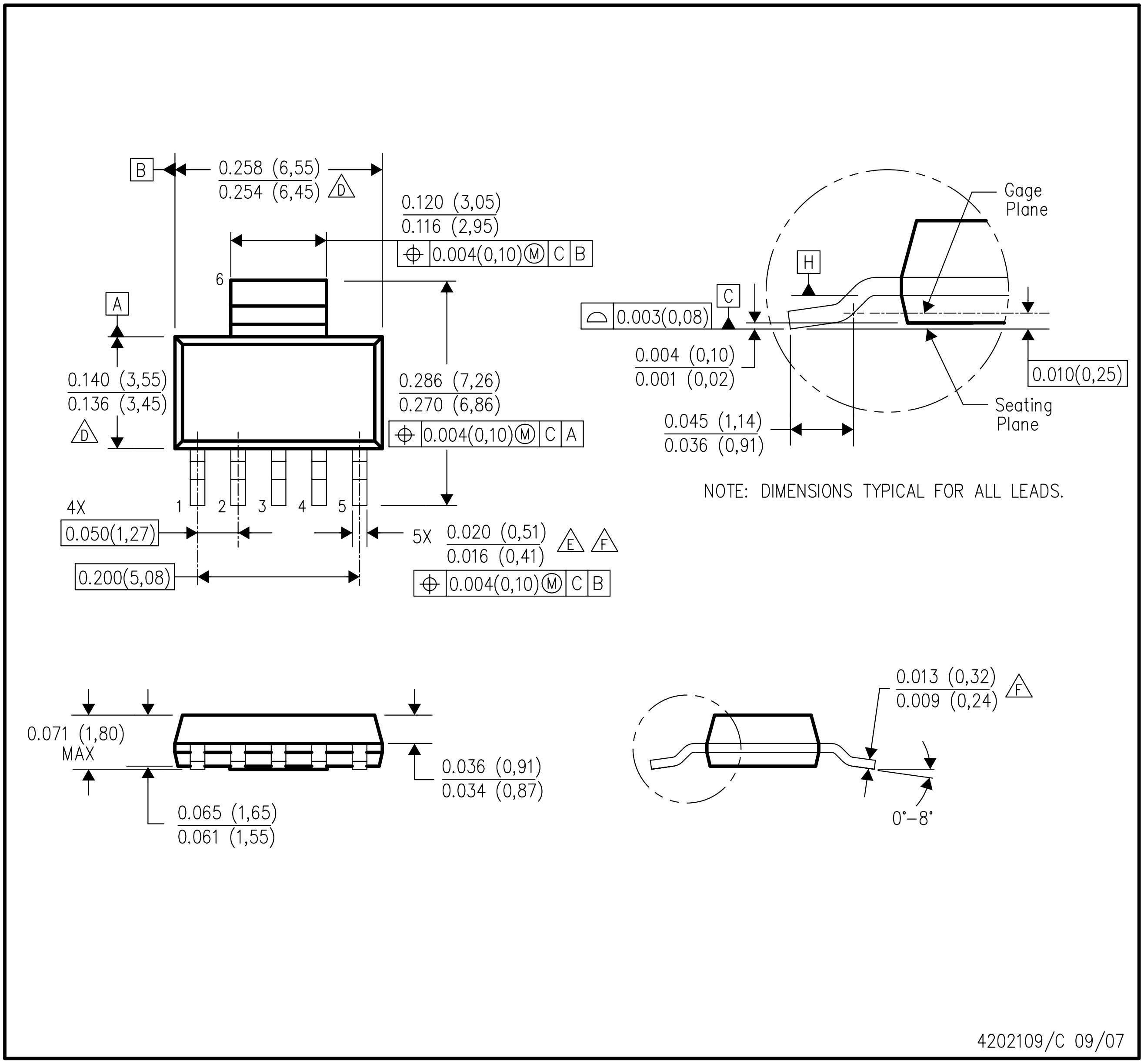
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

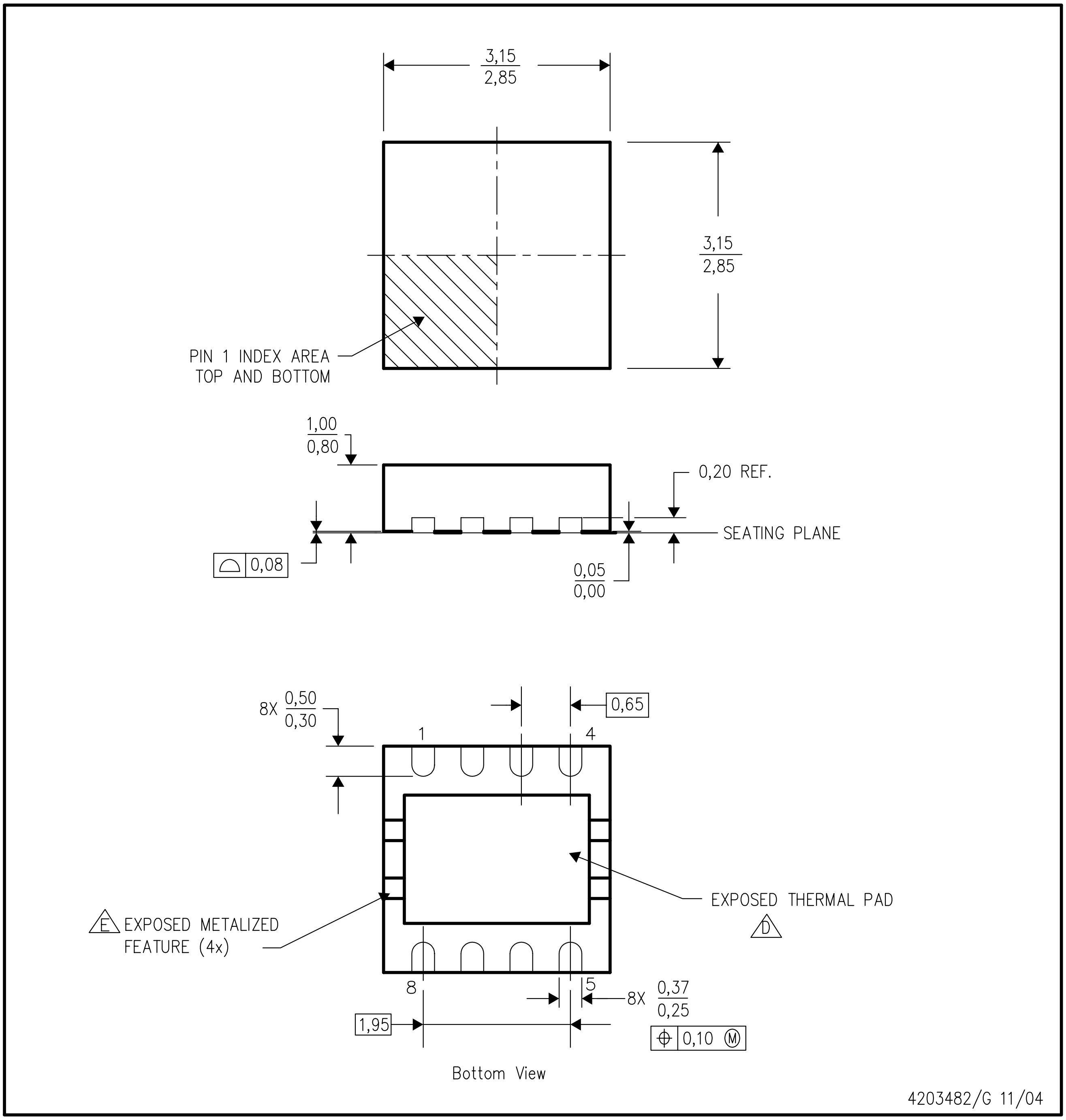
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79601DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS79601DRBR	SON	DRB	8	3000	346.0	346.0	29.0
TPS79601DRBT	SON	DRB	8	250	190.5	212.7	31.8
TPS79601KTTR	DDPAK/TO-263	KTT	5	500	346.0	346.0	41.0
TPS79601KTTT	DDPAK/TO-263	KTT	5	50	346.0	346.0	41.0
TPS79613DRBR	SON	DRB	8	3000	346.0	346.0	29.0
TPS79613DRBT	SON	DRB	8	250	190.5	212.7	31.8
TPS79618DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS79618KTTR	DDPAK/TO-263	KTT	5	500	346.0	346.0	41.0
TPS79618KTTT	DDPAK/TO-263	KTT	5	50	346.0	346.0	41.0
TPS79625DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS79625KTTR	DDPAK/TO-263	KTT	5	500	346.0	346.0	41.0
TPS79625KTTT	DDPAK/TO-263	KTT	5	50	346.0	346.0	41.0
TPS79628DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS79628DRBR	SON	DRB	8	3000	346.0	346.0	29.0
TPS79628DRBT	SON	DRB	8	250	190.5	212.7	31.8
TPS79628KTTR	DDPAK/TO-263	KTT	5	500	346.0	346.0	41.0
TPS79628KTTT	DDPAK/TO-263	KTT	5	50	346.0	346.0	41.0
TPS79630DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS79630KTTR	DDPAK/TO-263	KTT	5	500	346.0	346.0	41.0
TPS79630KTTT	DDPAK/TO-263	KTT	5	50	346.0	346.0	41.0
TPS79633DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS79633KTTR	DDPAK/TO-263	KTT	5	500	346.0	346.0	41.0
TPS79633KTTT	DDPAK/TO-263	KTT	5	50	346.0	346.0	41.0
TPS79650DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS79650DRBR	SON	DRB	8	3000	346.0	346.0	29.0
TPS79650DRBT	SON	DRB	8	250	190.5	212.7	31.8

DCQ (R–PDSO–G6) PLASTIC SMALL–OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Controlling dimension in inches.
- D. Body length and width dimensions are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
- E. Lead width dimension does not include dambar protrusion.
- F. Lead width and thickness dimensions apply to solder plated leads.
- G. Interlead flash allow 0.008 inch max.
- H. Gate burr/protrusion max. 0.006 inch.
- I. Datums A and B are to be determined at Datum H.

DRB (S–PDSO–N8) PLASTIC SMALL OUTLINE



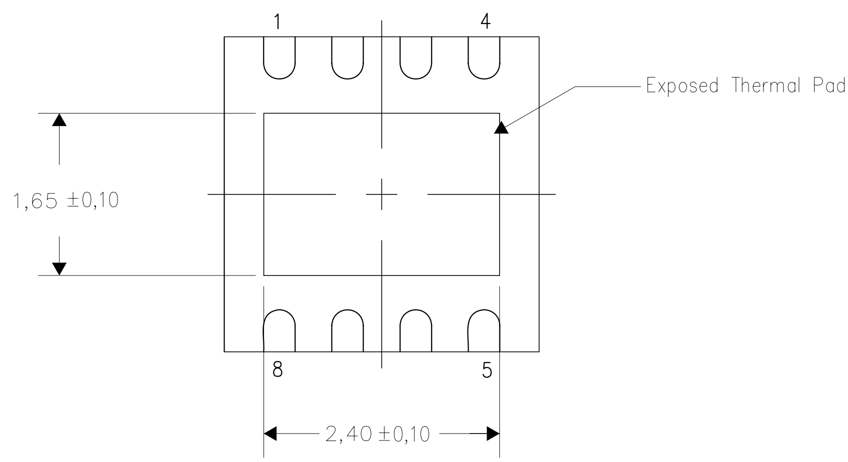
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Metalized features are supplier options and may not be on the package.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

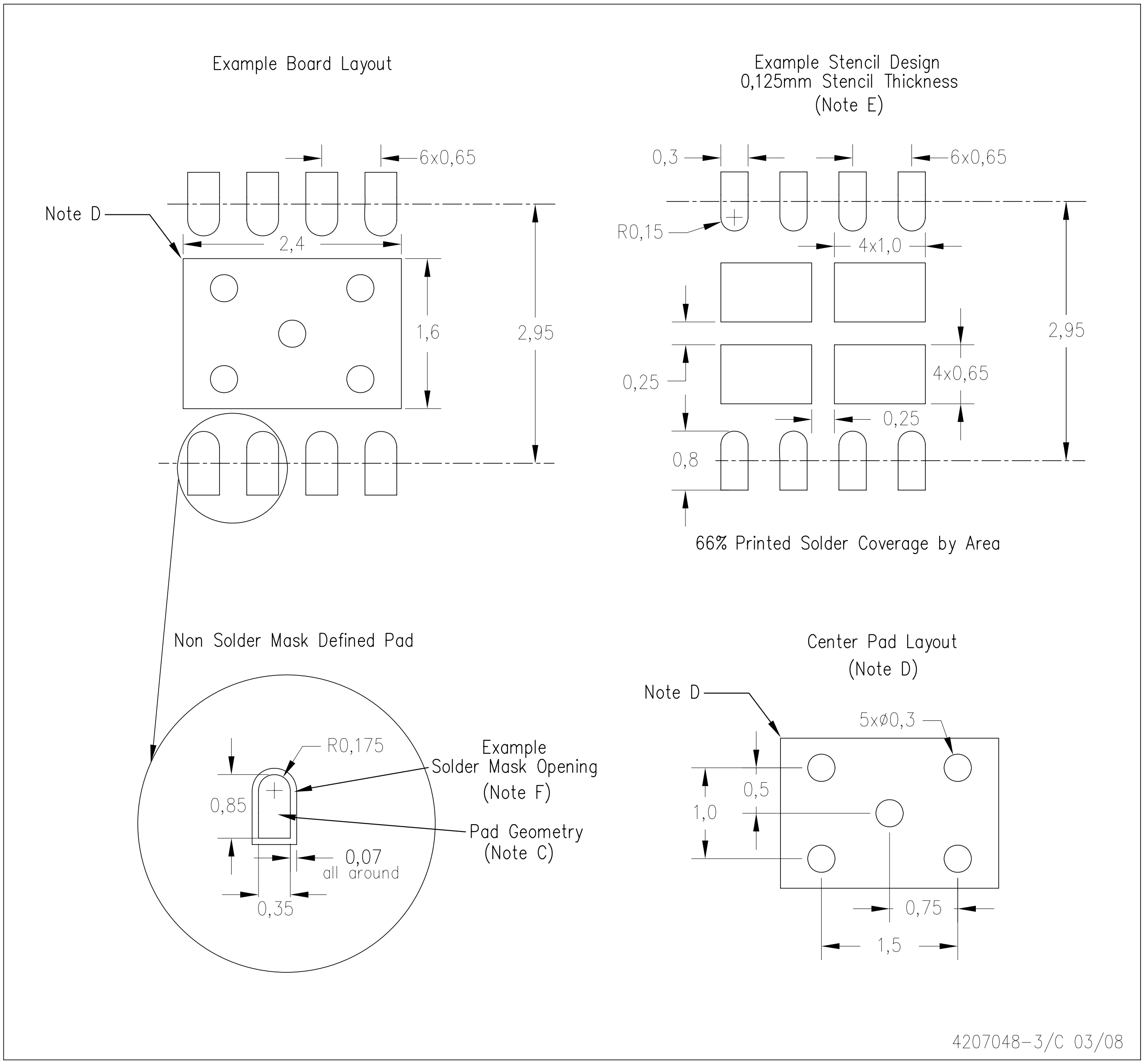


Bottom View

NOTE: All linear dimensions are in millimeters

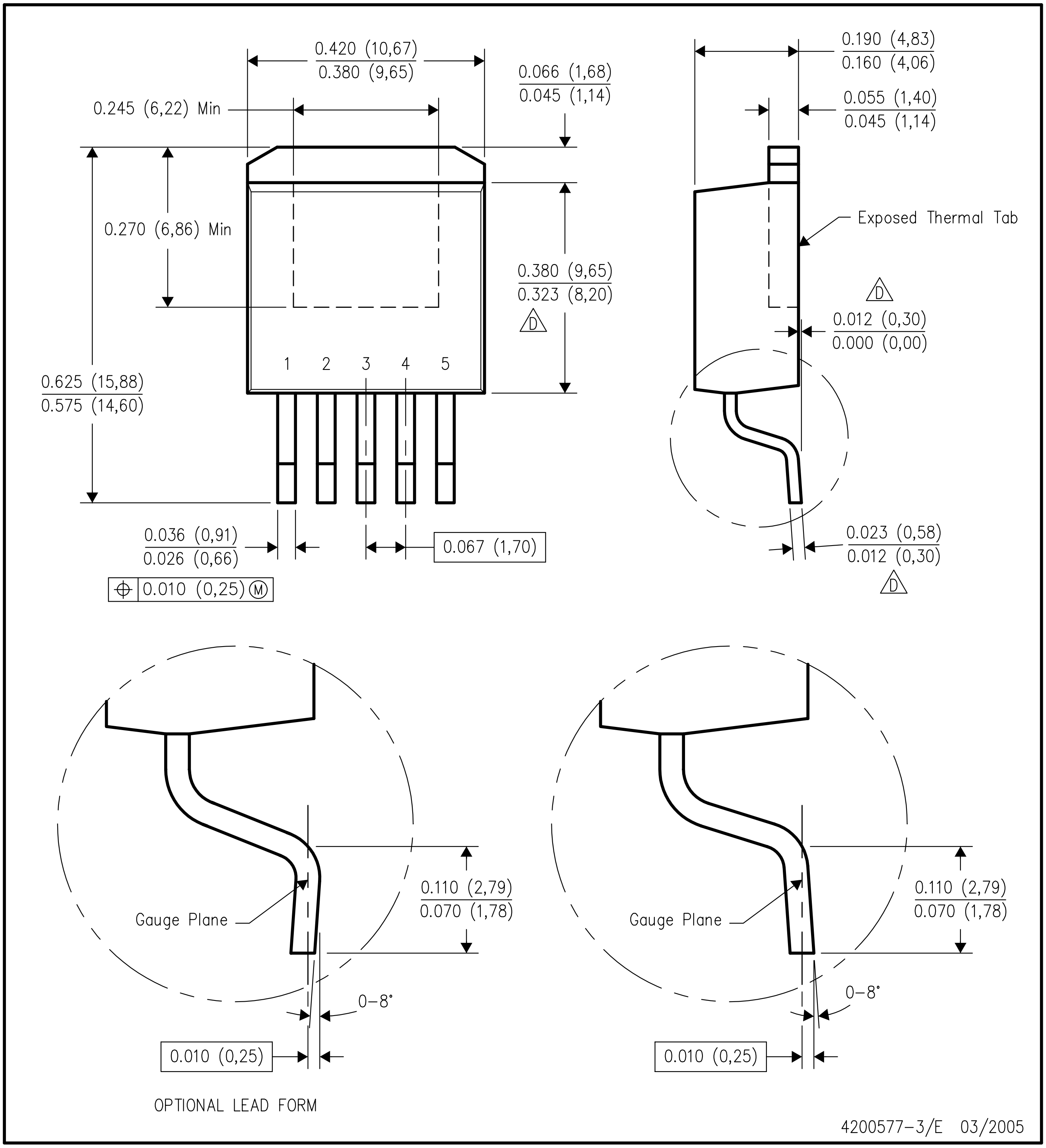
Exposed Thermal Pad Dimensions

DRB (S–VSON–N8)



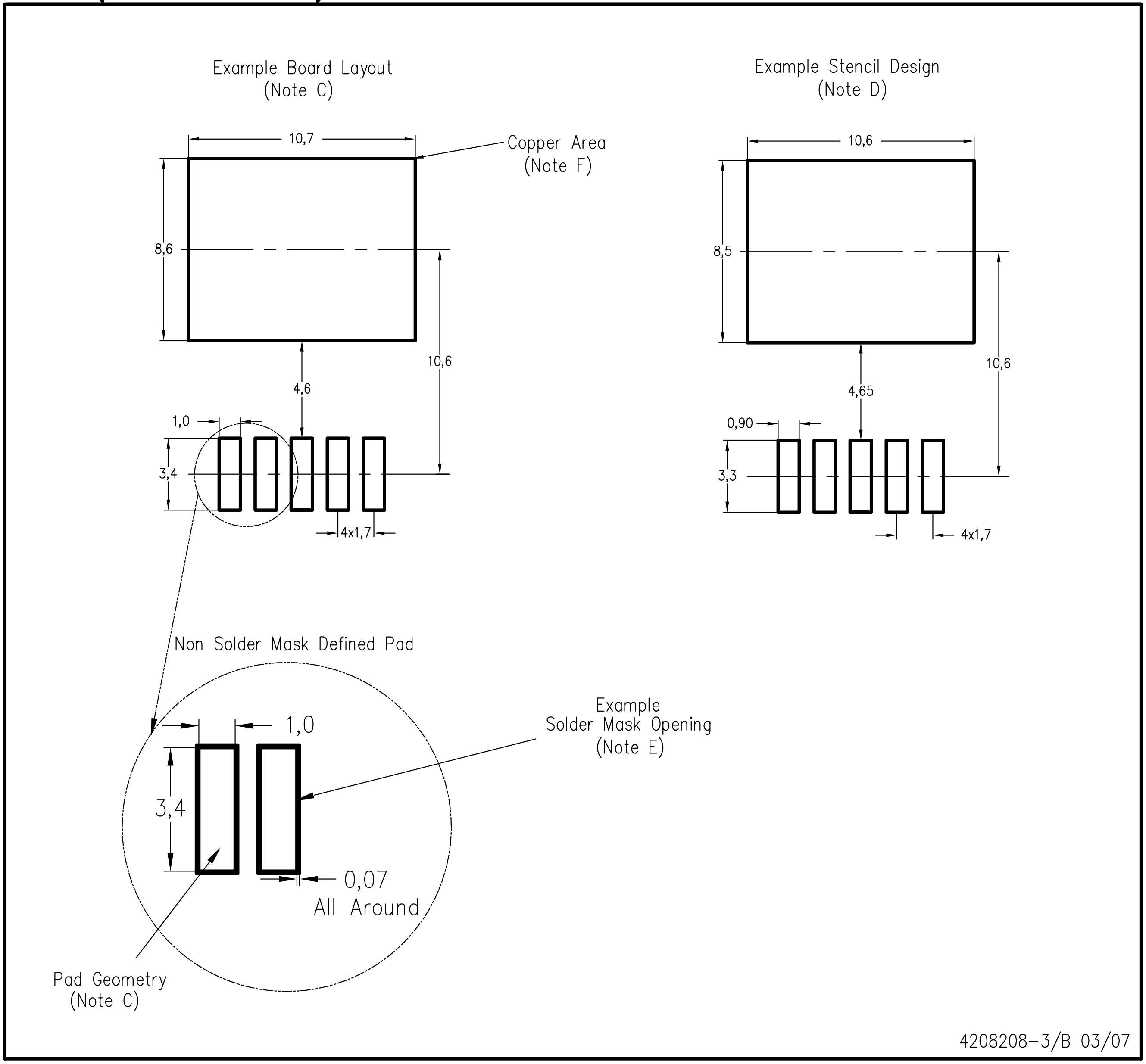
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for solder mask tolerances.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R–PSFM–G5)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

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