2SK3025

Silicon N-channel power MOS FET

■ Features

- Avalanche energy capability guaranteed
- High-speed switching
- Low ON resistance Ron
- No secondary breakdown
- Low-voltage drive
- High electrostatic energy capability

■ Applications

- Non-contact relay
- Solenoid drive
- Motor drive
- Control equipment
- Switching mode regulator

■ Absolute Maximum Ratings $T_C = 25$ °C

Parameter	Symbol	Rating	Unit
Drain-source surrender voltage	V _{DSS}	60	V
Gate-source surrender voltage	V _{GSS}	±20	V
Drain current	I_{D}	±30	A
Peak drain current	I_{DP}	±90	A
Avalanche energy capability *	EAS	45	mJ
Power dissipation	P_{D}	25	W
$T_a = 25^{\circ}C$		1	
Channel temperature	T _{ch}	150	°C
Storage temperature	$T_{\rm stg}$	-55 to +150	°C

Note) *: L = 0.1 mH, $I_L = 30 \text{ A}$, 1 pulse

■ Electrical Characteristics $T_C = 25^{\circ}C \pm 3^{\circ}C$

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Drain-source surrender voltage	V _{DSS}	$I_{\rm D} = 1 \text{ mA}, V_{\rm GS} = 0$	60			V
Drain-source cutoff current	I _{DSS}	$V_{DS} = 50 \text{ V}, V_{GS} = 0$			10	μΑ
Gate-source cutoff current	I_{GSS}	$V_{GS} = \pm 20 \text{ V} \cdot V_{DS} = 0$			±10	μΑ
Gate threshold voltage	V _{th}	$V_{DS} = 10 \text{ V}, I_{D} = 1 \text{ mA}$	1.0		2.5	V
Forward transfer admittance	Yfs	$V_{DS} = 10 \text{ V}, I_D = 15 \text{ A}$	10	18		S
Drain-source ON resistance	R _{DS(on)1}	$V_{GS} = 10 \text{ V}, I_D = 15 \text{ A}$		25	40	mΩ
	R _{DS(on)2}	$V_{GS} = 4 \text{ V}, I_D = 15 \text{ A}$		35	55	
Diode forward voltage	$V_{ m DSF}$	$I_{DR} = 15 \text{ A}, V_{GS} = 0$			-1.3	V
Short-circuit forward transfer capacitance (Common source)	C _{iss}	$V_{DS} = 10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$		1200		pF
Short-circuit output capacitance (Common source)	C _{oss}			400		pF
Reverse transfer capacitance (Common source)	C _{rss}			200		pF
Turn-on delay time	t _{d(on)}	$V_{DD} = 30 \text{ V}, I_D = 15 \text{ A}, R_L = 2 \Omega$		10		ns
Rise time	t _r	$V_{GS} = 10 \text{ V}$		20		ns
Fall time	$t_{\rm f}$			140		ns
Turn-off delay time	t _{d(off)}			350		ns
Thermal resistance (ch-c)	R _{th(ch-c)}				5.0	°C/W
Thermal resistance (ch-a)	R _{th(ch-a)}				125	°C/W

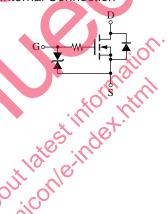
Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

Package

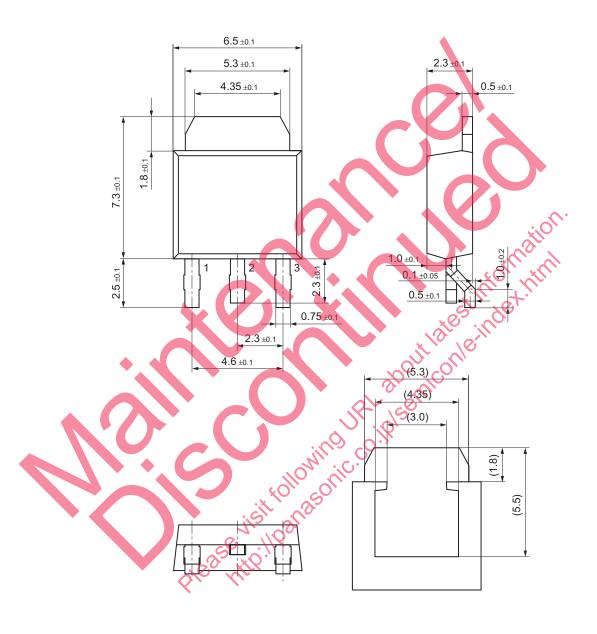
- Code
 - U-DL
- Pin Name
 - 1: Gate
 - 2: Drain
 - 3: Source

Marking Symbol: K3025

Internal Connection



U-DL Unit: mm



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