

2SD2459

Silicon NPN epitaxial planar type

For low-frequency output amplification

■ Features

- High collector-emitter voltage (Base open) V_{CEO}
- Low collector-emitter saturation voltage $V_{CE(sat)}$
- Mini Power type package, allowing downsizing of the equipment and automatic insertion through the tape packing and the magazine packing.

■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Collector-base voltage (Emitter open)	V_{CBO}	150	V
Collector-emitter voltage (Base open)	V_{CEO}	150	V
Emitter-base voltage (Collector open)	V_{EBO}	5	V
Collector current	I_C	1	A
Peak collector current	I_{CP}	1.5	A
Collector power dissipation *	P_C	1	W
Junction temperature	T_j	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Note) *: Printed circuit board: Copper foil area of 1 cm² or more, and the board thickness of 1.7 mm for the collector portion

■ Electrical Characteristics $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

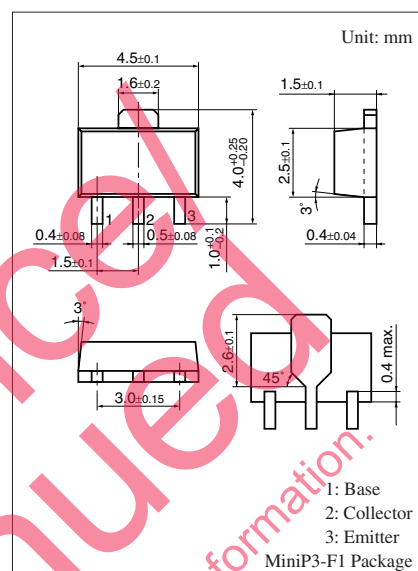
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-base voltage (Emitter open)	V_{CBO}	$I_C = 10\ \mu\text{A}, I_E = 0$	150			V
Collector-emitter voltage (Base open)	V_{CEO}	$I_C = 1\ \text{mA}, I_B = 0$	150			V
Emitter-base voltage (Collector open)	V_{EBO}	$I_C = 10\ \mu\text{A}, I_C = 0$	5			V
Collector-base cutoff current (Emitter open)	I_{CBO}	$V_{CB} = 75\ \text{V}, I_E = 0$			0.1	μA
Forward current transfer ratio	h_{FE1}^{*2}	$V_{CE} = 2\ \text{V}, I_C = 100\ \text{mA}$	120		340	—
	h_{FE2}^{*1}	$V_{CE} = 2\ \text{V}, I_C = 500\ \text{mA}$	40			
Collector-emitter saturation voltage ^{*1}	$V_{CE(sat)}$	$I_C = 500\ \text{mA}, I_B = 25\ \text{mA}$		0.11	0.30	V
Base-emitter saturation voltage ^{*1}	$V_{BE(sat)}$	$I_C = 500\ \text{mA}, I_B = 25\ \text{mA}$		0.8	1.2	V
Transition frequency	f_T	$V_{CB} = 10\ \text{V}, I_E = -50\ \text{mA}, f = 200\ \text{MHz}$		90		MHz
Collector output capacitance (Common base, input open circuited)	C_{ob}	$V_{CB} = 10\ \text{V}, I_E = 0, f = 1\ \text{MHz}$		12	20	pF

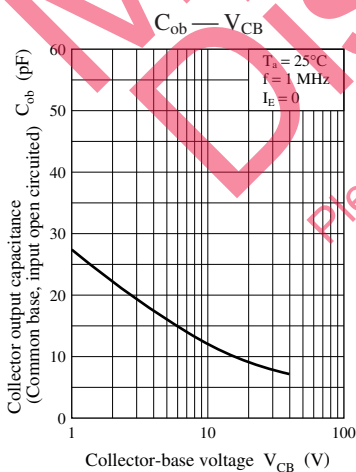
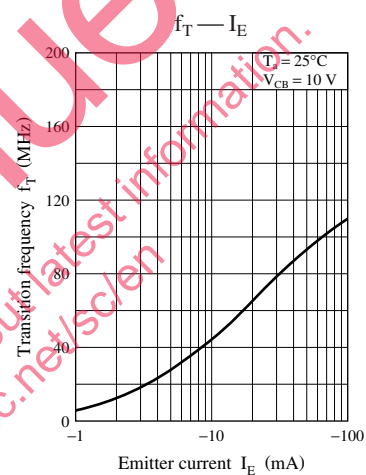
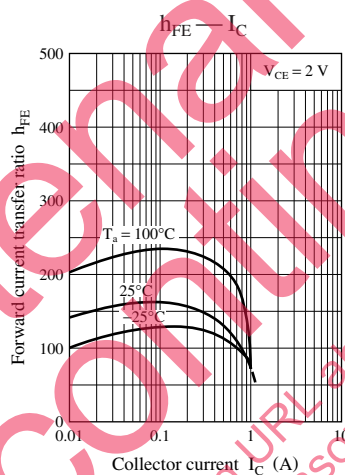
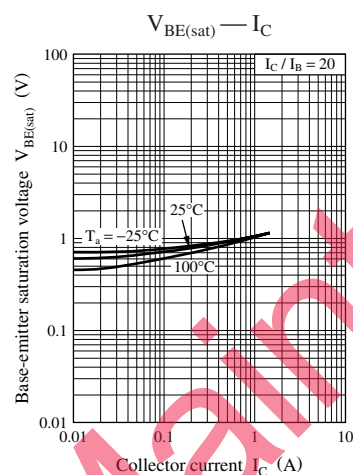
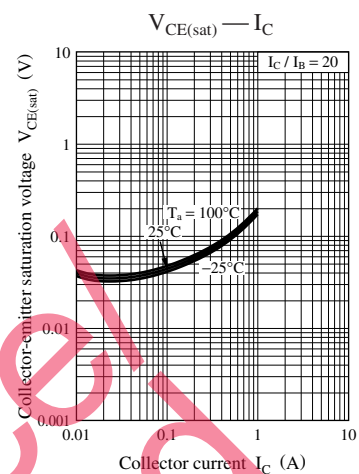
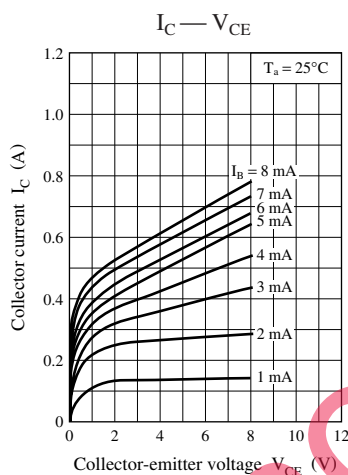
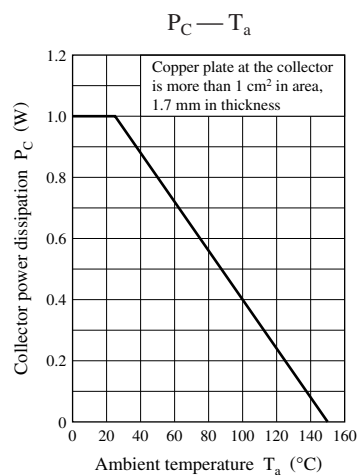
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

2. *1: Pulse measurement

*2: Rank classification

Rank	R	S
h_{FE1}	120 to 240	170 to 340





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