

2SC3507

Silicon NPN triple diffusion planar type

For high breakdown voltage high-speed switching

■ Features

- High-speed switching
- High collector-base voltage (Emitter open) V_{CBO}
- Satisfactory linearity of forward current transfer ratio h_{FE}
- Full-pack package which can be installed to the heat sink with one screw

■ Absolute Maximum Ratings $T_C = 25^\circ\text{C}$

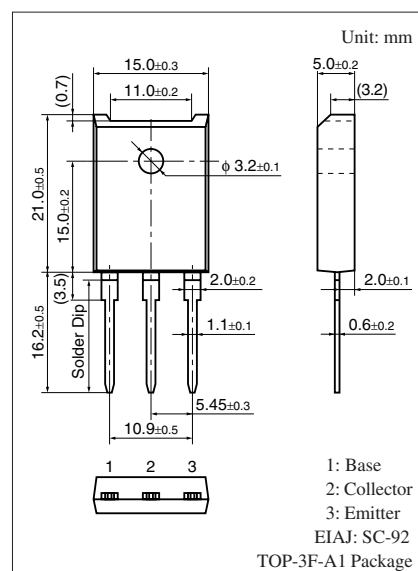
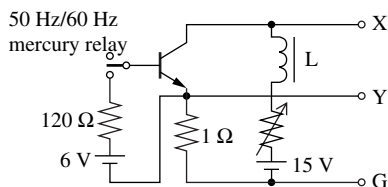
Parameter	Symbol	Rating	Unit
Collector-base voltage (Emitter open)	V_{CBO}	1 000	V
Collector-emitter voltage (E-B short)	V_{CES}	1 000	V
Collector-emitter voltage (Base open)	V_{CEO}	800	V
Emitter-base voltage (Collector open)	V_{EBO}	7	V
Collector current	I_C	5	A
Base current	I_B	3	A
Peak collector current	I_{CP}	10	A
Collector power dissipation	P_C	80	W
		3.0	
Junction temperature	T_j	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

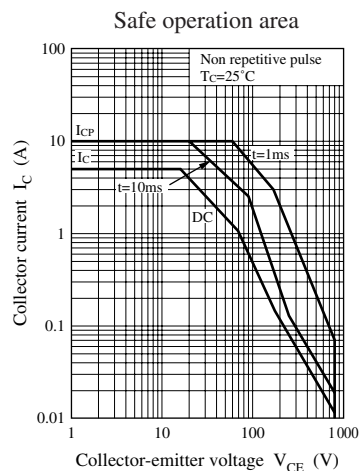
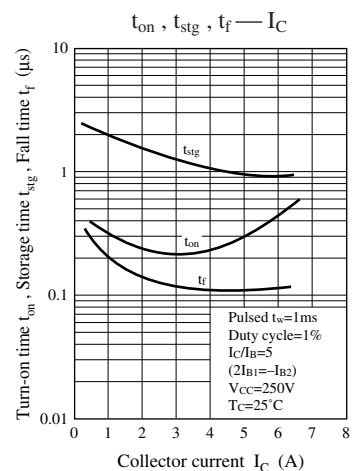
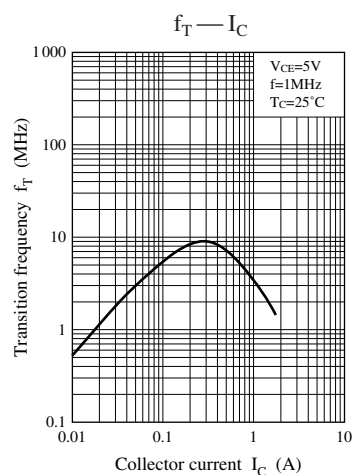
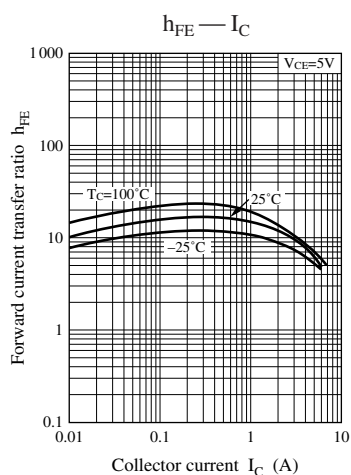
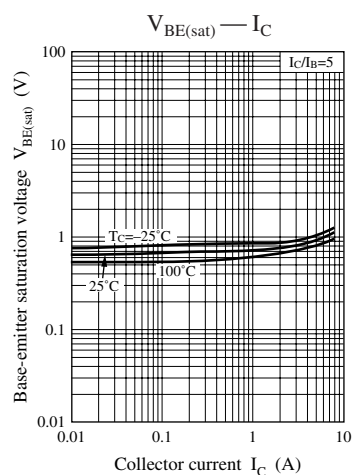
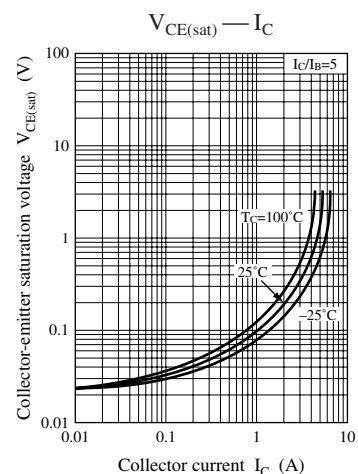
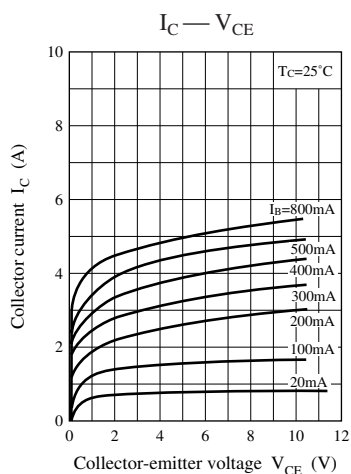
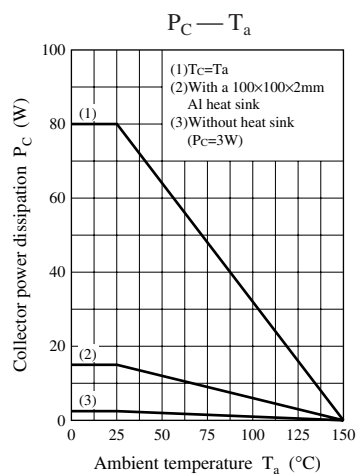
■ Electrical Characteristics $T_C = 25^\circ\text{C} \pm 3^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-emitter sustaining voltage *	$V_{CEO(SUS)}$	$I_C = 0.5 \text{ A}$, $L = 50 \text{ mH}$	800			V
Collector-base cutoff current (Emitter open)	I_{CBO}	$V_{CB} = 1\,000 \text{ V}$, $I_E = 0$			50	μA
Emitter-base cutoff current (Collector open)	I_{EBO}	$V_{EB} = 7 \text{ V}$, $I_C = 0$			50	μA
Forward current transfer ratio	h_{FE}	$V_{CE} = 5 \text{ V}$, $I_C = 3 \text{ A}$	6			—
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C = 3 \text{ A}$, $I_B = 0.6 \text{ A}$			1.5	V
Base-emitter saturation voltage	$V_{BE(sat)}$	$I_C = 3 \text{ A}$, $I_B = 0.6 \text{ A}$			1.5	V
Transition frequency	f_T	$V_{CE} = 5 \text{ V}$, $I_C = 0.5 \text{ A}$, $f = 1 \text{ MHz}$		6		MHz
Turn-on time	t_{on}	$I_C = 3 \text{ A}$			1.0	μs
Storage time	t_{stg}	$I_{B1} = 0.6 \text{ A}$, $I_{B2} = -1.2 \text{ A}$			2.5	μs
Fall time	t_f	$V_{CC} = 250 \text{ V}$			0.5	μs

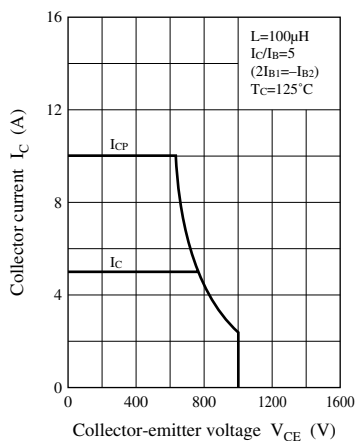
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

2. *: $V_{CEO(SUS)}$ test circuit

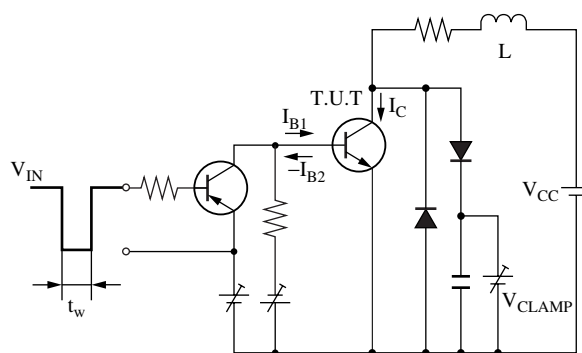




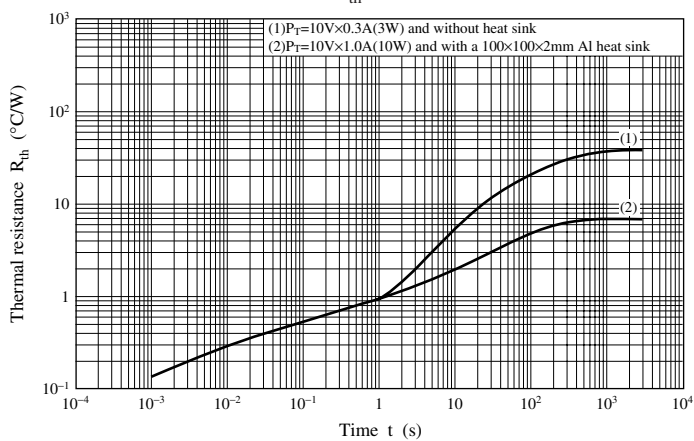
Safe operation area (Reserve bias)



Safe operation area (Reserve bias) measurement circuit



$R_{th} - t$



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