Highly Programmable Voltage Supply Controller and Supervisory Circuit

Preliminary

FEATURES

- Operational from any of four Voltage Monitoring Inputs
- Programmable Closed Loop Power-up Cascading
- Programmability allows monitoring any voltage between 0.9V and 6.0V with no external components
- Programmable Watchdog Timer
- Programmable Longdog™ Timer
- Programmable Reset Pulse Width
- Programmable Nonvolatile Combinatorial Logic for generation of Reset and Interrupt outputs
- Fault Status Register
- 4k-Bit Nonvolatile Memory

INTRODUCTION

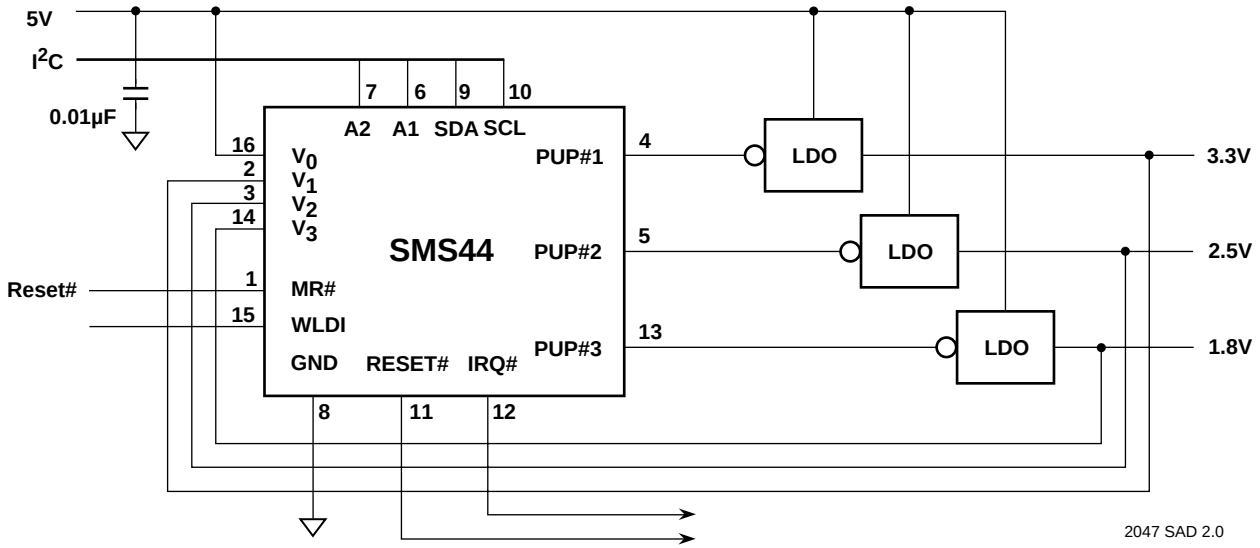
The SMS44 is a highly programmable voltage supply controller and supervisory circuit designed specifically for advanced systems that need to monitor multiple voltages. The SMS44 can monitor four separate voltages without the need of any external voltage divider circuitry.

The SMS44 can also be used to enable DC/DC converters or LDOs to provide a closed loop cascading of the supplies during power -up.

The SMS44 watchdog timer has a user programmable time-out period and it can be placed in an idle mode for system initialization or system debug. All of the functions are user accessible through an industry standard 2-wire serial interface.

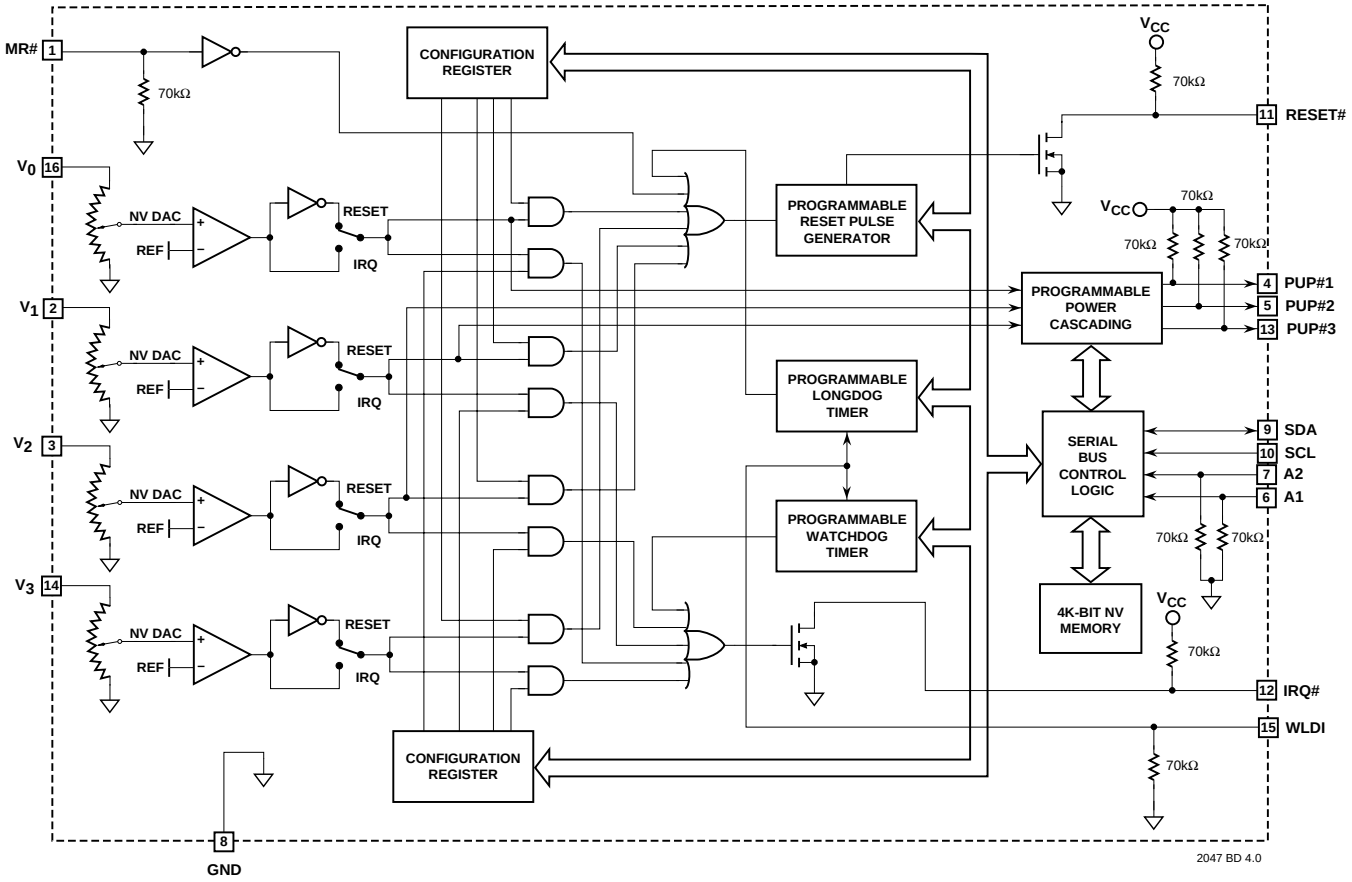
Programming of configuration, control and calibration values by the user can be simplified with the interface adapter and Windows GUI software obtainable from Summit Microelectronics.

SIMPLIFIED APPLICATION DRAWING



Closed Loop Power-up Supply Cascading

FUNCTIONAL BLOCK DIAGRAM



CASCADING

If a specific order in which the supplies are turned on and brought up to their valid voltage levels is needed, time based sequencing will not suffice. In this case supply cascading should be utilized, where the supplies are enabled a certain period of time after the previous voltage has reached its minimum valid level. Figure 1 shows that each succeeding voltage must reach its minimum valid level before the timer is started to time the interval, ***t***, for the next voltage. The duration of each ***t*** is programmable. The next supply is not enabled until the timer has elapsed. See also Figure 5.

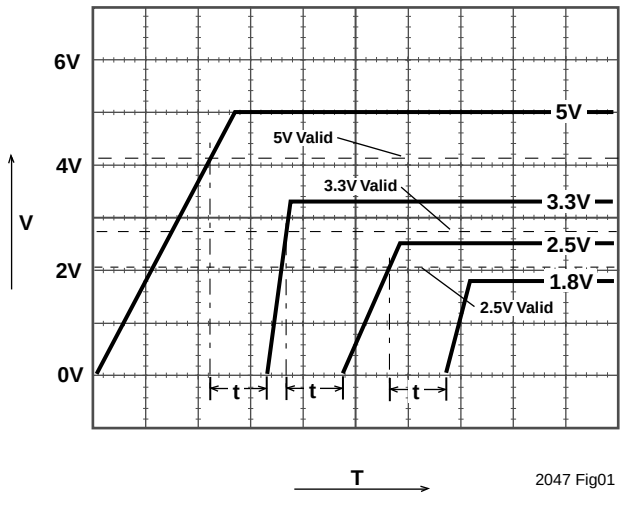
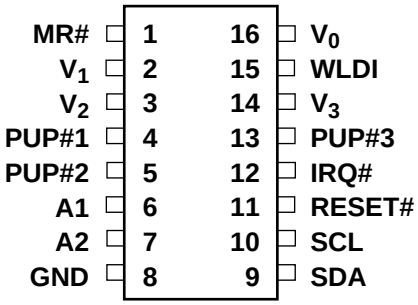


Figure 1. Cascading Power Supplies

PIN CONFIGURATION

16-Pin SOIC or
16-Pin SSOP



2047 PCon 2.0

PIN NAMES

Pin	Name	Function
1	MR#	Manual reset input
2	V_1	Voltage supply and monitor input
3	V_2	Voltage supply and monitor input
4	PUP#1	Power up permitted output
5	PUP#2	Power up permitted output
6	A1	Address input
7	A2	Address input
8	GND	Power supply return
9	SDA	Serial data I/O
10	SCL	Serial data clock
11	RESET#	Reset out
12	IRQ#	Interrupt out
13	PUP#3	Power up permitted output
14	V_3	Voltage supply and monitor input
15	WLDI	Watchdog/longdog timer interrupt
16	V_0	Voltage supply and monitor input

2047 Pins Table 2.0

RECOMMENDED OPERATING CONDITIONS

Temperature	–40ºC to 85ºC.
Voltage	2.7V to 5.5V

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to 125°C
Storage Temperature ..... –65°C to 150°C
Lead Solder Temperature (10s) ..... 300 °C
Terminal Voltage with Respect to GND:
V_0, V_1, V_2, and V_3 ..... –0.3V to 6.0V
All Others ..... –0.3V to 6.0V

***COMMENT**

Stresses beyond the listed Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

DC OPERATING CHARACTERISTICS

(**Over Recommended Operating Conditions; Voltages are relative to GND**)

Symbol	Parameter	Notes			Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage	1V min. refers to a valid reset output being generated			1.0		5.5	V
		Memory read/write operations: at least one of the V inputs must be at or above V_{CC} min.			2.7		5.5	V
I_{CC}	Supply current	$V_{CC} \leq 5.5V$; V_0 trip point 4.7V; V_1, V_2, V_3 = GND; MR# = V_{CC}; all outputs floating				200	400	µA
		Configuration register or memory access					3	mA
V_{PTH} Range	Programmable threshold range	Reset threshold voltage range V_0 to V_3 (20mV increments)			0.9		6.0	V
V_{PTH}	Programmable threshold				–2.5	V_{PTH}	2.5	%
V_{HYST}	V_{RST} hysteresis					30		mV
V_{OL}	Low voltage output	I_{SINK} = 1.2mA, $V_{CC} \geq$ 2.7V					0.3	V
		I_{SINK} = 200µA, V_{CC} = 1.2V					0.3	V
t_{PRTO}	Programmable reset pulse width		RTO1	RTO0				
			0	0	20	25	30	ms
			0	1	35	50	65	ms
			1	0	65	100	135	ms
			1	1	130	200	270	ms
t_{DRST}	V in to RESET# delay	100mV overdrive				20		µs

2047 Elect TableA 4.2

Symbol	Parameter	Notes			Min.	Typ.	Max.	Unit
t_{PWDTO}	Programmable Watchdog timer period	WD2	WD1	WD0				
		0	0	0		OFF		—
		0	1	1		400		ms
		1	0	0		800		
		1	0	1		1600		
		1	1	0		3200		
		1	1	1		6400		
t_{PLDTO}	Programmable Longdog timer period		LD1	LD0				
			0	0		OFF		—
			0	1		1600		ms
			1	0		3200		
			1	1		6400		
$t_{PDLY}X$	Programmable delay from V_{PTH} to PUP# out		PUP#X-1	PUP#X-0				
			0	0		OFF		—
			0	1		25		ms
			1	0		50		
			1	1		100		
I_{MR}	MR# pullup current					100		µA
T_{MR}	MR# input pulse width					300		ns
T_{DMRRST}	Delay from MR# low to RESET# low					200		ns
V_{IL}	Input threshold						0.6	V
V_{IH}					$0.7 \times V_{CC}$			V

2047 Elect TableB 4.2

PIN DESCRIPTIONS

V_0, V_1, V_2, V_3 (16, 2, 3, 14)

These inputs are used as the voltage monitor inputs and as the voltage supply for the SMS44. Internally they are diode ORed and the input with the highest voltage potential will be the default supply voltage.

The RESET# output will be true if any one of the four inputs is above 1V. However, for full device operation at least one of the inputs must be at 2.7V or higher.

The sensing threshold for each input is independently programmable in 20mV increments from 0.9V to 6.0V. Also, the occurrence of an under- or over-voltage condition that is detected as a result of the threshold setting can be used to generate subsequent action(s), such as RESET# or IRQ#. The programmable nature of the threshold voltage eliminates the need for external voltage divider networks.

GND

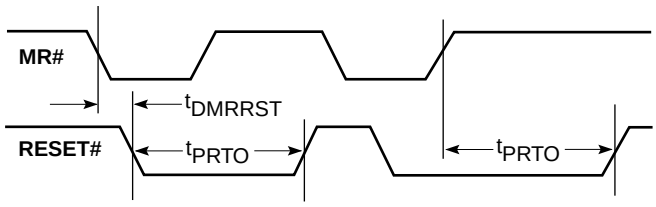
Power supply return.

MR# (1)

The manual reset input always generates a RESET# output whenever it is driven low. The duration of the RESET# output pulse will be initiated when MR# goes low and it will stay low for the duration of MR# low plus the programmed reset time-out period (t_{PRTO}). If MR# is brought low during a power-on cascade of the PUP#s the cascade will be halted for the reset duration, and will then resume from the point at which it was interrupted. MR# must be held low during a configuration register Write or Read. This signal is pulled down internally through a 70kΩ resistor, consequently the part is normally in reset mode when powered down.

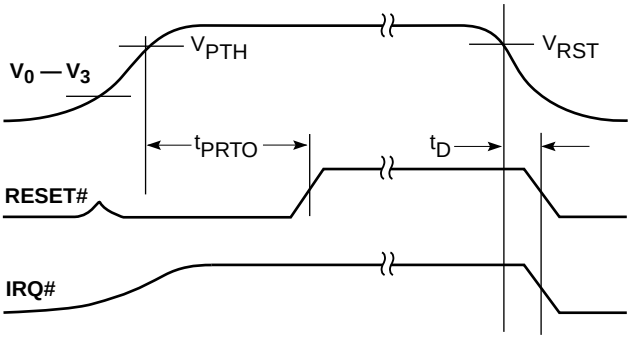
RESET# (11)

The reset output is an active low open drain output. It will be driven low whenever the MR# input is low or whenever an enabled under-voltage or over-voltage condition exists, or when a longdog timer expiration exists. The four voltage monitor inputs are always functioning, but their ability to generate a reset is programmable (**configuration register 4**). Refer to Figures 2 and 3 for a detailed illustration of the relationship between MR#, IRQ#, RESET# and the V_{IN} levels. This signal is pulled up internally through a 70kΩ resistor.



2047 Fig02 2.0

Figure 2. RESET# Timing with MR#



2047 Fig03 2.0

Figure 3. RESET# Timing with IRQ#

IRQ# (12)

The interrupt output is an active low open-drain output. It will be driven low whenever the watchdog timer times out or whenever an enabled under-voltage or over-voltage condition on a V input exists (**configuration register 6**). This signal is pulled up internally through a 70kΩ resistor.

WLDI (15)

Watchdog and longdog timer interrupt input. A low to high transition on the WLDI input will clear both the watchdog and longdog timers, effectively starting a new time-out period. This signal is pulled down internally through a 70kΩ resistor.

If WLDI is stuck low and no low-to-high transition is received within the programmed t_{PWDTO} period (programmed watch dog time-out) IRQ# will be driven low. If a transition is still not received within the programmed t_{PLDTO} period (programmed longdog time-out) RESET# will be driven low. Refer to Figure 4 for a detailed illustration.

Holding WLDI high will block interrupts from occurring but will not block the longdog from timing out and generating a reset. Refer to Figure 4 for a detailed illustration of the relationship between IRQ#, RESET#, and WLDI.

A1, A2 (6, 7)

A1 and A2 are the address inputs. When addressing the SMS44 memory or configuration registers the address inputs distinguish which one of four possible devices sharing the common bus is being addressed. These signals are pulled down internally through 70kΩ resistors.

SDA (9)

SDA is the serial data input/output pin. It should be tied to V_{CC} through a pull-up resistor.

SCL (10)

SCL is the serial clock input. It should be tied to V_{CC} through a pull-up resistor.

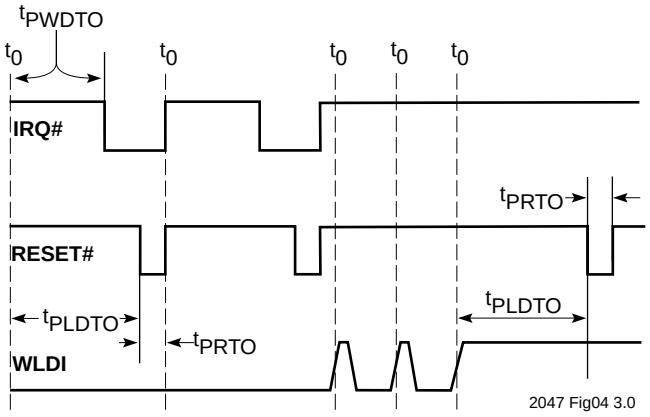


Figure 4. Watchdog, Longdog and WLDI Timing

PUP#1, PUP#2, PUP#3 (4, 5, 13)

These are the power-up permitted outputs when the SMS44 is programmed to provide the cascading of LDOs or DC/DC converters (***see Figures 1 and 5 for illustrations of cascading***). Each delay is independently enabled and programmable for its duration (**configuration register 7**). If all PUP# outputs are enabled the order of events would be as follows: V_0 above threshold then delay to PUP#1 turning on; V_1 above threshold then delay to PUP#2 turning on; V_2 above threshold then delay to PUP#3 turning on. The delays are programmable. These signals are pulled up internally through 70kΩ resistors.

DEVICE OPERATION

SUPPLY AND MONITOR FUNCTIONS

The V_0, V_1, V_2, and V_3 inputs are internally diode-ORed so that any one of the four can act as the device supply. The RESET# output will be guaranteed true so long as one of the four pins is at or above 1V.

> **Note***: for performing a memory operation (Read or Write) and to have the ability to change configuration register contents at least one supply input must be above 2.7V.*

Read/Write operations require a 0.01µF capacitor from the highest Vx input (normally V0) to GND. For optimum performance connect capacitors from each of the Vx inputs to GND. Locate the capacitors as physically close to the SMS44 as possible.

If cascading is enabled, the designer must insure V_0 is the primary supply and is the first to become active.

Associated with each input is a comparator with a programmable threshold for detection of under-voltage conditions on any of the four supply inputs. The threshold can be programmed in 20mV increments anywhere within the range of 0.9V to 6.0V. Configuration registers 0, 1, 2, and 3 adjust the thresholds for V_0, V_1, V_2, and V_3 respectively.

If the value contained in any register is all zeroes, the corresponding threshold will be 0.9V. If the contents were 05_{HEX} the threshold would then be 1.0V [0.9V + (5 × 0.02V)]. All four registers are configured as 8-Bit registers.

D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	Action
1	1	1	1	1	1	1	1	Highest threshold adjustment = 6.0V
0	0	0	0	0	0	0	0	Lowest threshold adjustment = 6.0V
0	0	0	0	0	1	1	0	Threshold = 0.9V + (6 × 0.02V) = 1.02V *(e.g.)*

2047 Table01

Table 1. Configuration Registers 0, 1, 2, and 3

RESET AND IRQ FUNCTIONS

Both the reset and interrupt outputs have four programmable sources for activation. Configuration register 4 is used for selecting the activation source, which can be any combination of V_0, V_1, V_2 and V_3. A monitor input can only be programmed to activate on either an under-voltage or over-voltage condition, but not both conditions.

The RESET# output will become active when triggered by a selected activation source such as an under-voltage condition on V1. When this condition ceases, the RESET# output will remain active for t_{PRTO} (programmable reset time-out). This reset time-out interval takes priority over the PUP outputs for use of the timer.

D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB
V_3	V_2	V_1	V_0	V_3	V_2	V_1	V_0
RESET Trigger Source				IRQ Trigger Source			

2047 Table02

Table 2. Configuration Register 4

The RESET# output has two hardwired sources for activation: the MR# input, and the expiration of the Longdog timer. RESET# will remain active so long as MR# is low, and will continue driving the RESET# output for t_{PRTO} (programmable reset time out) after MR# returns high. The MR# input cannot be bypassed or disabled. The Longdog timer can be bypassed by programming it to the off or idle mode.

The sole hardwired source for driving the IRQ# output low is the watchdog. The IRQ# circuitry is disabled during initial power up until the reset condition has terminated and the reset interval (t_{PRTO}) has timed out. The IRQ# output is cleared by a low-to-high transition of the WLDI signal. It can effectively be bypassed by programming it to the off or idle mode. Refer to Figures 2, 3 and 4 for a detailed illustration of the relationships among the affected signals.

The SMS44 also provides the option of the monitors triggering on either an under-voltage or over-voltage condition. The low-order four bits of configuration register 5 program these options.

Action	D3 MSB	D2	D1	D0 LSB
	V_3	V_2	V_1	V_0
Writing a 0 enables undervoltage detection for the selected V input	0	0	0	0
Writing a 1 enables overvoltage detection for the selected V input	1	1	1	1

2047 Table03

Table 3. Configuration Register 5 (D0 through D3)

The high order four bits of configuration register 5 are Read only, and their state indicates the sources of interrupts. Whenever an interrupt is generated the status of the V inputs will be recorded in the status register. The status will remain in the register until the device is powered-down or another interrupt occurs that overwrites the previous status.

If an interrupt occurs and no bits are set the default assumption must be the watchdog generated the interrupt.

D7 MSB	D6	D5	D4 LSB	Action
V_3	V_2	V_1	V_0	
0	0	0	0	Reading a 1 indicates the source of the interrupt
1	1	1	1	

2047 Table04

Table 4. Configuration Register 5 (D4 through D7)

WATCHDOG AND LONGDOG TIMERS

The SMS44 contains two timers that can be programmed independently. The Watchdog is intended to be of shorter duration and will generate an interrupt if it times out. The Longdog timer will generally be programmed to be of longer duration than the watchdog and it will generate a reset if it times out. Both timers are cleared by a low to high transition on WLDI and they both start simultaneously.

If the watchdog should time-out the device status will be recorded in the status register. If the Longdog times out RESET# will be driven low either until a WLDI clear is received or until t_{PRTO} (whichever occurs first), at which time it will return high. Refer to Figure 4 which illustrates the action of RESET# and IRQ# with respect to the Watchdog and Longdog timers and the WLDI input.

D7 MSB	D6	D5	D4	D3	Action
CAS	RTO1	RTO0	LD1	LD0	
x	x	x	**0**	**0**	Longdog Off
x	x	x	**0**	**1**	1600ms
x	x	x	**1**	**0**	3200ms
x	x	x	**1**	**1**	6400ms
x	**0**	**0**	x	x	t_{PRTO} = 25ms
x	**0**	**1**	x	x	t_{PRTO} = 50ms
x	**1**	**0**	x	x	t_{PRTO} = 100ms
x	**1**	**1**	x	x	t_{PRTO} = 200ms
0	x	x	x	x	Cascade On
1	x	x	x	x	Cascade Off

2047 Table05

Table 5. Configuration Register 6 (D3 through D7)

Action	D2	D1	D0 LSB
	WD2	WD1	WD0
OFF	0	0	0
400ms	0	1	1
800ms	1	0	0
1600ms	1	0	1
3200ms	1	1	0
6400ms	1	1	1

2047 Table06 1.0

Table 6. Configuration Register 6 (D0, D1, D2)

If WLDI is held low the timers will free-run generating a series of interrupts and resets. If WLDI is held high the interrupt (watchdog) output will be disabled and only the reset (Longdog) output will be active.

When the Longdog times out RESET# will be generated. When RESET# returns high (after t_{PRTO} or after a WLDI strobe) both timers are reset to time zero. Therefore, if the Longdog t_{PLDTO} is equal to or shorter than the watchdog t_{PWDTO}, RESET# will effectively clear the interrupt before it can drive the output low.

Register 6 is also used to set the programmable reset time-out period (t_{PRTO}) and to select the cascade option.

Cascade Delay Programming

The cascade delays are programmed in register 7. Bit 7 of register 6 must be set to a 0 in order to enable the cascading of the PUP# outputs. Cascading will not commence until V_0 is above its programmed threshold.

Each PUP# (-3, -2 and -1) is delayed according to the states of its Bit 1 and Bit 0 as indicated in Table 9. Refer to Figures 1 and 5 for the detailed timing relationship of the programmable power-on cascading.

The delay from V_{PTH0} until PUP#1 low is t_{PDLY1}. There is a similar t_{PDLYX} delay for V1 to PUP#2 and V2 to PUP#3. They are programmed in register 7. Cascading will always occur as indicated in the flow chart (Figure 7).

D7 MSB	D6	Action
Address Select		
Lock	AS0	
x	**0**	DTI = 1010, responds only when address bits = A2 & A1 logic states
x	**1**	DTI = 1011, responds only when address bits = A2 & A1 logic states
0	x	Config. Reg. Read/Write enabled
1	x	Config. Reg. Read/Write locked out

2047 Table07 3.0

Table 7. Configuration Register 7 (D7, D6)

D5	D4	D3	D2	D1	D0 LSB
PUP#3		PUP#2		PUP#1	
Bit 1	Bit 0	Bit 1	Bit 0	Bit 1	Bit 0

2047 Table08 3.0

Table 8. Configuration Register 7 (D5 through D0)

Bit 1	Bit 0	t_{PDLYX}
0	0	0ms (no) Delay
0	1	25ms Delay
1	0	50ms Delay
1	1	100ms Delay

2047 Table09 1.0

Table 9. PUP Delays, Configuration Register 7

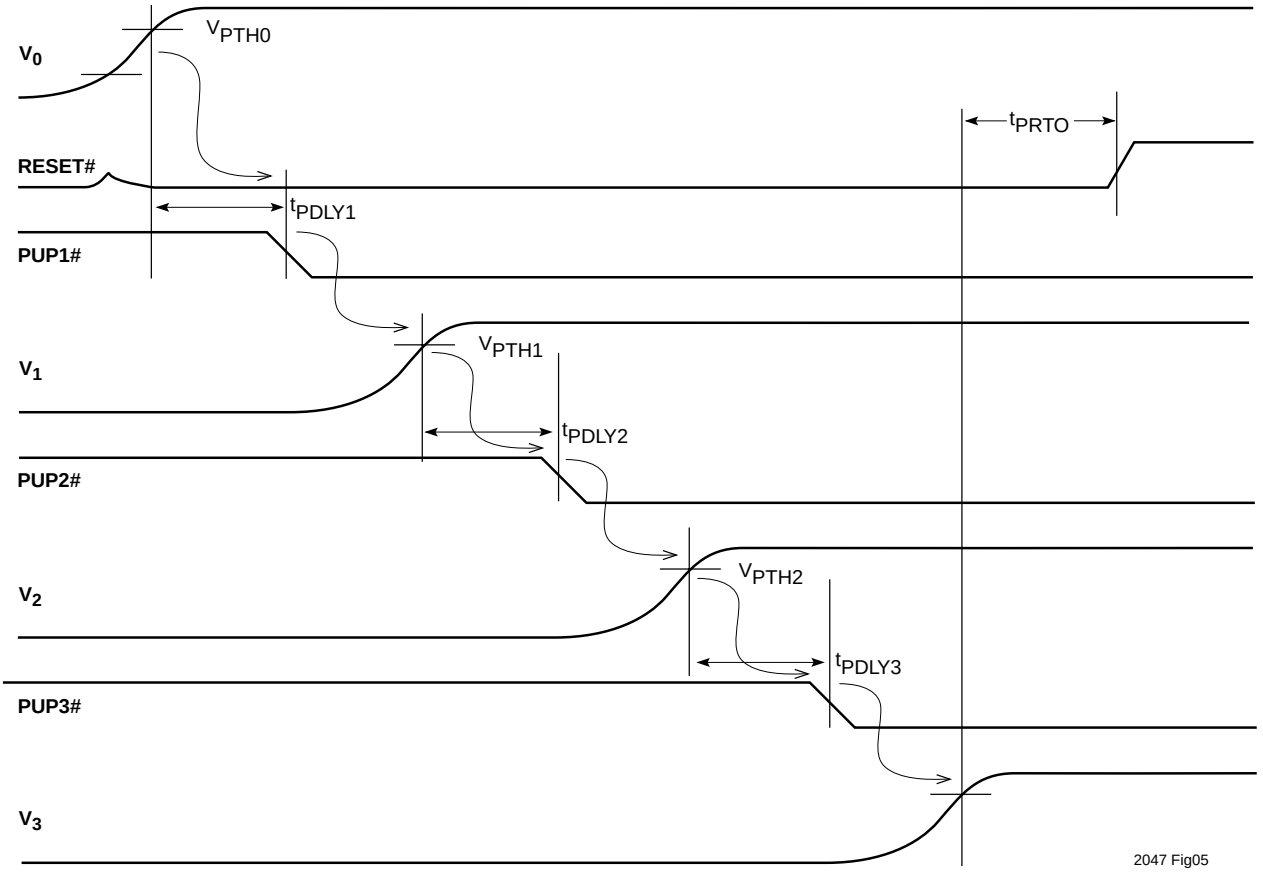


Figure 5. V_X Input and Resulting PUP# Cascade (RESET# set to trip on V_3 Undervoltage)

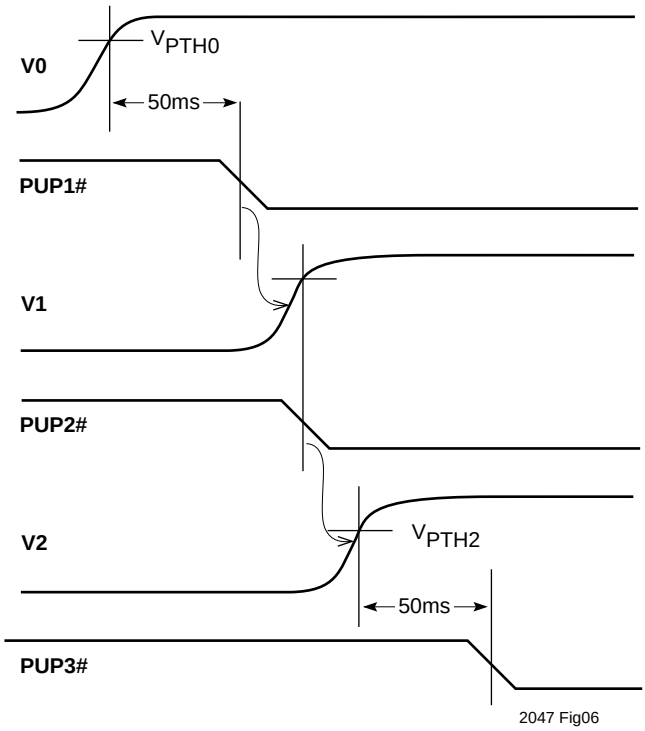


Figure 6. Timing with Register 7 Contents 22_{HEX}

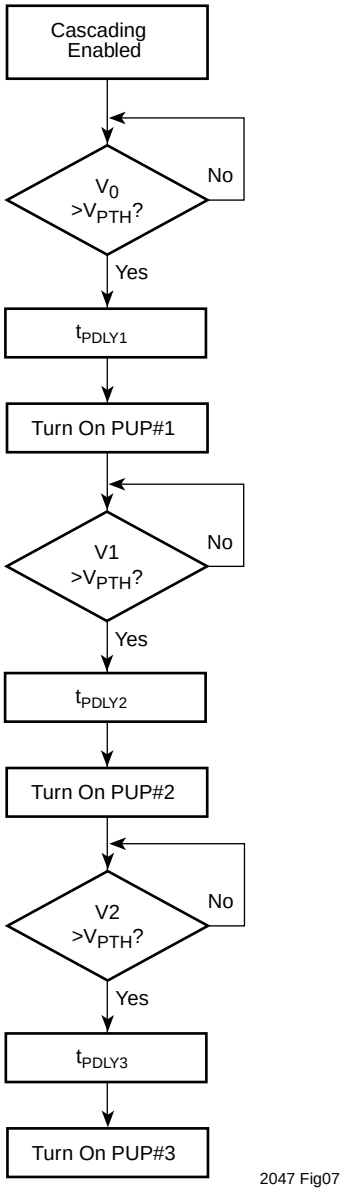


Figure 7. Cascade Flow Chart

HOOKUP

HARDWARE

The end user can use the summit SMX3200 programming cable and software that have been developed to operate with a standard personal computer. The programming cable interfaces directly between a PC's parallel port and the target application. The application's values are entered via an intuitive graphical user interface employing drop-down menus. See also Figure 13.

After the desired settings for the application are determined the software will generate a hex file that can be transferred to the target device or downloaded to Summit. If it is downloaded to Summit a customer part number will be assigned and the file will be used to customize the devices during the final electrical test operations.

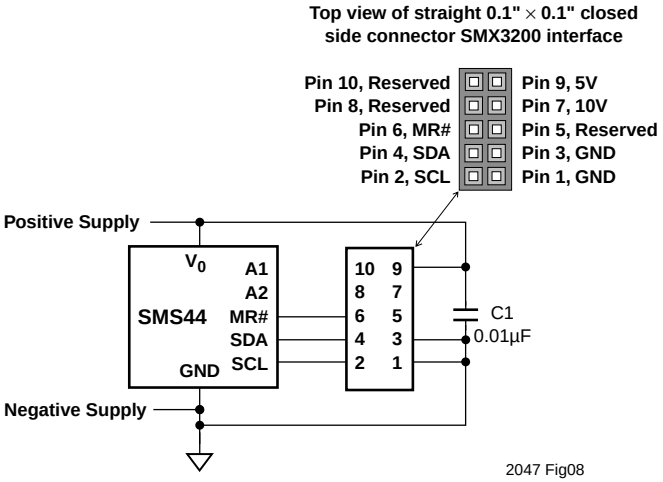


Figure 8. Programming Hookup

INTERFACE

MEMORY OPERATION

Data for the configuration registers and the memory array are read and written via an industry standard two-wire interface. The bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are a serial data line (SDA) and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus. See Memory Operating Characteristics: Table 10 and Figure 9.

Input Data Protocol

The protocol defines any device that sends data onto the bus as a transmitter and any device that receives data as a receiver. The device controlling data transmission is called the Master and the controlled device is called the Slave. In all cases the SMS44 will be a Slave device, since it never initiates any data transfers.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock high time because changes on the data line while SCL is high will be interpreted as start or stop condition.

Symbol	Parameter	Conditions	Min.	Max.	Units
f_{SCL}	SCL clock frequency		0	100	kHz
t_{LOW}	Clock low period		4.7		µs
t_{HIGH}	Clock high period		4.0		µs
t_{BUF}	Bus free time (1)	Before new transmission	4.7		µs
$t_{SU:STA}$	Start condition setup time		4.7		µs
$t_{HD:STA}$	Start condition hold time		4.0		µs
$t_{SU:STO}$	Stop condition setup time		4.7		µs
t_{AA}	Clock edge to valid output (1)	SCL low to valid SDA (cycle n)	0.3	3.5	µs
t_{DH}	Data Out hold time (1)	SCL low (cycle n+1) to SDA change	0.3		µs
t_R	SCL and SDA rise time (1)			1000	ns
t_F	SCL and SDA fall time (1)			300	ns
$t_{SU:DAT}$	Data In setup time (1)		250		ns
$t_{HD:DAT}$	Data In hold time (1)		0		ns
TI	Noise filter SCL and SDA (1)	Noise suppression		100	ns
t_{WR}	Write cycle time			5	ms

Note (1): These values are guaranteed by design.

2047 Table10 4.0

Table 10. Memory Operating Characteristics

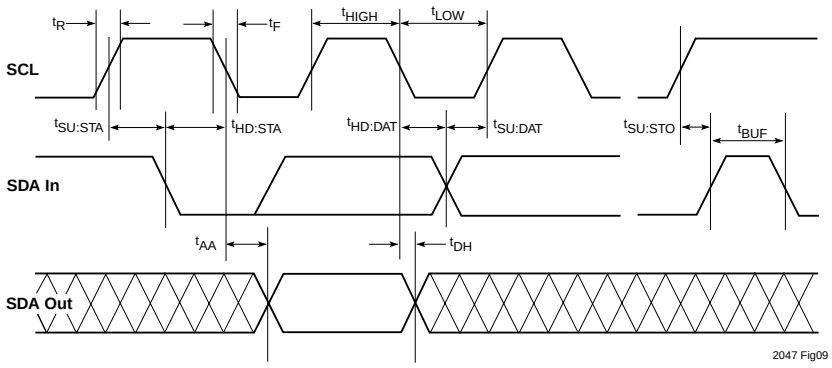


Figure 9. Memory Operating Characteristics

START and STOP Conditions

When both the data and clock lines are high the bus is said to be not busy. A high-to-low transition on the data line, while the clock is high, is defined as the Start condition. A low-to-high transition on the data line, while the clock is high, is defined as the Stop condition. See Figure 10.

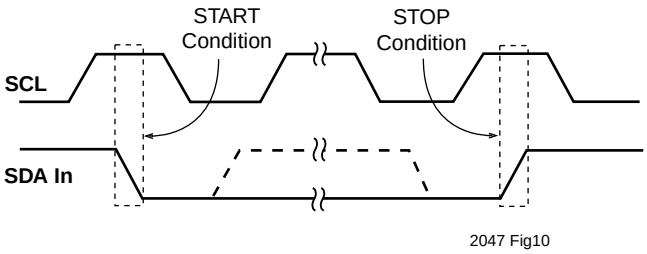


Figure 10. START and STOP Conditions

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the Master or the Slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line low to Acknowledge that it received the eight bits of data. The Master will leave the SDA line high (NACK) when it terminates a read function.

The SMS44 will respond with an Acknowledge after recognition of a Start condition and its slave address byte. If both the device and a write operation are selected the SMS44 will respond with an Acknowledge after the receipt of each subsequent 8-Bit word. In the READ mode the SMS44 transmits eight bits of data, then releases the SDA line, and monitors the line for an Acknowledge signal. If an Acknowledge is detected and no Stop condition is generated by the Master, the SMS44 will continue to transmit data. If a NACK is detected the SMS44 will terminate further data transmissions and await a Stop condition before returning to the standby power mode.

Device Addressing

Following a Start condition the Master must output the address of the Slave it is accessing. The most significant four bits of the Slave address are the device type identifier/address. For the SMS44 the default is 1010_{BIN}. The next two bits are the Bus Address. The next bit (the 7th) is the MSB of the memory address.

D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB
Address Bits							
Device Type				Bus		MSB	R/W
SMS44				x	x	x	x
1	0	0	1	⇦ Configuration Register			
1	0	1	0	⇦ Memory (default)			
1	0	1	1	⇦ Alternate Memory			

2047 Table11 1.0

Table 11. Slave Addresses

Read/Write Bit

The last bit of the data stream defines the operation to be performed. When set to 1 a Read operation is selected; when set to 0 a Write operation is selected.

WRITE OPERATIONS

The SMS44 allows two types of Write operations: byte Write and page Write. A byte Write operation writes a single byte during the nonvolatile write period (t_{WR}). The page Write operation, limited to the memory array, allows up to 16 bytes in the same page to be written during t_{WR}.

Byte Write

After the Slave address is sent (to identify the Slave device and select either a Read or Write operation), a second byte is transmitted which contains the low order 8 bit address of any one of the 512 words in the array. Upon receipt of the word address the SMS44 responds with an Acknowledge. After receiving the next byte of data it again responds with an Acknowledge. The Master then terminates the transfer by generating a Stop condition, at which time the SMS44 begins the internal Write cycle. While the internal Write cycle is in progress the SMS44 inputs are disabled and the device will not respond to any requests from the Master.

Page Write (memory only)

The SMS44 is capable of a 16-byte page Write operation. It is initiated in the same manner as the byte Write operation, but instead of terminating the Write cycle after the first data word the Master can transmit up to 15 more bytes of data. After the receipt of each byte the SMS44 will respond with an Acknowledge.

The SMS44 automatically increments the address for subsequent data words. After the receipt of each word the low order address bits are internally incremented by one.

The high order bits of the address byte remain constant. Should the Master transmit more than 16 bytes, prior to generating the Stop condition, the address counter will rollover and the previously written data will be overwritten. As with the byte Write operation, all inputs are disabled during the internal Write cycle. Refer to Figure 11 for the address, Acknowledge, and data transfer sequence.

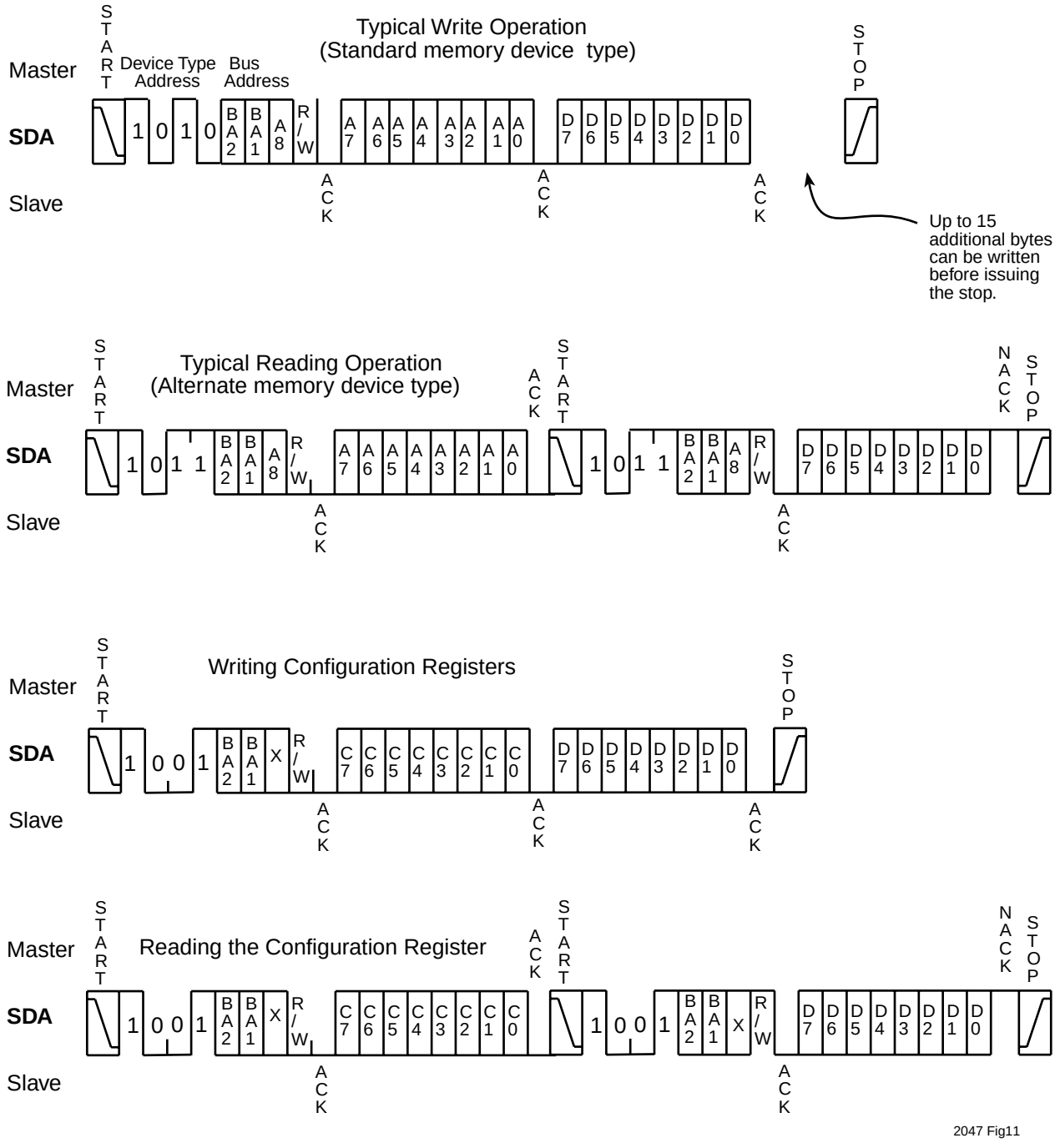


Figure 11. Read and Write Operations

Acknowledge Polling

When the SMS44 is performing an internal Write operation it will ignore any new Start conditions. Since the device will only return an acknowledge after it accepts the Start the part can be continuously queried until an acknowledge is issued, indicating that the internal Write cycle is complete. See the flow chart for the proper sequence of operations for polling.

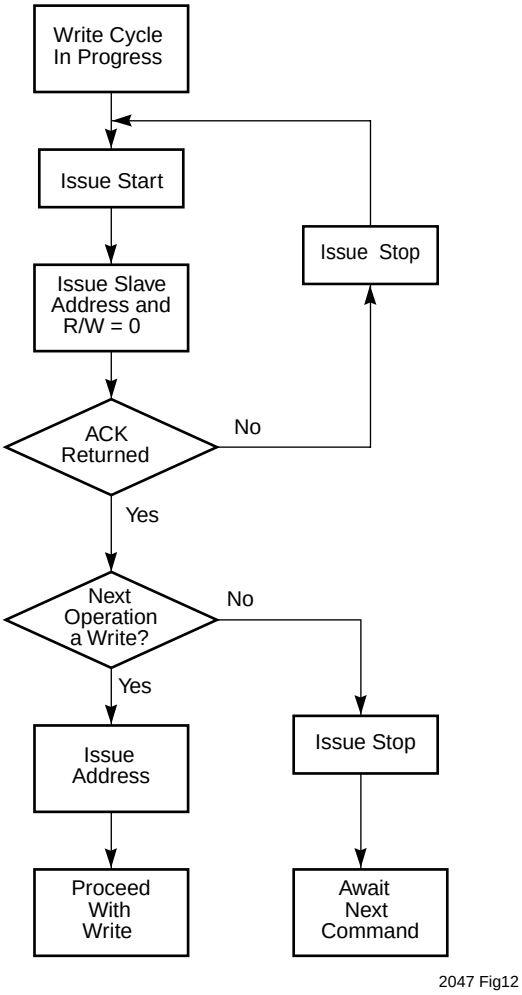


Figure 12. Write Flow Chart

READ OPERATIONS

Read operations are initiated with the R/W bit of the identification field set to 1. There are two different Read options: 1. Current Address Byte Read, and 2. Random Address Byte Read.

Current Address Read (memory only)

The SMS44 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a Read or Write) was to address location n, the next Read operation would access data from address location n+1 and increment the current address pointer. When the SMS44 receives the Slave address field with the R/W bit set to 1 it issues an acknowledge and transmits the 8-Bit word stored at address location n+1. The current address byte Read operation only accesses a single byte of data. The Master sets the SDA line to NACK and generates a stop condition. At this point the SMS44 discontinues data transmission.

Random Address Read (Register and Memory)

Random address Read operations allow the Master to access any memory location in a random fashion. This operation involves a two-step process. First, the Master issues a write command which includes the start condition and the Slave address field (with the R/W bit set to Write), followed by the address of the word it is to Read. This procedure sets the internal address counter of the SMS44 to the desired address. After the word address acknowledge is received by the Master it immediately reissues a Start condition, followed by another Slave address field with the R/W bit set to READ. The SMS44 will respond with an Acknowledge and then transmit the 8 data bits stored at the addressed location. At this point the Master sets the SDA line to NACK and generates a Stop condition. The SMS44 discontinues data transmission and reverts to its standby power mode.

Sequential READ (Memory Only)

Sequential Reads can be initiated as either a current address Read or random access Read. The first word is transmitted as with the other byte Read modes (current address byte Read or random address byte Read); however, the Master now responds with an Acknowledge, indicating that it requires additional data from the SMS44. The SMS44 continues to output data for each Acknowledge received. The Master terminates the sequential Read operation by responding with a NACK, and issues a Stop condition. During a sequential Read operation the internal address counter is automatically incremented with each Acknowledge signal. For Read operations all address bits are incremented, allowing the entire array to be read using a single Read command. After a count of the last memory address the address counter will rollover and the memory will continue to output data.

APPLICATIONS

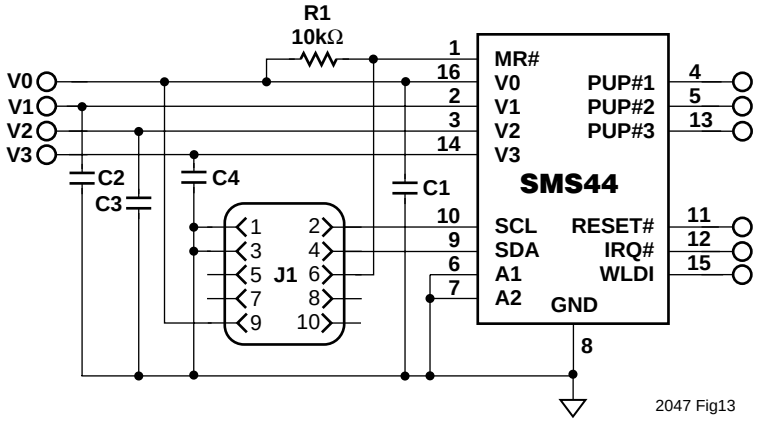


Figure 13. Application Schematic

NOTES:

1. C1, C2, C3 and C4 are all 0.01µF.
2. C1 is required for Read/Write operations.
3. C2, C3, and C4 are recommended for noisy environments and whenever input voltages are near the OV and/or UV reset level trip points.
4. Connector J1 is an SMX3200 (see Figure 8).
5. The signal MR# has an internal pull-down resistor. Resistor R1 is required to provide pull-up.

ORDERING INFORMATION

SMS44 G

Base Part Number

Package
G = SSOP
S = SOIC

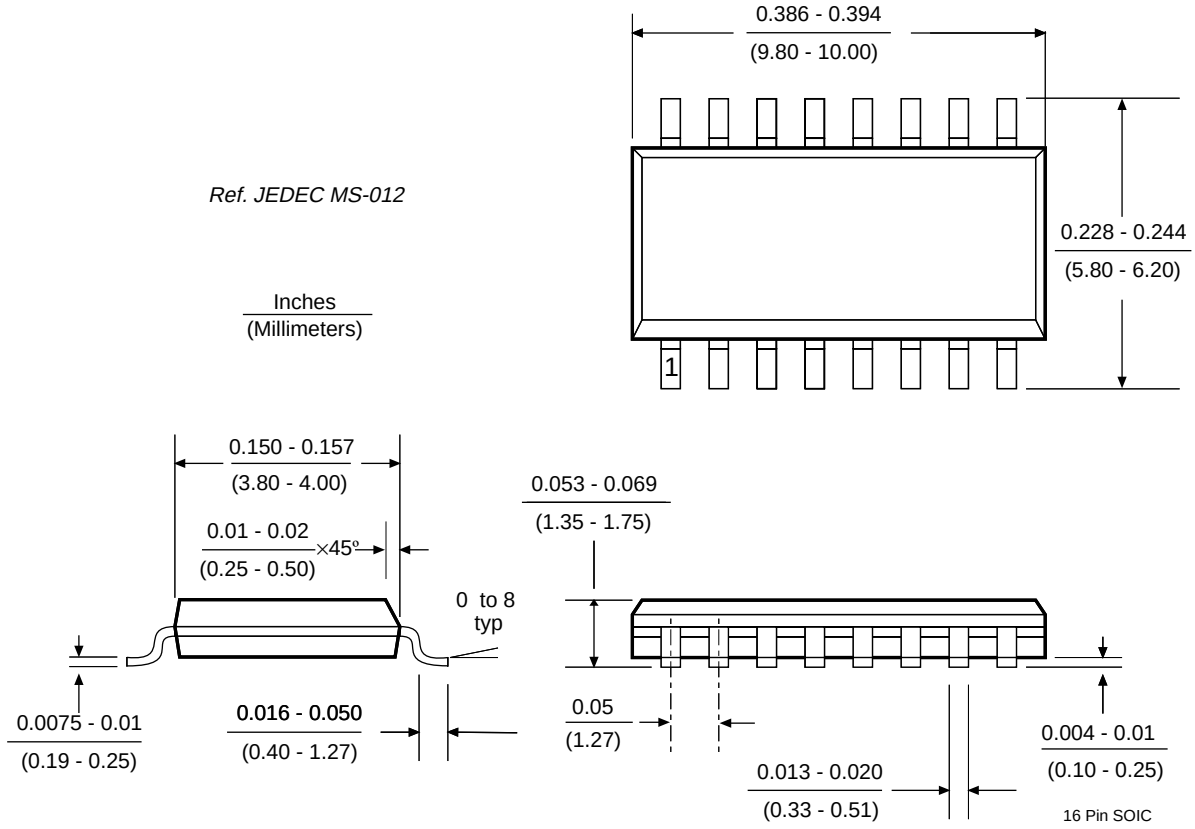
2047 Tree 1.0

PACKAGES

16 PIN SOIC PACKAGE

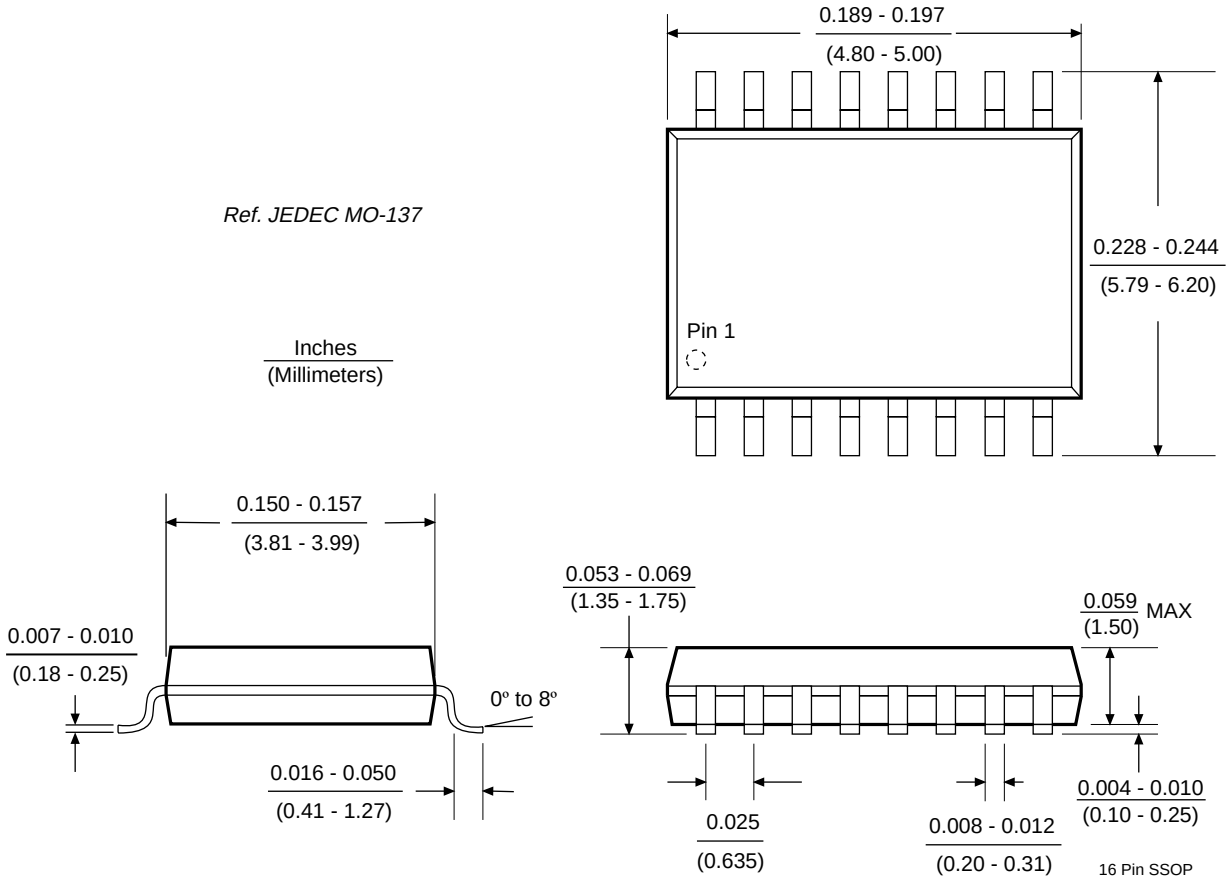
Ref. JEDEC MS-012

Inches
(Millimeters)



16 Pin SOIC

16 PIN SSOP PACKAGE



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