SBT3100 Bluetooth™ MAC Controller

PRELIMINARY SPECIFICATION

Product Description:

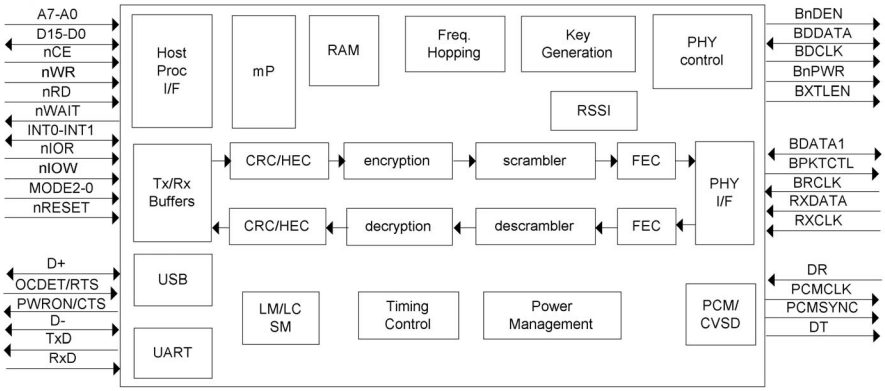
The SBT3100 Bluetooth™ MAC Controller IC is part of Signia's complete Bluetooth™ solution that includes RF and Baseband chipsets, antennas, software protocol stacks and reference designs.

The SBT3100 provides Bluetooth™ Link Control and Link Management functions that support up to 8 voice/data channels compliant with the Bluetooth™ Specification 1.0B. The SBT3100 contains an on-board microprocessor and static RAM for easy implementation in notebook PCs, PDAs, internet appliances and other devices requiring low power, cost effective Bluetooth™ functionality.

The SBT3100 is optimized for use with Signia's SBT5010 Bluetooth™ transceiver for use in Bluetooth™ applications in the globally available ISM band operating in the 2.4-2.5 GHz frequency range. A low pin count transceiver interface complies with the BlueRF™ standard for bi-directional communication, allowing interoperability with the SBT5010 and other BlueRF™ compliant transceivers. It consists of a three wire RF bus for transmit, receive and control data, a three wire serial data bus for general control data, and power management.

This product is available in industry standard packaging.

Block Diagram:



Key Features:

- A component of Signia's family of complete hardware and software Bluetooth™ solutions and is optimized for use with Signia's SBT5010 Transceiver
- Encryption/decryption, and authentication key generation enhanced by on-chip hardware accelerator
- Supports pico-net and scatter-net protocols
- Contains a complete implementation of Bluetooth™ link management functions
- Hardware implemented Bluetooth™ link control functions
- Compliant to Bluetooth™ specification version 1.0B and BlueRF™ interface
- Fully supports all SCO and ACL traffic channels
- Transmit/receive buffer management for reduced buffer size
- Support for transmit power control for long range applications.
- Support for RSSI channel quality measurement for each link
- Provides power management for active, sniff, hold and park modes
- Support for PCM A-law/μ-law and CVSD codec
- Supports PCMCIA, USB and UART interfaces

Applications:

- Battery Powered Portable and Handheld Devices
- Laptop Computers
- PDAs
- Modems and Internet Access Points
- Cordless and Cellular Phones
- PCMCIA or CompactFlash

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Ratings

Absolute Maximum Ratings					
Parameter	**Symbol**	**Rating**			**Units**
		MIN	**TYP**	**MAX**	
Operating Temperature	T_{OP}	-20		+85	°C
Storage Temperature	T_{ST}	-55		+125	°C
Supply Voltage to Core	V_{DD}	+2.25		+3.0	V
Supply Voltage to I/O	V_{DD_IO}	+2.25		+3.6	V
Applied Voltages to Other Pins	V_{IN}	-0.3		+3.0	V

Notes:

1. Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics section below.
2. These devices are electro-static sensitive. Devices should be transported and stored in anti-static containers. Equipment and personnel contacting the devices need to be properly grounded. Cover work benches with grounded conductive mats.
3. Information given in this data sheet is believed to be accurate and reliable at the time of printing. However, Signia reserves the right to make changes to products and specifications without notice.

Electrical Characteristics

The following specifications are guaranteed for T_A = 25 °C, V_{DD} = 2.5V**,** unless otherwise noted

Parameter	Symbol	Specification			Units	Condition
		MIN	**TYP**	**MAX**		
DC Specifications						
V_{DD} supply Voltage - Core	V_{DD}	2.25	2.5	2.75	V	
V_{DD_IO} supply Voltage - IO	$\mathbf{V_{DD\_IO}}$	2.25		3.3	V	
Current Consumption - Connection	I_{DD_CONN}		15		mA	V_{DD}=2.5V, $\mathbf{V_{DD\_IO}}$=2.5V
Current Consumption - Peak	I_{DD_PEAK}		30		mA	V_{DD}=2.5V, $\mathbf{V_{DD\_IO}}$=2.5V
Current Consumption - Standby (Idle)	I_{DD_SB}		0.5		mA	V_{DD}=2.5V, $\mathbf{V_{DD\_IO}}$=2.5V
Digital Inputs						
Logic input high	V_{IH}	0.7 $\mathbf{V_{DD\_IO}}$		$\mathbf{V_{DD\_IO}}$	V	
Logic input low	V_{IL}	-0.1		0.3 $\mathbf{V_{DD\_IO}}$	V	
High Level Input Current	I_{IH}			10	µA	
Low Level Input Current	I_{IL}	-10			µA	
Digital Outputs						
Logic output high	V_{OH}	0.9 $\mathbf{V_{DD\_IO}}$		$\mathbf{V_{DD\_IO}}$	V	
Logic output low	V_{OL}	0		0.1 $\mathbf{V_{DD\_IO}}$	V	
Output High Current	I_{OH}			4.0	mA	
Output Low Current	I_{OL}	-4.0			mA	

Functional Description

The SBT3100 provides all the Bluetooth™ Link Control (LC) functions, real-time activities as well as channel related DSP functions implemented in hardware. The Bluetooth™ Link Management (LM) and Host Communication Interface (HCI) functions are performed on-chip in SBT3100 as well to enable the host communication over the Bluetooth™ link.

The channel related DSP functions such as Forward Error Correction (FEC), Scrambler, encryption, key generation, CRC/HEC and access code correlator are

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implemented in hardware. The PCM/CVSD audio transcoder functions are also incorporated in the DSP function block.

The real-time functions include TDMA/TDD timing control, TX/RX frequency hopping calculation, RF front-end programming and symbol timing synchronization. The call processing state control, Bluetooth™ sub-system power management and link quality measurements are also supported by the SBT3100.

PHY I/F – Physical Layer Interface

The SBT3100 can be programmed to support either BlueRF or Signia's proprietary Interfaces for transmit and receive data.

When the SBT3100 interfaces with BlueRF compatible PHY device, the SBT3100 will burst out transmit data at symbol rate in the transmit mode. In the receive mode, RXMODE2 is supported by SBT3100.

The SBT3100 can also receive recovered symbol clock and recovered demodulated data from Bluetooth™ PHY device in the Signia's proprietary interface mode.

FEC – Forward Error Correction

The channel encoding and decoding for the FEC are applied to the Bluetooth™ packet based on the transmit/receive packet type. FEC rate of 1/3 and 2/3 are implemented to combat the noisy environments. The FEC error checking results are also used for measuring the link quality.

Scrambler/De-scrambler

The main purpose of scrambling the transmit data is to prevent any unwanted DC offset due to the long sequences of 1's or 0's. The data transients will also help the symbol clock tracking performance.

Encryption/Decryption

The SBT3100 provides encryption/decryption engine in hardware for data security compliant to the Bluetooth™ encryption Specification. The encryption/decryption is initialized every transmit/receive slot automatically once the encryption mode is set on a particular traffic channel.

CRC/HEC – Cyclic Redundancy Check/Header Error Check (Correction)

In order to execute the re-transmission scheme, the ACL packet payload can be protected by the CRC. If the CRC error is detected on the receive side, proper action will be taken in the Link Control (LC).

Bluetooth™ packet header information is protected heavily by the error correction code. Upon receiving the packet on receiving side, the header field will be checked first to ensure correct packet header received.

Both CRC and HEC errors will be used to measure the link quality for a particular traffic channel.

TX/RX Buffers

5.5 Kbytes of buffer space are implemented in the SBT3100 to buffer multiple TX/RX packets. This buffer space is organized as multiple FIFO's and are dynamically assigned to different links for improved channel bandwidth and buffer usage. A Tx packet will stay in the buffer until it is transmitted (if no ACK is required), ack'ed (if one is required), or successfully broadcasted. A Rx packet will remain in the buffer until it is read by the host. When a packet is retired from the buffer, the FIFO it resided is recycled. To ensure correct packet sequencing, order of the buffers/packets is maintained.

PCM/CVSD Interface

The PCM A-law/μ-law and CVSD transcoding functions are implemented to support the Bluetooth™ audio requirements. The PCM coding block converts between A-law/μ-law and linear PCM voice data. The CVSD coding block provides conversion between CVSD coded data and linear voice samples.

PHY Control – Physical Layer Control Interface

The SBT3100 provides 3-wires Dbus serial interfaces specified in the BlueRF Specifications between the SBT3100 and PHY device. The PHY device internal registers (synthesizer programming, RF front-end, RSSI etc.) can be read/write access by the SBT3100.

Beside the serial bus communication, the SBT3100 also provides power down and sleep mode control to PHY device for power saving mode.

RSSI – Received Signal Strength Indicator

To monitor and maintain the channel quality of each traffic link, the SBT3100 provides link quality measurement algorithm based on receive signal strength, BER and FER.

Key Generation – Authentication/Encryption Key

In order to establish a communication link, the authentication process is performed between two devices. To protected Bluetooth™ air data, the encryption process is needed. The authentication keys and encryption key are generated using on chip key generation hardware block. The authentication key exchange and validation is also performed in hardware. The key generation and validation are carried out without any firmware intervened.

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Frequency Hopping

The Bluetooth™ standard uses frequency hopping spread spectrum technique. The hopping sequences are based on the different call processing states, device address, time slot information as well as different country regulations. Since the frequency is programmed into the PHY device synthesizer before each transmit/receive slot, frequency hopping algorithm is performed in hardware to reduce the firmware overhead.

USB/UART

In addition to the bus-based Host Processor Interface, two separate USB and UART interfaces are also provided. The USB interface follows the standard USB v1.1 specification and can be configured as a device or as a hub.

The UART interface implements a 4-wire subset (TxD/RxD/nRTS/nCTS) of the NS16550 and can be clocked at up to 1.5 Mbaud. Both the USB and the UART interface are used as transport-layer interface to carry commands and data from the host to the Bluetooth™ device. They are selected using the 3 mode bits mentioned above.4-wire UART interfaces is supported by the SBT3100.

LC State Machine

SBT3100 implements the complete Link Control function in hardware to relieve the host from the time-critical missions. The LC state machine maintains the FLOW, ARQN, and SEQN bits for each active ACL links to ensure a smooth and error-free transmission for each data packet. For SCO links, the LC maintains the TX/RX schedules and automatically merges DM1 and HV1 into DV packet when necessary. For master devices, the TX-scheduling is extended to include the ACL links so that multiple TX-packets from different ACL links can be queued in the TX buffer simultaneously.

Micro-Processor/RAM

SBT3100 implements all the time critical Link Management (LM) function in hardware to release the host processor from per-slot activities. All the link management timers such as the Npoll, Nsupervision, Tw_inquiry_scan, Tinquiry_scan, Tw_page_scan, Tpage_scan, etc. are implemented in hardware also in SBT3100. In addition, state machines that deal with Inquiry, Inquiry-Scan, Page, Page-Scan, Park modes as well as TDD switch are also done in the hardware. These supports should significantly reduce the complexity and time-critical-ness of the LM software running on the on-chip Microprocessor. The on-chip Micro-processor could provide processing power of handling higher layer protocol and application software which essentially supporting standalone Bluetooth™ platform with no additional host processor component.

The local RAM spaces are partitioned into program and data memories. The firmware and application programs for the microprocessor can be loaded into local program memory space from external Flash memory device via the memory interfaces. The SBT3100 can access up to 1M-byte external memory space.

Timing Control

Besides the coarse-grain, per-slot timing supports for the Link Control and Link Management, fine-grain timing control within a slot is also provided for better control over the RF timing. This is to accommodate the idiosyncrasies of different RF chips in synthesizer programming delays and TX/RX signal processing delays. Also provided in hardware are circuit to compute the slot-offset between the master and the slave clocks, and circuit to adjust the estimated master clock based on the slot-offset. Both are crucial to support inter-piconet and scatternet communications.

Power Management

The SBT3100 supports all the Bluetooth™ standby mode configurations. The standby mode includes sniff, hold and park modes. In the Bluetooth™ active mode, the active period of transmit and receive chains are also controlled. The other internal hardware blocks are shutdown in the different power saving modes.

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