®

SONET/SDH/ATM OC-48 8:1 TRANSMITTER | S3041

FEATURES

- Micro-power Bipolar technology
- Complies with Bellcore and ITU-T specifications
- On-chip high-frequency PLL for clock generation
- Supports 2.488 GHz (OC-48)
- Reference frequency of 155.52 MHz
- 8-bit LVDS data path
- Compact 100 TQFP/TEP package
- Diagnostic loopback mode
- Line loopback
- Lock detect
- Low jitter LVPECL interface
- Single 3.3V supply

APPLICATIONS

- SONET/SDH-based transmission systems
- SONET/SDH modules
- SONET/SDH test equipment
- ATM over SONET/SDH
- Section repeaters
- Add drop multiplexers
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

GENERAL DESCRIPTION

The S3041 SONET/SDH Mux chip is a fully integrated serialization SONET OC-48 (2.488 GHz) interface device. The chip performs all necessary parallel-to-serial and clock synthesis functions in conformance with SONET/SDH transmission standards. The device is suitable for SONET-based ATM applications. Figure 1 shows a typical network application.

On-chip clock synthesis PLL components are contained in the S3041 Mux chip allowing the use of a slower external transmit clock reference. The chip can be used with a 155.52 MHz reference clock, in support of existing system clocking schemes.

The low jitter LVPECL interface guarantees compliance with the bit-error rate requirements of the Bellcore and ITU-T standards. The S3041 is packaged in a 100 TQFP/TEP, offering designers a small package outline.

Figure 1. System Block Diagram
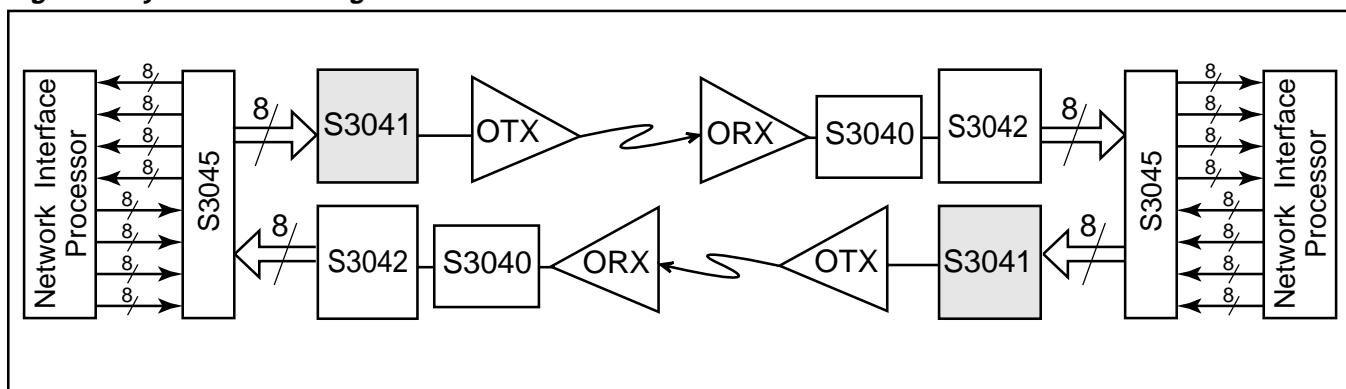
S3041 OVERVIEW

The S3041 Mux implements SONET/SDH serialization and transmission functions. The block diagram in Figure 2 shows basic operation of the chip. This chip can be used to implement the front end of SONET equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip includes parallel-to-serial conversion and system timing. The system timing circuitry consists of a high-speed phase detector, clock dividers, and clock distribution throughout the front end.

The sequence of operations is as follows:

Transmitter Operations:

1. 8-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Internal clocking and control functions are transparent to the user. Details of data timing can be seen in Figures 7 through 10.

Suggested Interface Devices

AMCC	S3040	OC-48 Clock Recovery Device
AMCC	S3045	OC-48 to OC-12 Demux
AMCC	S3042	OC-48 Demux

Figure 2. S3041 Functional Block Diagram
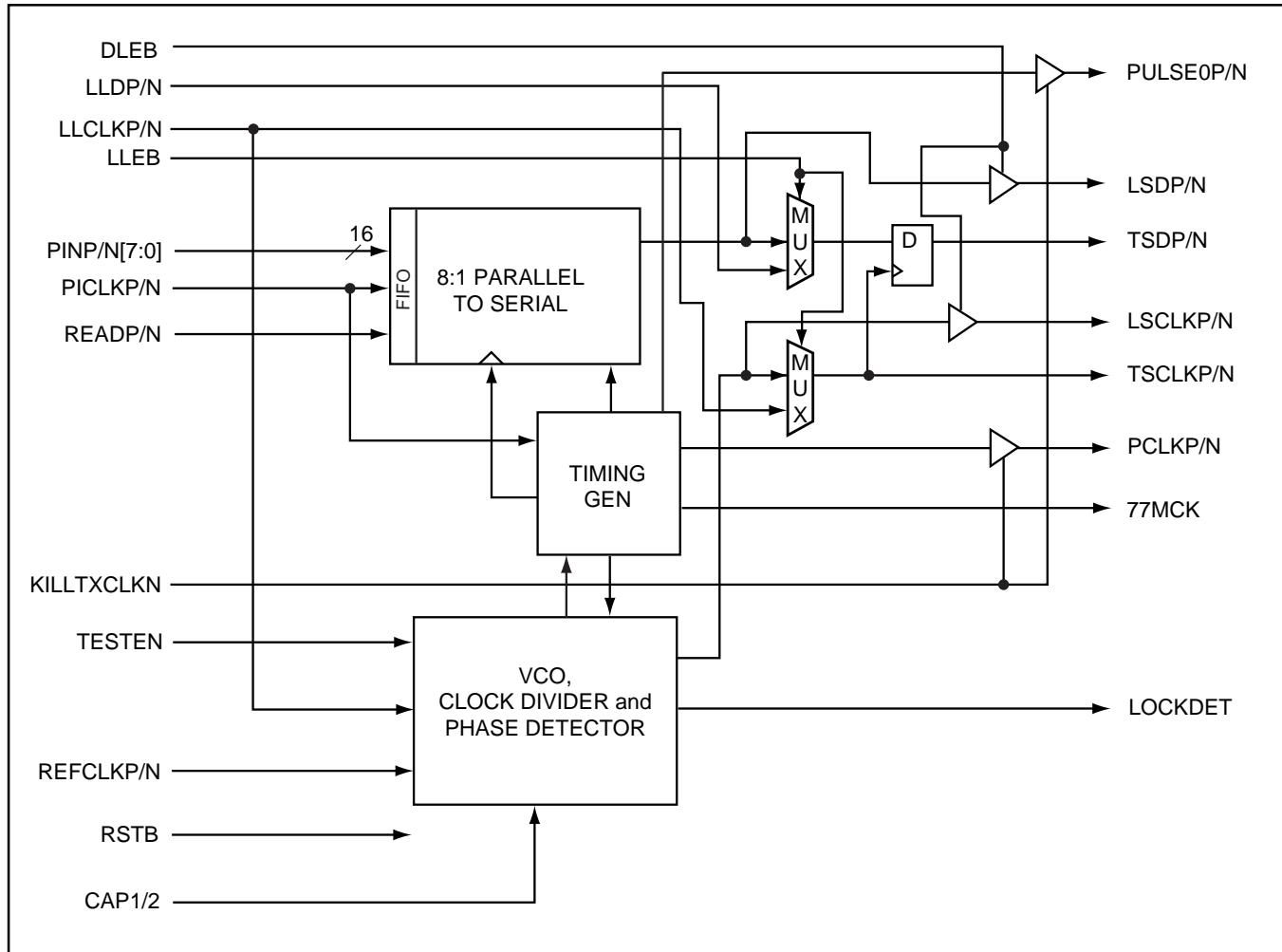
SONET OVERVIEW

Synchronous Optical Network (SONET) is a standard for connecting one fiber system to another at the optical level. SONET, together with the Synchronous Digital Hierarchy (SDH) administered by the ITU-T, forms a single international standard for fiber interconnect between telephone networks of different countries. SONET is capable of accommodating a variety of transmission rates and applications.

The SONET standard is a layered protocol with four separate layers defined. These are:

- Photonic
- Section
- Line
- Path

Figure 3 shows the layers and their functions. Each of the layers has overhead bandwidth dedicated to administration and maintenance. The photonic layer simply handles the conversion from electrical to optical and back with no overhead. It is responsible for transmitting the electrical signals in optical form over the physical media. The section layer handles the transport of the framed electrical signals across the optical cable from one end to the next. Key functions of this layer are framing, scrambling, and error monitoring. The line layer is responsible for the reliable transmission of the path layer information stream carrying voice, data, and video signals. Its main functions are synchronization, multiplexing, and reliable transport. The path layer is responsible for the actual transport of services at the appropriate signaling rates.

Figure 4 shows a standard OC-48 Frame former structure.

Data Rates and Signal Hierarchy

Table 1 contains the data rates and signal designations of the SONET hierarchy. The lowest level is the basic SONET signal referred to as the synchronous transport signal level-1 (STS-1). An STS-N signal is made up of N byte-interleaved STS-1 signals. The optical counterpart of each STS-N signal is an optical carrier level-N signal (OC-N). The S3041 chip supports OC-48 rate (2.488 Gbps).

Figure 3. SONET Structure
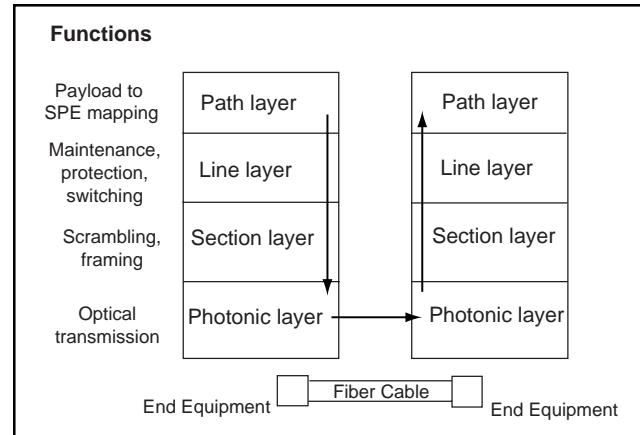
Table 1. SONET Signal Hierarchy

Elec.	CCITT	Optical	Data Rate (Mbps)
STS-1		OC-1	51.84
STS-3	STM-1	OC-3	155.52
STS-12	STM-4	OC-12	622.08
STS-24	STM-8	OC-24	1244.16
STS-48	STM-16	OC-48	2488.32

Figure 4. STS–48/OC–48 Frame Format
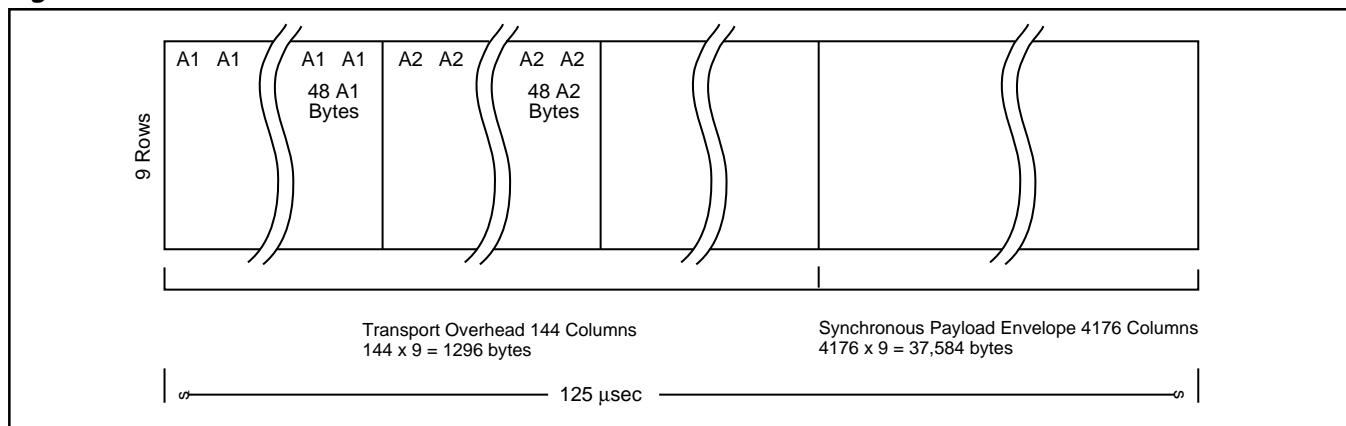
S3041 ARCHITECTURE/FUNCTIONAL DESIGN

Mux Operation

The S3041 performs the serializing stage in the processing of a transmit SONET STS-48 bit serial data stream. It converts the byte serial 311 Mbyte/sec data stream to bit serial format at 2.488 Gbps. Diagnostic loopback is provided (transmitter to receiver), and Line Loopback is also provided (receiver to transmitter).

A high-frequency bit clock is generated from a 155.52 MHz frequency reference by using a frequency synthesizer consisting of an on-chip phase-locked loop circuit with a divider.

Clock Divider and Phase Detector

The Clock Divider and Phase Detector, shown in the block diagram in Figure 2, contains monolithic PLL components.

The REFCLK input must be generated from a differential LVPECL crystal oscillator which has a frequency accuracy of better than 20 ppm in order for the VCOCLK frequency to have the same accuracy required for operation in a SONET system.

In order to meet the .01 UI SONET jitter specifications, the maximum reference clock jitter must be guaranteed over the 12 KHz to 20 MHz bandwidth. For details of reference clock jitter requirements, see Table 2.

Table 2. Reference Jitter Limits

Maximum Reference Clock Jitter in 12 kHz to 20 MHz Band	Operating Mode
1 ps rms	STS-48

Timing Generator

The Timing Generator function, seen in Figure 2, provides two separate functions. It provides a byte rate version of the TSCLK, and a mechanism for aligning the phase between the incoming byte clock and the clock which loads the parallel-to-serial shift register.

The PCLK output is a byte rate version of TSCLK. For STS-48, the PCLK frequency is 311 MHz. PCLK is intended for use as a byte speed clock for upstream multiplexing and overhead processing circuits. Using PCLK for upstream circuits will ensure a stable frequency and phase relationship between the data coming into and leaving the S3041 device.

In the parallel-to-serial conversion process, the incoming data is passed from the PICLK byte clock timing domain to the internally generated byte clock timing domain, which is phase aligned to TSCLK.

The Timing Generator also produces a feedback reference clock to the Phase Detector. A counter divides the synthesized clock down to the same frequency as the reference clock REFCLK.

Parallel-to-Serial Converter

The FIFO is used to accomodate phase differences between the internal byte clock and the external PICLK. The READ and PULSE signals are used to control the FIFO to prevent overflow/underflow conditions.

The Parallel-to-Serial converter shown in Figure 2 is comprised of a FIFO and a parallel-to-serial register. The FIFO latches the data from the PIN[7:0] bus on the rising edge of PICLK. The parallel-to-serial register is a parallel loadable shift register which takes its parallel input from the FIFO.

An internally generated byte clock, which is phase aligned to the transmit serial clock as described in the Timing Generator description, activates the parallel data transfer between registers. The serial data is shifted out of the second register at the TSCLK rate.

Table 3. Input Pin Assignment and Description

Pin Name	Level	I/O	Pin #	Description
PINP7 PINN7 PINP6 PINN6 PINP5 PINN5 PINP4 PINN4 PINP3 PINN3 PINP2 PINN2 PINP1 PINN1 PINP0 PINN0	LVDS	I	29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44	Parallel Data Input. A 311 Mbyte/sec word, aligned to the PICLK parallel input clock. PIN<7> is the most significant bit (corresponding to bit 1 of each PCM word, the first bit transmitted). PIN<0> is the least significant bit (corresponding to bit 8 of each PCM word, the last bit transmitted). PIN<7:0> is sampled on the rising edge of PICLK.
PICLKP PICLKN	LVDS	I	47 48	Parallel Input Clock. A 311 MHz nominally 50% duty cycle input clock, to which PIN<7:0> is aligned. PICLK is used to transfer the data on the PIN inputs into a holding register in the parallel-to-serial converter. The rising edge of PICLK samples PIN<7:0>.
LLDP LLDN	Externally Biased Diff. LVPECL	I	58 57	Line Loopback Data. Inputs normally provided from a companion S3042 device. Used to implement a line loopback function in which the receive serial data and clock signals are regenerated and passed through the S3041 transmitter.
LLCLKP LLCLKN	Externally Biased Diff. LVPECL	I	62 61	Line Loopback Clock. Inputs normally provided from a companion S3042 device. Used to implement a line loopback function in which the receive serial data and clock signals are regenerated and passed through the S3041 transmitter.
REFCLKP REFCLKN	Internally Biased Diff. LVPECL	I	80 81	Reference Clock. 155.52 MHz. The clock generator circuit will lock to this reference clock by comparing the REFCLK with an internally divided down clock.
DLEB	LVTTL	I	65	Diagnostic Loopback Enable. Active Low. When active, selects diagnostic loopback. The primary data (TSD) and clock (TSCLK) are always active. When active, the diagnostic loopback clock, (LSCLK), and data (LSD) outputs are active.
RSTB	LVTTL	I	64	Master Reset. Reset input for the device, active low. During reset, PCLK does not toggle.
LLEB	LVTTL	I	68	Line Loopback Enable. Active Low. Selects Line Loopback when active. When LLEB is active, the S3041 will route the data from the LLD/LLCLK inputs to the TSD/TSCLK outputs. Inactive for normal operation.

Table 3. Input Pin Assignment and Description (Con't.)

Pin Name	Level	I/O	Pin #	Description
READP READN	LVDS	I	20 21	Elastic Store Write Differential Input. This input pin is clocked in using the rising edge of PICLK clock. This input is used to align the elastic store. The S3041 mux will monitor the READ input for a fault condition. If there is no activity or stuck high more than one pulse every twelfth 311 MHz clock cycle, a fault condition will be declared. The PULSE0 signal will output two 311 MHz pulse width instead of one every sixth 311 MHz clock cycle.
KILLTXCLKN	LVTTL	I	69	Kill Transmit Clock Input. In normal operation, the KILLTXCLKN should be set High. When this input is Low, it will force the PCLK and PULSE0 outputs Low.
TESTEN	LVTTL	I	60	Test Clock Enable.When this input is High, it will select the LLCLK input instead of the internally generated 2.488 GHz clock as the system clock. When this input is Low, it will select the internally generated 2.488 GHz clock. For normal operation, set low.
CAP1 CAP2	Analog	I	94 93	External loop filter capacitor pins. The loop filter capacitor and resistors are connected to these pins. (See Figure 18).

Table 4. Output Pin Assignment and Description

Pin Name	Level	I/O	Pin #	Description
TSCLKP TSCLKN	Diff. CML	O	7 8	Transmit Clock output. Transmit serial clock that can be used to retime the TSD signal. An optical transmitter can use the rising edge of TSCLK to retime the TSD data.
TSDP TSDN	Diff. CML	O	11 12	Transmit Serial Data. Serial data stream signals, normally connected to an optical transmitter module.
PCLKP PCLKN	LVDS	O	45 46	Parallel Clock. A reference clock generated by dividing the internal bit clock by eight. It is normally used to coordinate byte-wide transfers between upstream logic and the S3041 device.
LSDP LSDN	Low Swing Diff. CML	O	67 66	Loopback Serial Data. Serial data stream signals normally connected to a companion S3042 device for diagnostic loopback purposes. The LSD outputs are updated on the rising edge of the LSCLK.
LSCLKP LSCLKN	Low Swing Diff. CML	O	75 74	Loopback Serial Clock. Serial clock signals normally connected to a companion S3042 device for diagnostic loopback purposes. The LSD outputs are updated on the rising edge of the LSCLK.
77MCK	LVTTL	O	51	77 MHz Clock Output. 77 MHz clock output from the clock synthesizer.
PULSE0P PULSE0N	LVDS	O	22 23	Elastic Store Read Differential Outputs. This output pulse is sychronized with the falling edge of PCLKP/N. This signal is used to align the elastic store. The PULSE0 output should be active for only one pulse every twelfth 311 MHz clock cycle during the normal (no fault) operation. If the S3041 mux detects no activity or stuck high more than one pulse every twelfth 311 MHz on the READ input, a fault condition will be declared. The S3041 mux will output a two 311 MHz pulse width instead of one every sixth 311 MHz clock cycle.
LOCKDET	LVTTL	O	19	Lock Detect. Goes Low after the PLL has locked to the clock provided on the REFCLK pins. LOCKDET is an asynchronous output.

Table 5. Common Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
COREGND	GND		1, 2, 15, 83, 96, 98, 99	Core Ground
COREVCC	+3.3V		3, 4, 16, 90, 97, 100	Core VCC
CMLVCC	+3.3V		5, 14, 72, 73, 76, 77	CML VCC
CMLGND	GND		6, 13, 63, 70, 71, 78, 79,	CML Ground
TTLVCC	+3.3V		18	TTL VCC
TTLGND	GND		52 53	TTL Ground
LVDSGND	GND		24 25	LVDS Ground
LVDSVCC	+3.3V		27 28	LVDS VCC
PECLVCC	+3.3V		55 56	PECL VCC
PECLGND	GND		54	PECL Ground
AVCC	+3.3V		84, 88, 91	Analog VCC
AGND	GND		85, 89, 92	Analog Ground
NC			9, 10, 17, 26, 49, 50, 59, 82, 86, 87, 95	Not Connected

Figure 5. S3041 Pinout

Top pins (left to right, 100–76):
COREVCC (100), COREGND (99), COREGND (98), COREVCC (97), COREGND (96), NC (95), CAP1 (94), CAP2 (93), AGND (92), AVCC (91), COREVCC (90), AGND (89), AVCC (88), NC (87), NC (86), AGND (85), AVCC (84), COREGND (83), NC (82), REFCLKN (81), REFCLKP (80), CMLGND (79), CMLGND (78), CMLVCC (77), CMLVCC (76)

Left pins (top to bottom, 1–25):
Pin	Signal
1	COREGND
2	COREGND
3	COREVCC
4	COREVCC
5	CMLVCC
6	CMLGND
7	TSCLKP
8	TSCLKN
9	NC
10	NC
11	TSDP
12	TSDN
13	CMLGND
14	CMLVCC
15	COREGND
16	COREVCC
17	NC
18	TTLVCC
19	LOCKDET
20	READP
21	READN
22	PULSE0P
23	PULSE0N
24	LVDSGND
25	LVDSGND

Center: S3041 Pinout Top View — 100 TQFP/TEP

Right pins (top to bottom, 75–51):
Pin	Signal
75	LSCLKP
74	LSCLKN
73	CMLVCC
72	CMLVCC
71	CMLGND
70	CMLGND
69	KILLTXCLKN
68	LLEB
67	LSDP
66	LSDN
65	DLEB
64	RSTB
63	CMLGND
62	LLCLKP
61	LLCLKN
60	TESTEN
59	NC
58	LLDP
57	LLDN
56	PECLVCC
55	PECLVCC
54	PECLGND
53	TTLGND
52	TTLGND
51	77MCK

Bottom pins (left to right, 26–50):
NC (26), LVDSVCC (27), LVDSVCC (28), PINP7 (29), PINN7 (30), PINP6 (31), PINN6 (32), PINP5 (33), PINN5 (34), PINP4 (35), PINN4 (36), PINP3 (37), PINN3 (38), PINP2 (39), PINN2 (40), PINP1 (41), PINN1 (42), PINP0 (43), PINN0 (44), PCLKP (45), PCLKN (46), PICLKP (47), PICLKN (48), NC (49), NC (50)

Figure 6. 100 TQFP/TEP Package

DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	b	e
MIN		0.05	1.35	15.80	13.95	15.80	13.95	0.50	0.17	0.50 BSC.
NOM			1.40	16.00	14.00	16.00	14.00	0.60	0.22	
MAX	1.60	0.15	1.45	16.20	14.05	16.20	14.05	0.75	0.27	

Thermal Management

Device	Max Power	Θja	Comments
S3041	1.6 W	26˚C/W	Required air flow of 100 LFPM or with DW0045-28 heatsink.
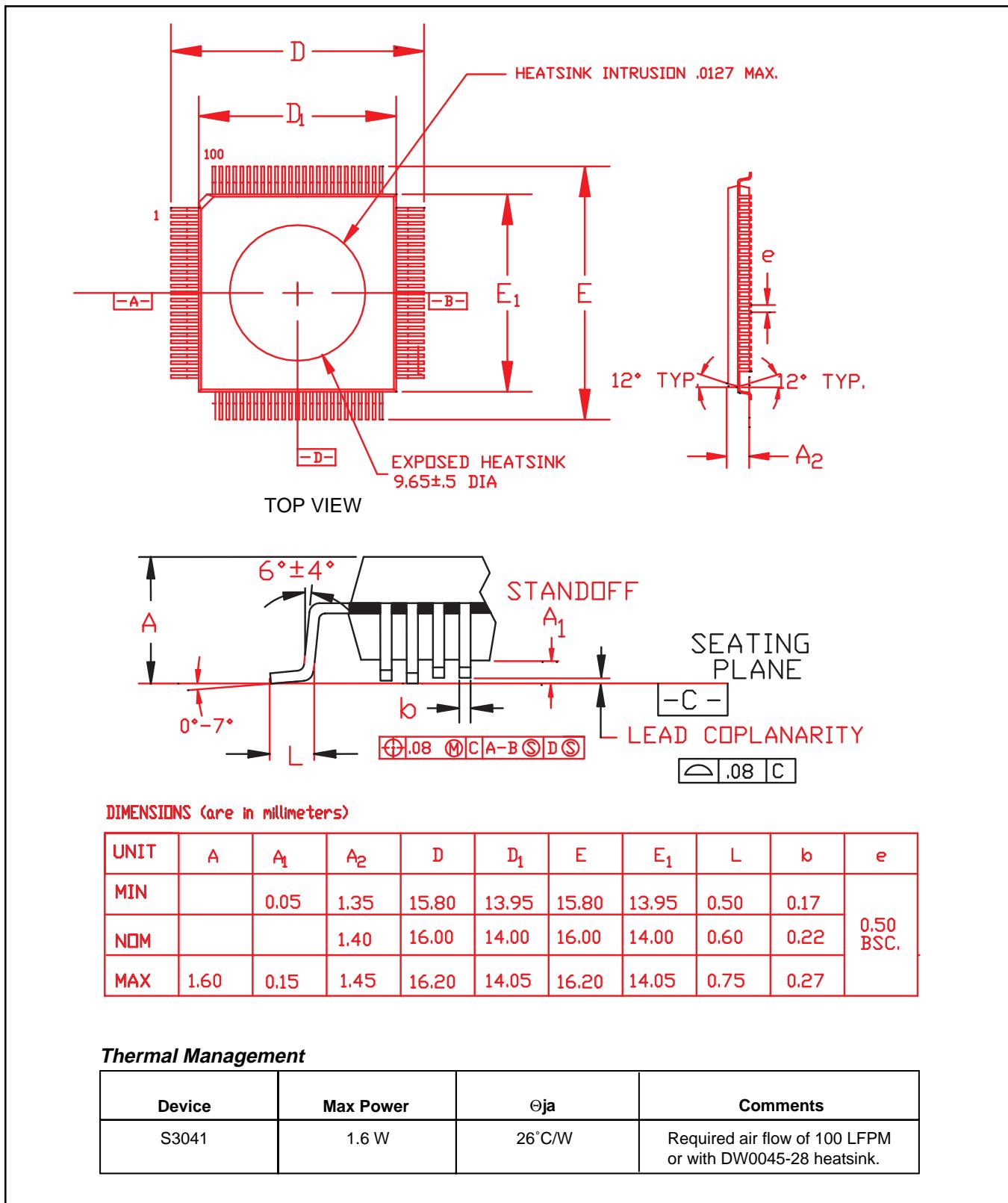
OTHER OPERATING MODES

Diagnostic Loopback

When the Diagnostic Loopback Enable (DLEB) input is active, the differential serial clock and data outputs are enabled. A loopback from the transmitter to the receiver at the serial data rate can be set up for diagnostic purposes.

Line Loopback

The Line Loopback circuitry consists of alternate clock and data inputs. For the S3041, it selects the source of the data and clock which is output on TSD and TSCLK. When the Line Loopback Enable input (LLEB) is high, it selects data and clock from the Parallel to Serial Converter block. When LLEB is low, it forces the output data multiplexer to select data and clock from the LLD and LLCLK inputs, and a receive-to-transmit loopback can be established at the serial data rate. Both Diagnostic and Line Loopback can be active at the same time.

Table 6. Performance Specifications

Parameter	Min	Typ	Max	Units	Condition
Nominal VCO Center Frequency		2.488 ±12%		MHz	
Reference Clock Frequency Tolerance	-20		+20	ppm	Required to meet SONET output frequency specification.
Reference Clock Input Duty Cycle	45		55	%	
Reference Clock Rise & Fall Times			1.5	ns	20% to 80% of amplitude.

Table 7. Output Jitter Generation vs. Ambient Temperature with Heatsink (DW0045-28) and 100 LFPM

	Temperature	Jitter Generation			Unit
Voltage		3.1	3.3	3.47	V
	−40˚ C	0.006	0.006	0.006	UI
	25˚ C	0.007	0.006	0.006	UI
	70˚ C	0.007	0.007	0.007	UI
	85˚ C	0.007	0.007	0.007	UI

Table 8. Output Jitter Generation vs. Ambient Temperature in Still Air

	Temperature	Jitter Generation			Unit
Voltage		3.1	3.3	3.47	V
	−40˚ C	0.006	0.006	0.006	UI
	25˚ C	0.007	0.007	0.007	UI
	70˚ C	0.008	0.007	0.007	UI
	85˚ C	0.008	0.008	0.008	UI

Note: Data were taken with 100 sweeps on HP test equipment.

Table 9. LVTTL Input/Output DC Characteristics

Symbol	Description	Min	Typ	Max	Unit	Conditions
V_{IH}	Input High Voltage	2.0		TTL V_{CC}	V	TTL V_{CC} = Max
V_{IL}	Input Low Voltage	0.0		0.8	V	TTL V_{CC} = Max
I_{IH}	Input High Current			50	µA	V_{IN} = 2.4 V
I_{IL}	Input Low Current	-500			µA	V_{IN} = 0.5 V
V_{OH}	Output High Voltage	2.2			V	V_{IH} = Min. V_{IL} = Max. I_{OH} = -100 µA
V_{OL}	Output Low Voltage			0.5	V	V_{IH} = Min. V_{IL} = Max. I_{OL} = 4 mA

Note: All parameters are specified with respect to the source termination and ground with V_{TTL} = Max. = 3.465V.

Table 10. LVDS Input/Output DC Characteristics[1]

Symbol	Description	Min	Typ	Max	Unit	Conditions
V_{IH}	Input High Voltage	1.1		1.7	V	$V_{LVDSVCC}$ = Max
V_{IL}	Input Low Voltage	.9		1.5	V	$V_{LVDSVCC}$ = Max
V_{INDIFF}[2]	Input Voltage Differential	200		900	mV	$V_{LVDSVCC}$ = Max
$V_{INSINGLE}$	Input Single-ended Voltage	100		450	mV	$V_{LVDSVCC}$ = Max
R_{DIFF}	Differential Input Resistance	80	100	120	Ω	$V_{LVDSVCC}$ = Max
I_{IH}	Input High Current			+10	µA	V_{IN} = Max
I_{IL}	Input Low Current	-10			µA	$V_{IN =} V_{LVDSVCC}$
V_{KH}	High I/O Clamp Voltage	0.15		1.5	V	I_I = Io = +100µA $V_{LVDSVCC}$ = 0V
V_{KL}	Low I/O Clamp Voltage	-0.15		-1.5	V	I_I = Io = -100µA $V_{LVDSVCC}$ = 0V
V_{OH}	Output High Voltage	1.00		1.80	V	V_{IH} = Min V_{IL} = Max
V_{OL}	Output Low Voltage	.700		1.40	V	V_{IH} = Min V_{IL} = Max
$V_{OUTDIFF}$[2]	Output Differential Voltage	460	740	900	mV	V_{IH} = Max V_{IL} = Min
$V_{OUTSINGLE}$	Output Single-ended Voltage	230	370	450	mV	V_{IH} = Max V_{IL} = Min

Note: Output loading is 220Ω to GND and 100Ω line-to-line.
1. All parameters are specified with respect to the source termination and ground with V_{TTL} = Max. = 3.465V.
2. See Figure 11.

Table 11. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	-40		85	˚C
Junction Temperature Under Bias			+130	˚C
Voltage on V_{CC} with Respect to GND	3.13	3.3	3.47	V
Voltage on any LVPECL Input Pin	V_{CC} -2		V_{CC}	V
ICC		390	455	mA

Table 12. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Storage Temperature	-65		150	˚C
Voltage on V_{CC} with Respect to GND	-0.5		+4.0	V
Voltage on any LVPECL Input Pin	0		V_{CC}	V
High Speed LVPECL Output Source Current			50	mA

ESD Ratings

The S3041 is rated to the following ESD voltages based on the human body model:

1. All pins are rated at or above 500 V except pin 57, pin 58, pin 61, pin 62, pin 92, and pin 94.

Table 13. Differential CML Output DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Condition
V_{OL}	CML Output LOW Voltage	V_{CC} -0.95		V_{CC} -0.55	V	100Ω line-to-line.
V_{OH}	CML Output HIGH Voltage	V_{CC} -0.35		V_{CC} -0.10	V	100Ω line-to-line.
$\Delta V_{OUTDIFF}$	CML Serial Output Differential Voltage Swing	560		1300	mV	100Ω line-to-line. See Figure 11.
$\Delta V_{OUTSINGLE}$	CML Serial Output Single-ended Voltage Swing	280		650	mV	100Ω line-to-line. See Figure 11.

Table 14. Low Swing Differential CML Output DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OL}	Low Swing CML Output LOW Voltage	V_{CC} -0.50		V_{CC} -0.25	V	100Ω line-to-line.
V_{OH}	Low Swing CML Output HIGH Voltage	V_{CC} -0.20		V_{CC} -0.05	V	100Ω line-to-line.
$\Delta V_{OUTDIFF}$	Low Swing CML Serial Output Differential Voltage Swing	360		800	mV	100Ω line-to-line. See Figure 11.
$\Delta V_{OUTSINGLE}$	Low Swing CML Serial Output Single-ended Voltage Swing	180		400	mV	100Ω line-to-line. See Figure 11.

Table 15. Internally Biased Differential LVPECL Input DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
ΔV_{INDIFF}	Differential Input Voltage Swing	300		1200	mV	See Figure 11.
$\Delta V_{INSINGLE}$	Single-ended Input Voltage Swing	150		600	mV	See Figure 11.
R_{DIFF}	Differential Input Resistance	80	100	120	Ω	

Table 16. Externally Biased Differential LVPECL Input DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{BIAS}	LVPECL DC Bias Voltage	V_{CC} -1.2		V_{CC} -0.8	V	Inputs open.
V_{IL}	LVPECL Input LOW Voltage	V_{CC} -2.000		V_{CC} -0.25	V	
V_{IH}	LVPECL Input HIGH Voltage	V_{CC} -1.20		V_{CC} -0.05	V	
ΔV_{INDIFF}	Differential Input Voltage Swing	300		1200	mV	See Figure 11.
$\Delta V_{INSINGLE}$	Single-ended Input Voltage Swing	150		600	mV	See Figure 11.
R_{DIFF}	Differential Input Resistance	80	100	120	Ω	

Figure 7. Line Loopback Input Timing Diagram
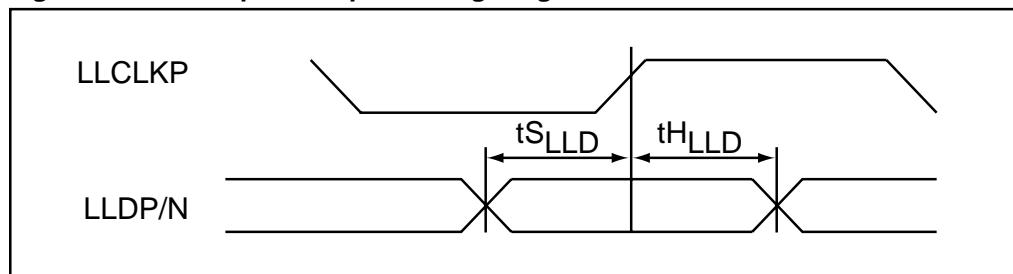

Notes on High-Speed LVPECL Input Timing:

1.   Timing is measured from the cross-over point of the reference signal to the cross-over point of the input.

Table 17. AC Transmitter Timing Characteristics

Symbol	Description	Min	Max	Units
	TSCLK/LSCLK Frequency (nom. 2.488 GHz)		2.6	GHz
	TSCLK/LSCLK Duty Cycle	40	60	%
	PICLK Duty Cycle	33	67	%
tS_{PIN}	READP/N PIN [7.0] Set-up Time w.r.t. PICLK	0.5		ns
tH_{PIN}	READP/N PIN [7.0] Hold Time w.r.t. PICLK	0.5		ns
tP_{TSD}	TSCLK/LSCLK Low to TSD/LSD Valid Propagation Delay	−100	+ 100	ps
tS_{TSD}	TSD/LSD Set-up Time w.r.t. TSCLK/LSCLK	125		ps
tH_{TSD}	TSD/LSD Hold Time w.r.t. TSCLK/LSCLK	100		ps
tS_{LLD}	LLDP/N Set-up Time w.r.t. LLCLKP/N	100		ps
tH_{LLD}	LLDP/N Hold Time w.r.t. LLCLKP/N	100		ps
	77MCK Duty Cycle	40	60	%
	77MCK Output rise and fall times (10pf load)		2.1	ns
	LVDS Output rise and fall times (20-80% 275Ω to GND and 100Ω line-to-line)		800	ps
	CML Output rise and fall times (20-80% 100Ω line-to-line)		150	ps
	Low Swing CML Output rise and fall times (20-80% 100Ω line-to-line)		150	ps
tP_{PICLK}	PICLK Delay from PCLK	0	13	ns
tP_{PRCLK}	Read Delay from Pulse	0	13	ns
tS_{PULSE}	PULSE0 Set-up Time w.r.t. PCLK	1		ns
tH_{PULSE}	PULSE0 Hold Time w.r.t. PCLK	1		ns

Figure 8.
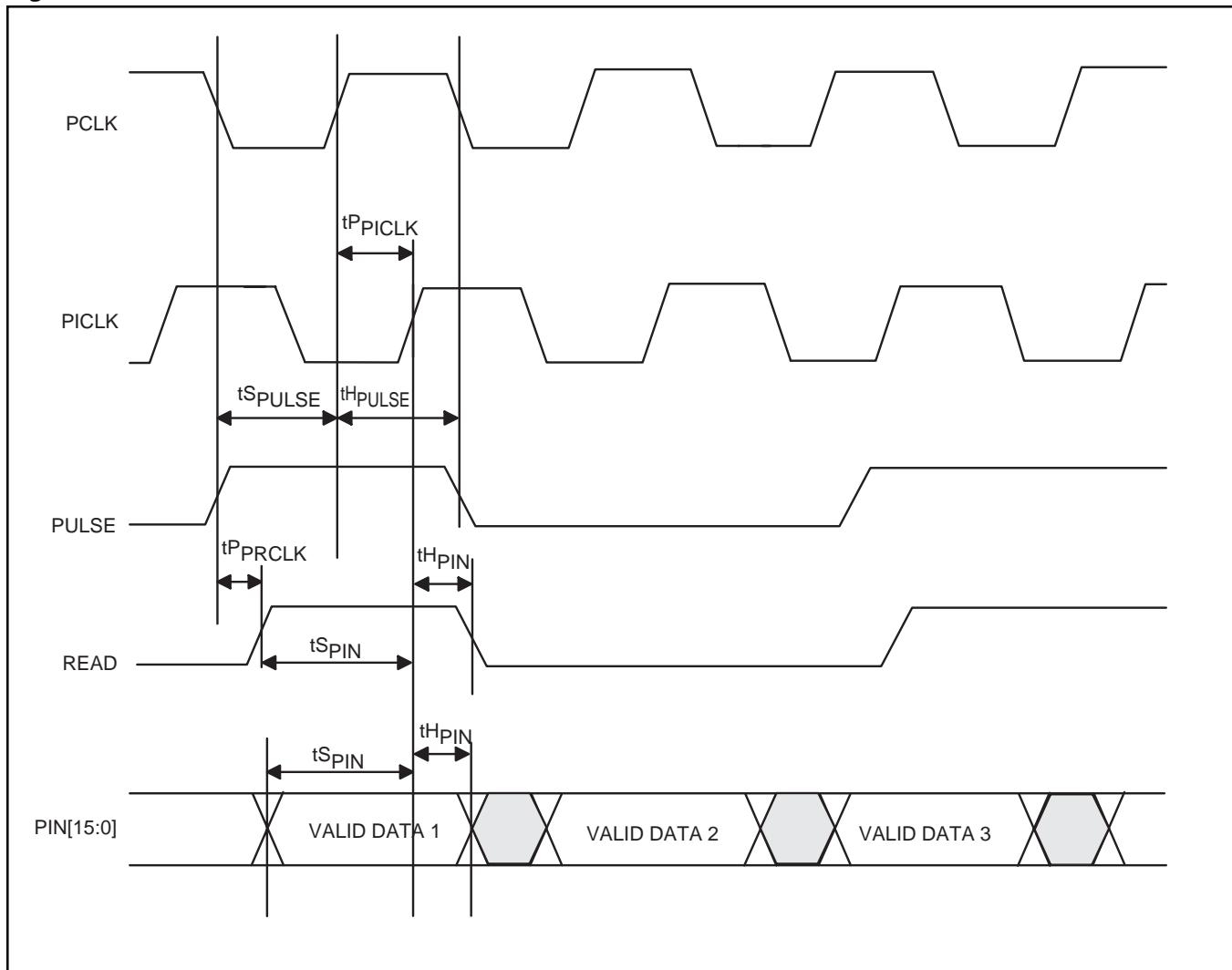
Figure 9. Pin AC Input Timing
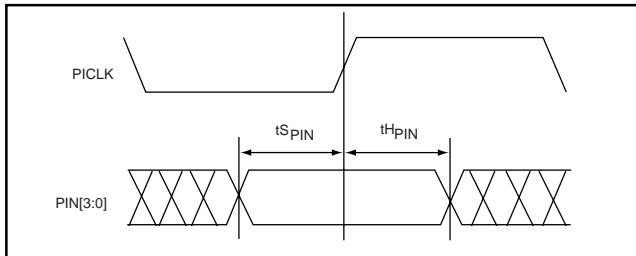
1. When a set-up time is specified on LVDS signals between an input and a clock, the set-up time is the time in picoseconds from the cross-over point of the input to the cross-over point of the clock.
2. When a hold time is specified on LVDS signals between an input and a clock, the hold time is the time in picoseconds from the cross-over point of the clock to the cross-over point of the input.

Figure 10. Output Timing
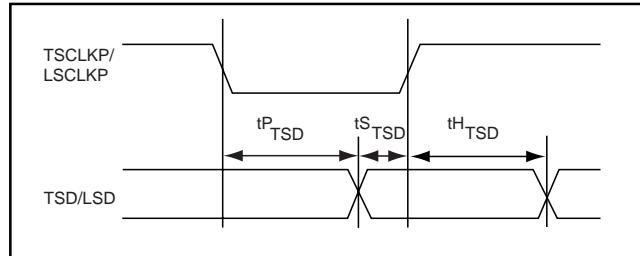
Notes on High-Speed CML Output Timing
1. Output propagation delay time is the time in nanoseconds from the cross-over point of the reference signal to the cross-over point of the output.

Figure 11. Differential Voltage Measurement
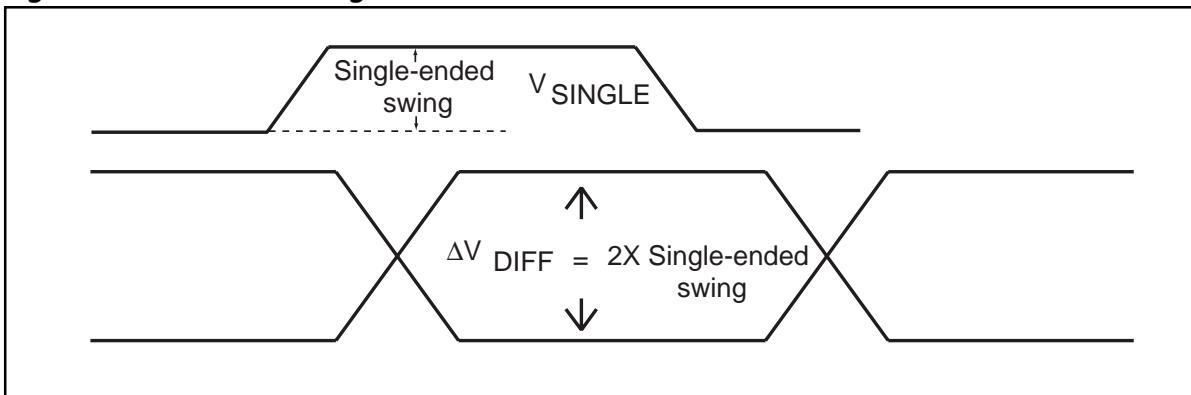
Figure 12. S3045 LVDS Driver to S3041 LVDS Input Direct Coupled Termination
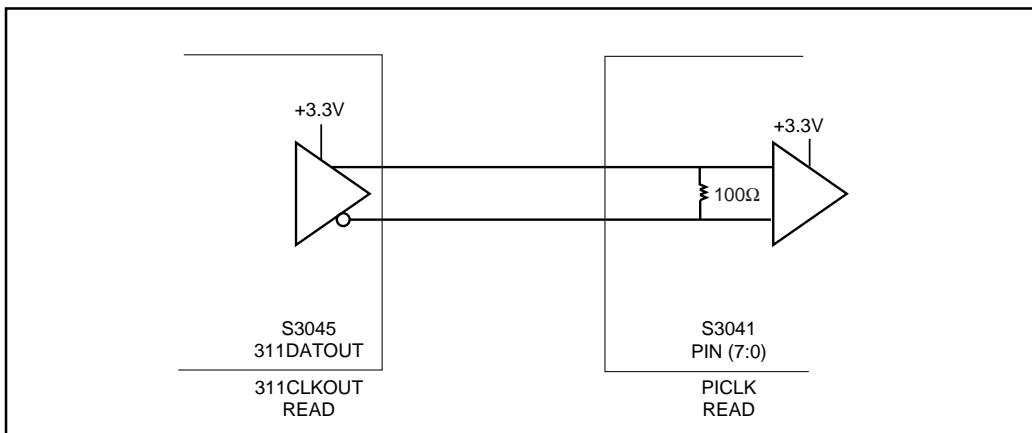
Figure 13. S3041 CML Output to +5V PECL Input AC Coupled Termination
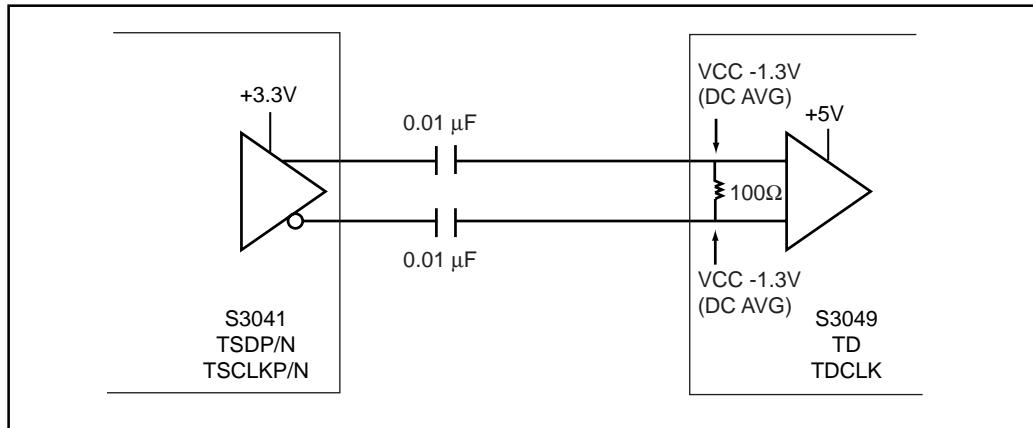
Figure 14. S3041 to S3042 for Diagnostic Loopback
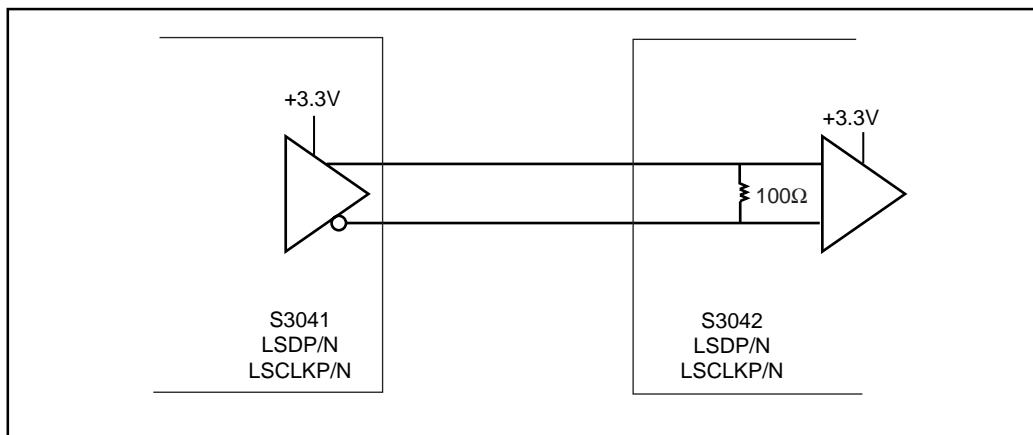
Figure 15. Single-Ended LVPECL Driver to S3041 Input AC Coupled Termination
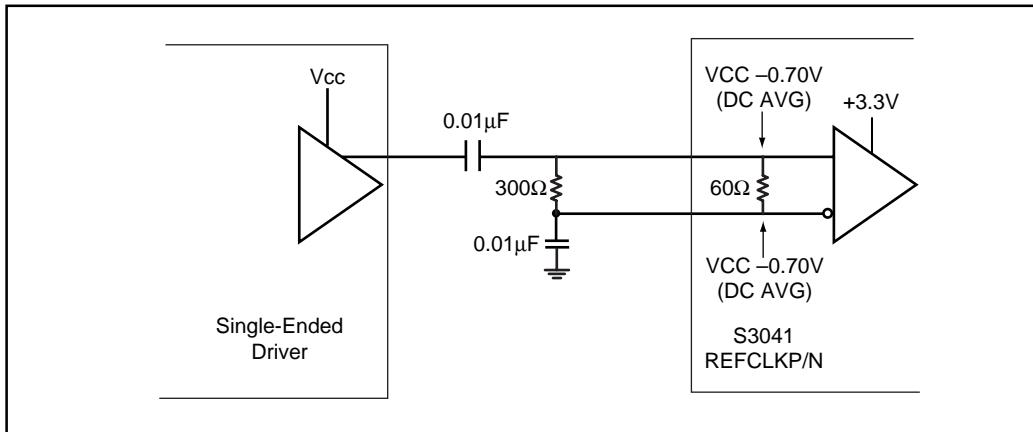
*Figure 16. +5V Differential PECL Driver to S3041 Input AC Coupled Termination*

+5V
0.01µF
330Ω
330Ω   0.01µF
VCC −0.70V (DC AVG)   +3.3V
100Ω
VCC −0.70V (DC AVG)
S3041 REFCLKP/N
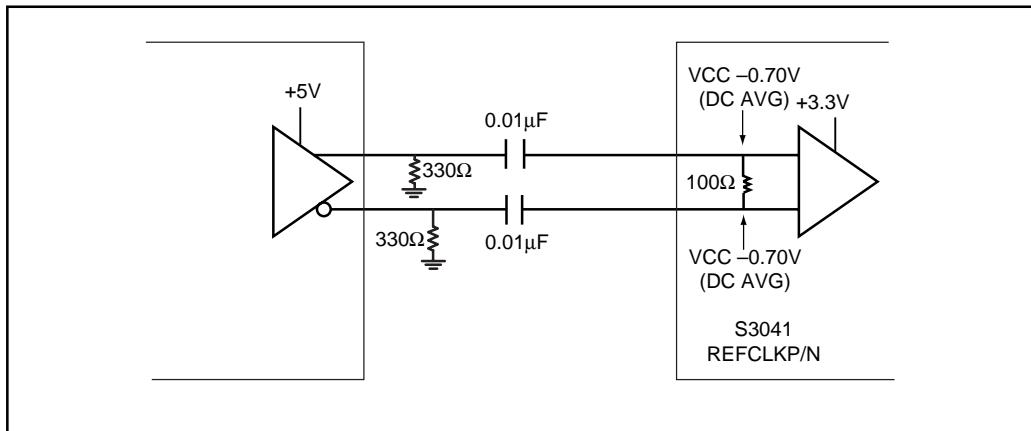
Figure 17. S3041 to S3045 Terminations

+3.3V
275Ω
275Ω
100Ω
+3.3V
S3041 PULSE PCLK
S3045 PULSE 311TCLK
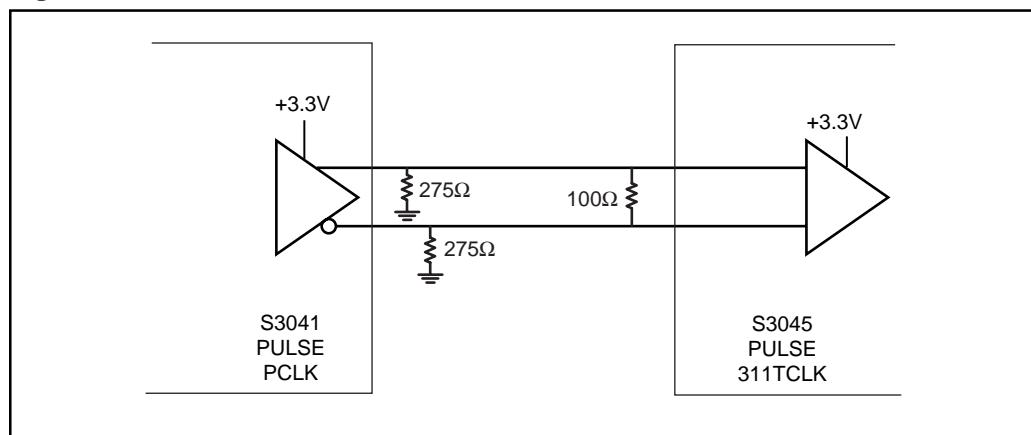
Figure 18. External Loop Filter Components

2.2 µF
62Ω   62Ω
CAP1   CAP2

AMCC

SONET/SDH/ATM OC-48 8:1 TRANSMITTER S3041
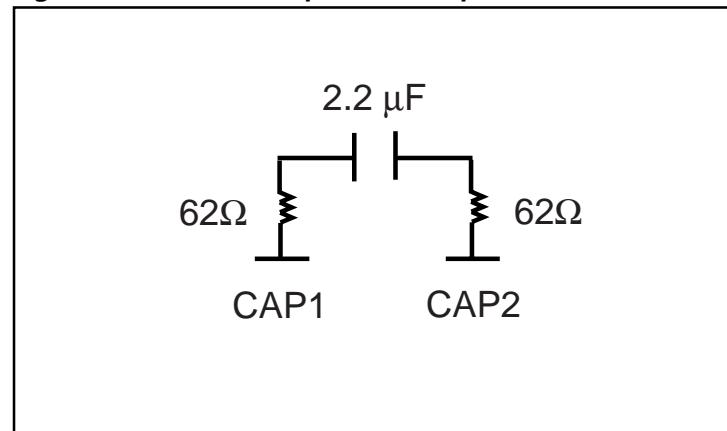
The S3041 utilizes a unique elastic store buffer which can be set in two different configurations allowing the system designer to be flexible in the way a system is to be layed out. The configuration of the elastic store buffer is dependent upon the I/O pins which comprise the Synch Timing loop. This loop is formed from PULSE(I/P) to READ(O/P) and PCLK(I/P) to PICLK(O/P). The elastic store buffer can be thought of as a memory stack with a read pointer. The PULSE signal is the read pointer which announces that it has read a register and when fed back to READ input, it synchronizes the write operation of the buffer so as not to simultaneously write over the same register that it has read previously.

Figure 19.
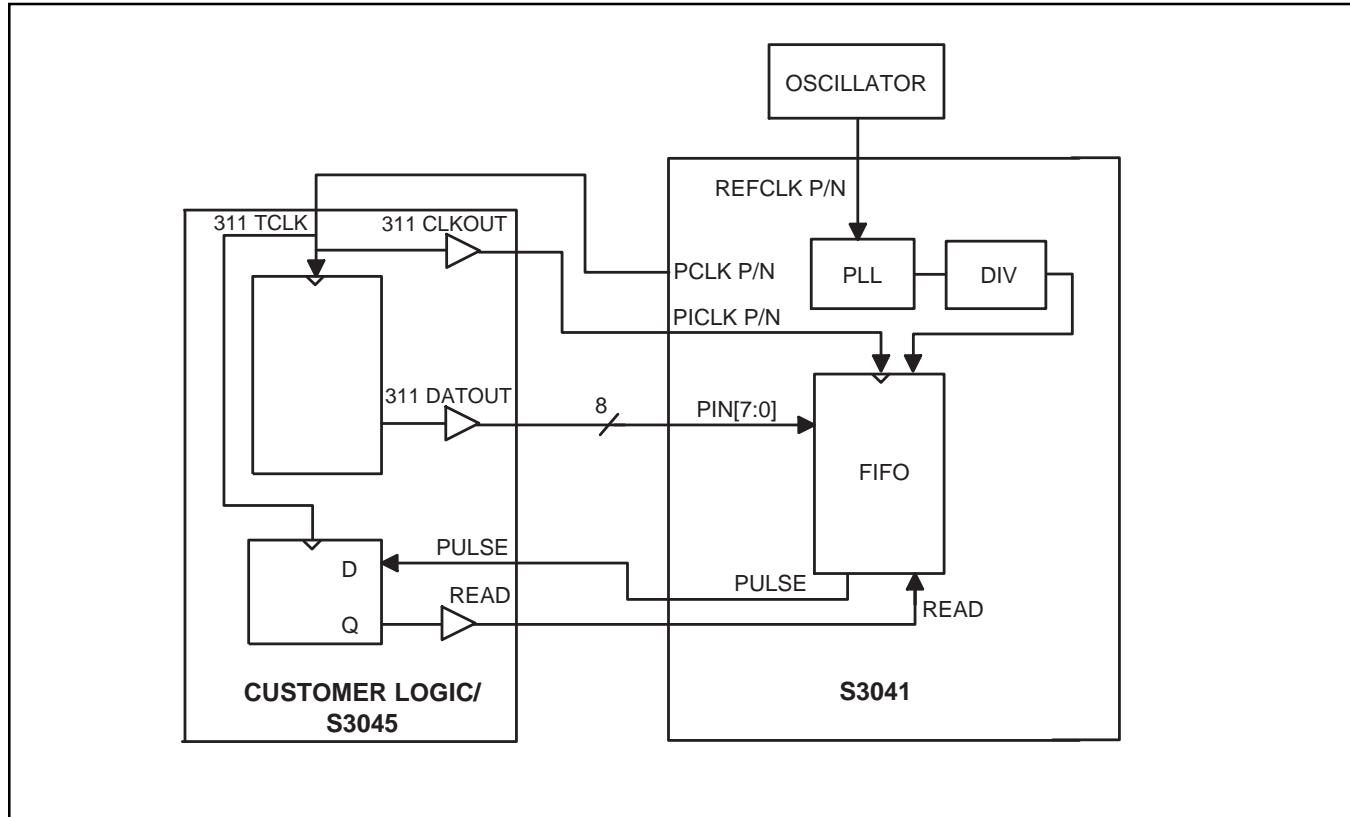
In the figure shown above, we are using the second configuration of the elastic store buffer. This configuration fully utilizes the elastic store buffer and allows the user a delay accommodation of 0 to 13ns. The PULSE delay must follow the PCLK delay. It is very important that the relationship between these two signals be kept all the way through the loop. Otherwise it is possible to under or over spill the buffer. It is important to insure that the PULSE signal is retimed along with the outgoing data to the S3041.

Figure 20. Typical Eye Opening for TSD
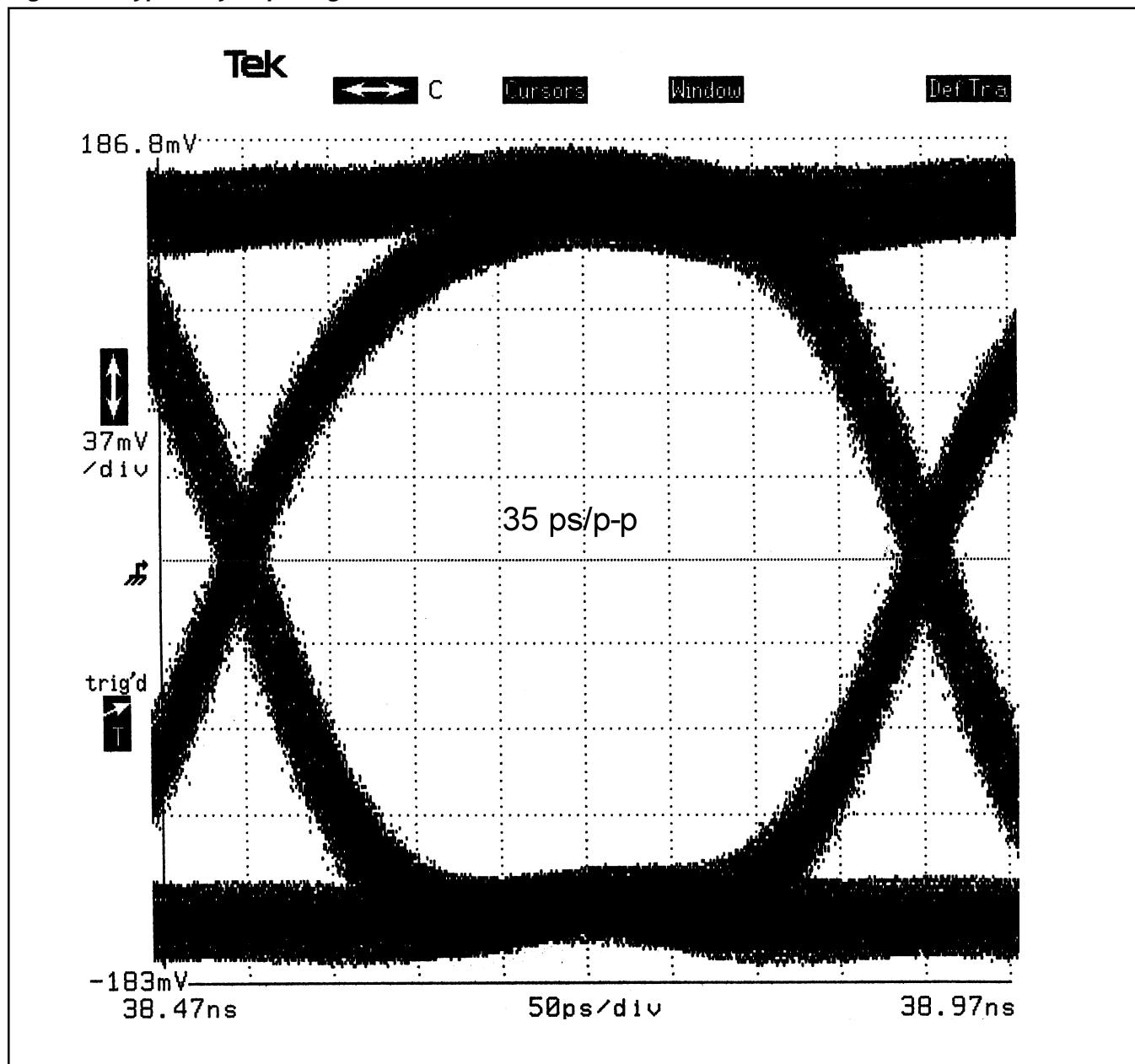
Ordering Information

PREFIX	DEVICE	PACKAGE	HEATSINK
S – Integrated Circuit	3041	TF – 100 TQFP/TEP	H2 – W/DW0045-28 Heatsink Unattached

<u>**X**</u>   <u>**XXXX**</u>   <u>**XX**</u>   <u>**XX**</u>

Prefix   Device   Package   Heatsink
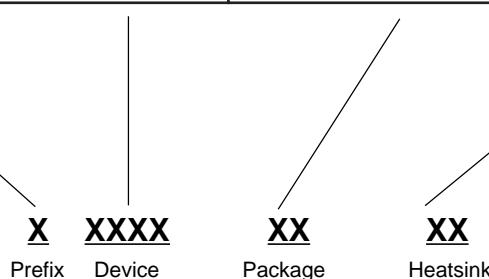
ISO 9001 CERTIFIED

Applied Micro Circuits Corporation • 6290 Sequence Dr., San Diego, CA 92121

Phone: (858) 450-9333 • (800) 755-2622 • Fax: (858) 450-9885

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