# GLM COMPLIANT SERIAL INTERFACE CIRCUITS S2044/S2045

## FEATURES

- Complies with the electrical and link levels of the Gigabaud Link Module (GLM) specification
- Functionally compliant with ANSI X3T11 Fibre Channel physical and transmission protocol standards
- S2044 transmitter incorporates phase-locked loop (PLL) providing clock synthesis from low-speed reference
- S2045 receiver PLL configured for clock and data recovery
- 1062 Mb/s (GLM), 531 Mb/s (HGLM) and 266 Mb/s (QGLM) operation
- 10- or 20-bit parallel TTL compatible interface
- 1 watt typical power dissipation for chipset
- +3.3/+5V power supply
- Low-jitter serial PECL compatible interface
- Lock detect
- Local loopback
- Compact 52 PQFP package
- Fibre Channel framing performed by receiver
- Continuous downstream clocking from receiver
- TTL compatible outputs possible with +5V I/O power supply

## APPLICATIONS

High-speed data communications

- Mainframe/Workstation
- Switched networks
- Proprietary extended backplanes
- Mass storage devices/RAID drives

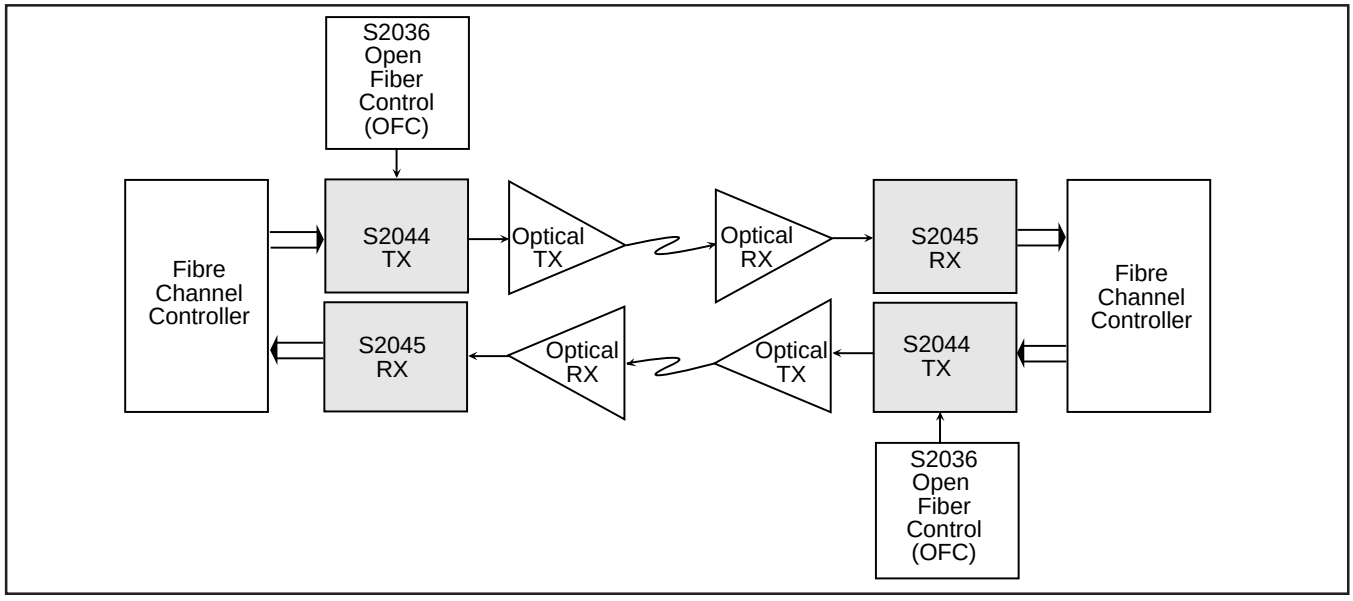
## GENERAL DESCRIPTION

The S2044 and S2045 transmitter and receiver pair are designed to perform high-speed serial data transmission over fiber optic or coaxial cable interfaces conforming to the requirements of the ANSI X3T11 Fibre Channel specification. The chipset is Gigabaud Link Module (GLM) compliant and supports 1062 Mb/s (GLM) and 531 Mb/s Half-GLM (HGLM) and 266 Mb/s Quarter-GLM (QGLM) modes with associated 10 or 20-bit data word.

The chipset performs parallel-to-serial and serial-to-parallel conversion and framing for block-encoded data. The S2044 on-chip PLL synthesizes the high-speed clock from a low-speed reference. The S2045 on-chip PLL synchronizes directly to incoming digital signals, to receive the data stream. The transmitter and receiver each support differential PECL-compatible I/O for fiber optic component interfaces, to minimize crosstalk and maximize data integrity. Local loopback allows for system diagnostics. The I/O section can operate from either a +3.3V or a +5V power supply. With a 3.3V power supply the chipset dissipates only 1W typically.

Figure 1 shows a typical network configuration incorporating the chipset. The chipset is compatible with AMCC's S2036 Open Fiber Control (OFC) device.

***Figure 1. System Block Diagram***



## OVERVIEW

The S2044 transmitter and S2045 receiver provide serialization and deserialization functions for block-encoded data to implement a Fibre Channel interface. Operation of the S2044/S2045 chips is straightforward, as depicted in Figure 2. The sequence of operations is as follows:

**Transmitter**

1. 10/20-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

**Receiver**

1. Clock and data recovery from serial input
2. Serial-to-parallel conversion
3. Frame detection
4. 10/20-bit parallel output

The 10/20-bit parallel data handled by the S2044 and S2045 devices should be from a DC-balanced encoding scheme, such as the 8B/10B transmission code, in which information to be transmitted is encoded 8 bits at a time into 10-bit transmission characters[1].

Internal clocking and control functions are transparent to the user. Details of data timing can be seen in Figure 5.

A lock detect feature is provided on the receiver, which indicates that the PLL is locked (synchronized) to the data stream.

**Loopback**

Local loopback is supported by the chipset, and provides a capability for performing offline testing of the interface to ensure the integrity of the serial channel before enabling the transmission medium. It also allows for system diagnostics.

***Figure 2. Fibre Channel Interface Diagram***

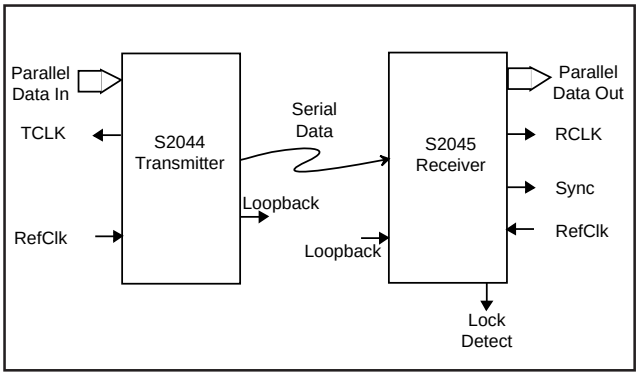
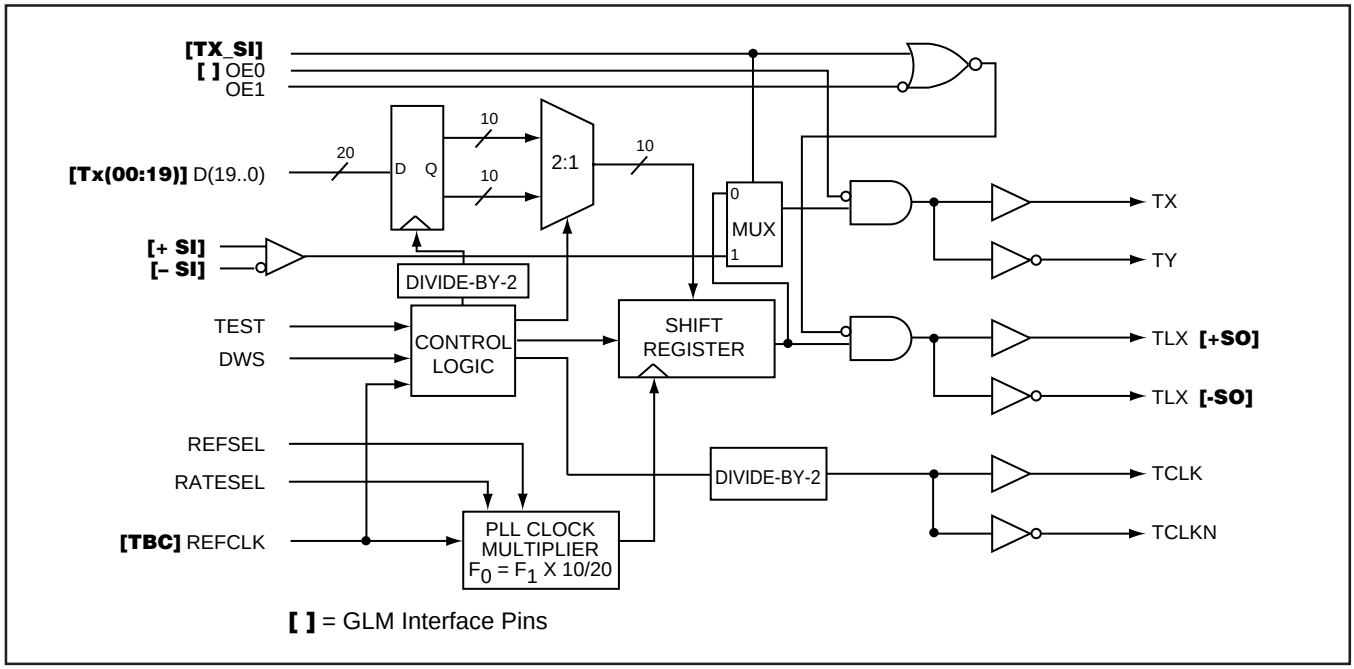



***Table 1. Transmitter Operating Modes***

| RATESEL | DWS | REFSEL | Data Rate (Mbits/sec) | Word Width (Bits) | Reference Clock Frequency (MHz) | TCLK/TCLKN Frequency (MHz) |
|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1062.5 | 10 | 106.25 | 53.125 |
| 0 | 0 | 0 | 1062.5 | 20 | 53.125 | 53.125 |
| 1 | 1 | 1 | 531.25 | 10 | 53.125 | 53.125 |
| 1 | 0 | 0 | 531.25 | 20 | 26.5625 | 26.5625 |
| Open | 1 | 1 | 265.625 | 10 | 26.5625 | 26.5625 |

***Figure 3. S2044 Functional Block Diagram***




1. A.X. Widmer and P.A. Franaszek, “A Byte-Oriented DC Balanced (0,4) 8B/10B Transmission Code,” IBM Research Report RC 9391, May 1982.


Applied Micro Circuits Corporation
6195 Lusk Blvd., San Diego, CA 92121 • (619) 450-9333

## S2044 TRANSMITTER FUNCTIONAL DESCRIPTION

The S2044 transmitter accepts parallel input data and serializes it for transmission over fiber optic or coaxial cable media. The chip is fully compatible with the ANSI X3T11 Fibre Channel standard, and supports the Fibre Channel standard's data rates of 1062, 531 and 266 Mbit/sec.

The parallel input data word can be either 10 bits or 20 bits wide, depending upon DWS pin selection. A block diagram showing the basic chip function is shown in Figure 3.

### Parallel/Serial Conversion

The parallel-to-serial converter takes in 10-bit or 20-bit wide data from the input latch and converts it to a serial data stream. Parallel data is latched into the transmitter on the positive going edge of REFCLK. The data is then clocked synchronous to the clock synthesis unit serial clock into the serial output shift register. The shift register is clocked by the internally generated bit clock which is 10 times the REFCLK input frequency. The state of the serial outputs is controlled by the output enable pins, OE0 and OE1. D10 is transmitted first in 10-bit mode. D0 is transmitted first in 20-bit mode. Table 2 shows the mapping of the parallel data to the 8B/10B codes.

### 10-Bit/20-Bit Mode

The S2044 operates with either 10-bit or 20-bit parallel data inputs. Word width is selectable via the DWS pin. In 10-bit mode, D10–D19 are used and D0-D9 are ignored.

### Reference Clock Input

The reference clock input (REFCLK) must be supplied with a PECL single-ended AC coupled crystal clock source with 100 PPM tolerance to assure that the transmitted data meets the Fibre Channel frequency limits. The internal serial clock is frequency locked to the reference clock. The word rate clock (TCLK, TCLKN) output frequency is determined by the selected operating speed and word width. Refer to Table 1 for TCLK/TCLKN clock frequencies.

***Table 2. Data Mapping to 8b/10b Alphabetic Representation***

| | First Data Byte | | | | | | | | | | Second Data Byte | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TX[00:19] or RX[00:19] | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 |
| 8b/10b alphabetic representation | a | b | c | d | e | i | f | g | h | j | a | b | c | d | e | i | f | g | h | j |
| | ↑ First bit transmitted in 20-bit mode | | | | | | | | | | ↑ First bit transmitted in 10-bit mode | | | | | | | | | |

***Figure 4. S2045 Functional Block Diagram***

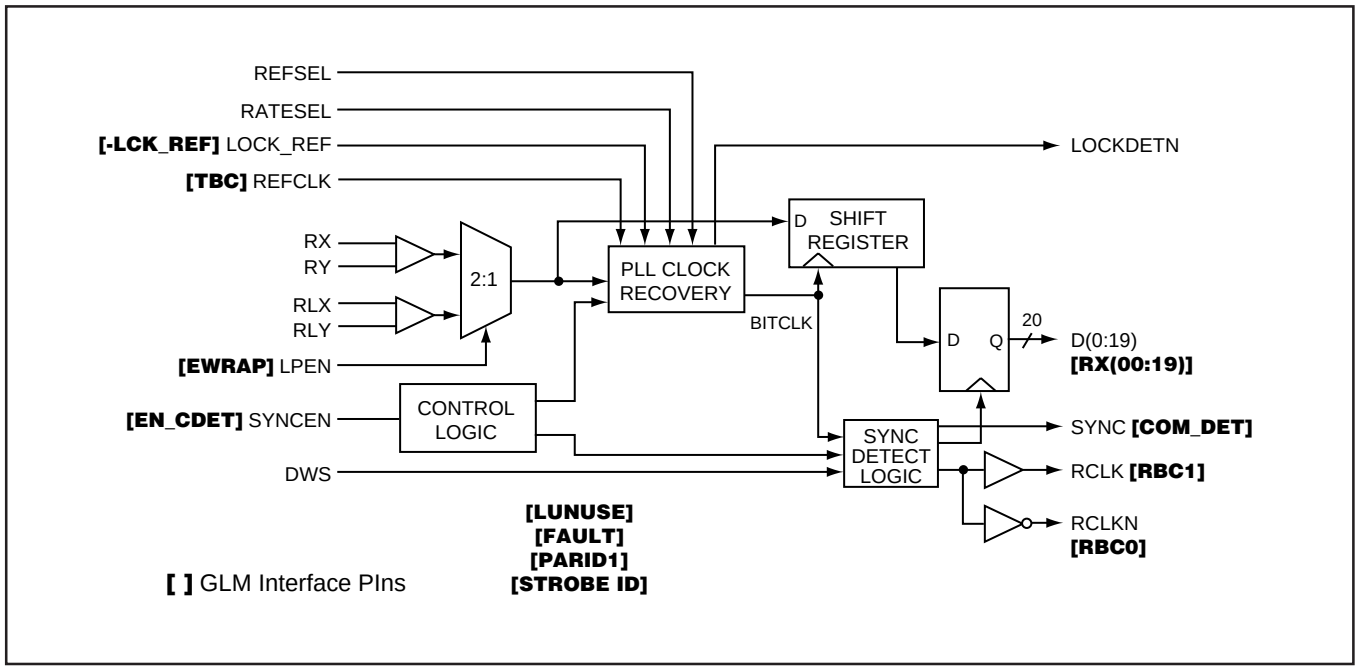


***Figure 5. Functional Waveform***

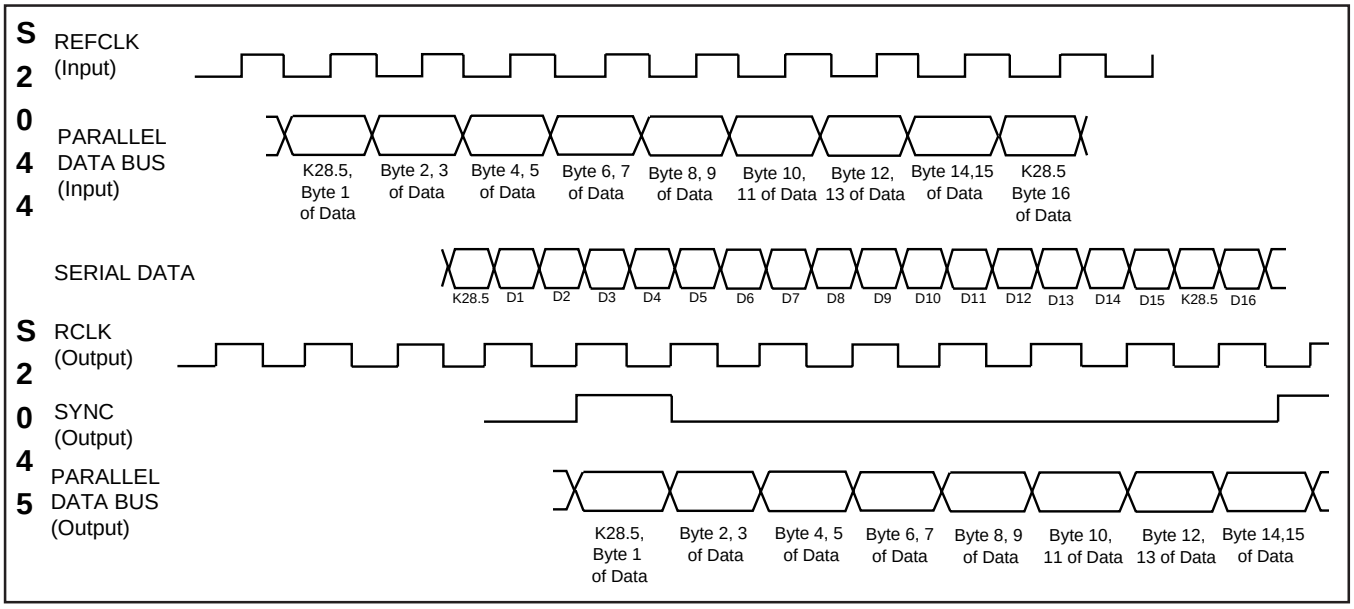



***Table 3. Data Mapping to 8b/10b Alphabetic Representation***

| | First Data Byte | | | | | | | | | | Second Data Byte | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TX[00:19] or RX[00:19] | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 |
| 8b/10b alphabetic representation | a | b | c | d | e | i | f | g | h | j | a | b | c | d | e | i | f | g | h | j |
| | ↑ First bit received in 20-bit mode | | | | | | | | | | ↑ First bit received in 10-bit mode | | | | | | | | | |

## S2045 RECEIVER FUNCTIONAL DESCRIPTION

The S2045 receiver is designed to implement the ANSI X3T11 Fibre Channel specification receiver functions. A block diagram showing the basic chip function is provided in Figure 5.

Whenever a signal is present, the S2045 attempts to achieve synchronization on both bit and transmission-word boundaries of the received encoded bit stream. Received data from the incoming bit stream is provided on the device's parallel data outputs.

The S2045 accepts serial encoded data from a fiber optic or coaxial cable interface. The serial input stream is the result of the serialization of 8B/10B encoded data by an FC compatible transmitter. Clock recovery is performed on-chip, with the output data presented to the Fibre Channel transmission layer as 10- or 20-bit parallel data. The chip is programmable to operate at the Fibre Channel specified operating frequencies of 1062, 531 and 266 Mbit/s.

### Serial/Parallel Conversion

Serial data is received on the RX, RY pins. The PLL clock recovery circuit will lock to the data stream if the clock to be recovered is within ±100 PPM of the internally generated bit rate clock. The recovered clock is used to retime the input data stream. The data is then clocked into the serial to parallel output registers. The parallel data out can be either 10 or 20 bits wide determined by the state of the DWS pin. The word clock (RCLK) is synchronized to the incoming data stream word boundary by the detection of the fiber channel K28.5 synchronization pattern (0011111010, positive running disparity).

### 10-Bit/20-Bit Mode

The S2045 will operate with either 10-bit or 20-bit parallel data outputs. This option is selectable via the DWS pin. See Tables 3 and 4. In 10-bit mode, D10–D19 are used and D0–D9 are driven to the logic high state.

***Figure 6. Loopback Diagram***

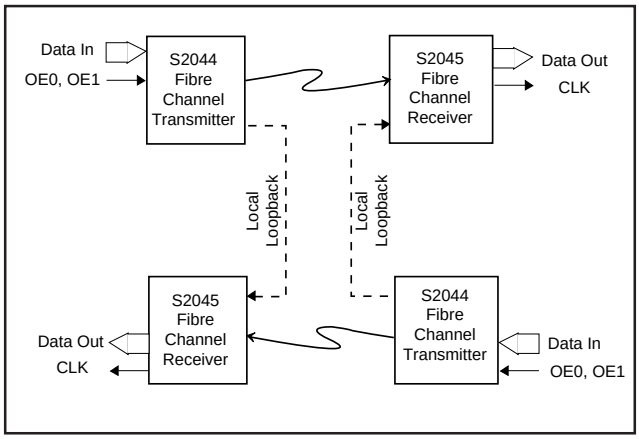



***Table 4. Receiver Operating Modes***

| RATESEL | DWS | REFSEL | Data Rate (Mbits/sec) | Word Width (Bits) | Reference Clock Frequency (MHz) | RCLK/RCLKN Frequency (MHz) |
|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1062.5 | 10 | 106.25 | 53.125 |
| 0 | 0 | 0 | 1062.5 | 20 | 53.125 | 53.125 |
| 1 | 1 | 1 | 531.25 | 10 | 53.125 | 53.125 |
| 1 | 0 | 0 | 531.25 | 20 | 26.5625 | 26.5625 |
| Open | 1 | 1 | 265.625 | 10 | 26.5625 | 26.5625 |

### Reference Clock Input

The reference clock input must be supplied with a PECL single-ended AC coupled crystal clock source at ±100 PPM tolerance. See Table 4 for reference clock frequencies.

### Framing

The S2045 provides SYNC character recognition and data word alignment of the TTL level compatible output data bus. During the data realignment process, the RCLK phase will be adjusted. No glitches will occur in the RCLK signal due to the realignment. In systems where the SYNC detect function is undesired, a LOW on the SYNCEN input disables the SYNC function and the data will be “un-framed”.

When framing is disabled by low SYNCEN, the S2045 simply achieves bit synchronization within 250 bit times and begins to deliver parallel output data words whenever it has received full transmission words. No attempt is made to synchronize on any particular incoming character.

The SYNC output signal will go high whenever a K28.5 character (positive disparity) is present on the parallel data outputs. The SYNC output signal will be low at all other times. This is true whether the S2045 is operating in 10-bit mode or in 20-bit mode.

### Lock Detect

The S2045 lock detect function indicates the state of the phase-locked loop (PLL) clock recovery unit. The PLL will indicate lock within 250 bit times after the start of receiving serial data inputs. If the serial data inputs have an instantaneous phase jump (from a serial switch, for example) the PLL will not indicate an out-of-lock state, but will recover the correct phase alignment within 250 bit times. If a run length of 64 bits is exceeded, or if the transition density is less than 12%, the loop will be declared out of lock and will attempt to re-acquire bit synchronization. When lock is lost, the PLL will shift from the serial input data to the reference clock, so that correct frequency downstream clocking will be maintained.

In any transfer of PLL control from the serial data to the reference clock, the RCLK/RCLKN output remains phase continuous and glitch free, assuring the integrity of downstream clocking.

### Start-Up Procedure

The clock recovery PLL requires an initilization procedure to correctly achieve lock on the serial data inputs. At power-up or loss of lock, the PLL must first acquire frequency lock to the local reference clock. This can be accomplished connecting the –LOCK_REF pin to a 10 ms reset signal. If this is not possible, the PLL can also be initialized by guaranteeing that no data is seen at the serial data inputs for a minimum of 10 ms upon power-up. If the serial data inputs cannot be controlled, then the S2045 can be put into the loopback mode and the loopback outputs of the S2044 must be quiescent for a minimum of 10 ms after power-up.

## OTHER OPERATING MODES

### Loopback

Local loopback requires a S2044 and a S2045 as shown in Figure 6. When enabled, serial data from the S2044 transmitter is sent to the S2045 receiver, where the clock is extracted and the data is deserialized. The parallel data is then sent to the subsystem for verification. This loopback mode provides the capability to perform offline testing of the interface to guarantee the integrity of the serial channel before enabling the transmission medium. It also allows system diagnostics.

### Operating Frequency Range

The S2044 and S2045 are optimized for operation at the Fibre Channel rates of 265.625, 531.25, and 1062.5 Mbit/s. Operation in other than Fibre channel rates is possible if the rate falls within ±10% of the nominal rate. REFCLK must be selected to be within 100 ppm of the desired byte or word clock rate.

### Test Modes

The TEST pin on the S2044 and the SYNCEN pin on the S2045 provide a PLL bypass mode that can be used for operating the digital area of the chip. In this mode, clock signals are input through the reference clock pins. This can be used for testing the device during the manufacturing process or during an off-line self-test. Sync detection is always enabled in test mode.

***S2044 Pin Assignment and Descriptions***

| Pin Name | Level | I/O | Pin # | Description |
|---|---|---|---|---|
| D19<br>D18<br>D17<br>D16<br>D15<br>D14<br>D13<br>D12<br>D11<br>D10<br>D9<br>D8<br>D7<br>D6<br>D5<br>D4<br>D3<br>D2<br>D1<br>D0 | TTL | I | 50<br>49<br>48<br>47<br>44<br>43<br>42<br>41<br>38<br>37<br>36<br>35<br>31<br>30<br>29<br>28<br>25<br>24<br>23<br>22 | Accepts parallel input data. Data is clocked in on the rising edge of REFCLK. In 20-bit mode, D0 is transmitted first. In 10-bit mode, D10-19 are used, D0-D9 are ignored, and D10 is transmitted first. |
| TEST | Static TTL | I | 20 | Multilevel input used for factory testing. When not connected, REFCLK replaces the internal bit clock to facilitate factory testing. In normal use, this input is wired to ground. |
| DWS | Static TTL | I | 19 | The level on this pin selects the parallel data bus width. When LOW, a 20-bit parallel bus width is selected, and D(0-19) are active. When HIGH, a 10-bit parallel data bus is selected, D(10-19) are active and D(0-9) are not used. (See Table 1.) A rising edge will reset the part (used for test). |
| REFCLK | PECL | I | 16 | (Externally capacitively coupled.) A crystal-controlled reference clock for the PLL clock multiplier. The frequency of REFCLK is set by the REFSEL pin. (See Table 1.) |
| TCLK<br>TCLKN | Diff. TTL | O | 12<br>11 | Differential TTL word rate clock true and complement. See Table 1 for frequency. |
| TY<br>TX | Diff. PECL | O | 9<br>8 | Differential PECL outputs that transmit the serial data and drive 75 or 50 termination to Vcc– 2V. Enabled by OE0. TX is the positive output, and TY is the negative output. |
| TLX<br>TLY | Diff. PECL | O | 5<br>4 | Differential PECL outputs that are functionally equivalent to TX and TY. They are intended to be used for loopback testing. Enabled by OE1. |

***S2044 Pin Assignment and Descriptions (Continued)***

| Pin Name | Level | I/O | Pin # | Description |
|---|---|---|---|---|
| OE0 | Static TTL | I | 2 | Active low output-enable control for TX/TY outputs. TX/TY will go to the logic low state when disabled. |
| OE1 | TTL | I | 1 | Active low output-enable control for TLX/TLY outputs. TLX/TLY will go to the logic low state when disabled. |
| REFSEL | Static TTL | I | 18 | Multilevel input used to select the reference clock frequency. (See Table 1.) |
| RATESEL | Static TTL | I | 15 | Multilevel input used to select the operating speed of the transmitter. (See Table 1.) |
| ECLVCC | +3.3V | – | 21, 39 | Core +3.3V |
| TTLGND | GND | – | 14 | TTL Ground |
| TTLVCC | +3.3V/ +5V | – | 17 | TTL Power Supply (+5V if TTL) |
| ECLIOVCC | +3.3V | – | 3, 10 | PECL I/O Power Supply |
| ECLIOVEE | +3.3V | – | 6, 7 | PECL I/O Power Supply |
| AVCC | +3.3V | – | 27, 32 | Analog Power Supply |
| AVEE | GND | – | 26, 33 | Analog Ground |
| ECLVEE | GND | – | 13, 40, 51, 52 | Core Ground |
| TX_SI | Multi-level | I | 34 | Multilevel signal that determines where the data which is presented to the link comes from and whether the ±SO signals are enabled. When this input is low, the TX/TY outputs transmit the serialized data from the parallel transmit data lines. When this input is high, the TX/TY outputs transmit the data from the ±SI inputs. |
| +SI<br>–SI | Diff. PECL | I | 45<br>46 | These inputs are a serial data stream (1.0625 Gb/s, 531.25 Mb/s, 265.625) which shall control the link modulation (TX/TY) if the TX_SI input is high. |

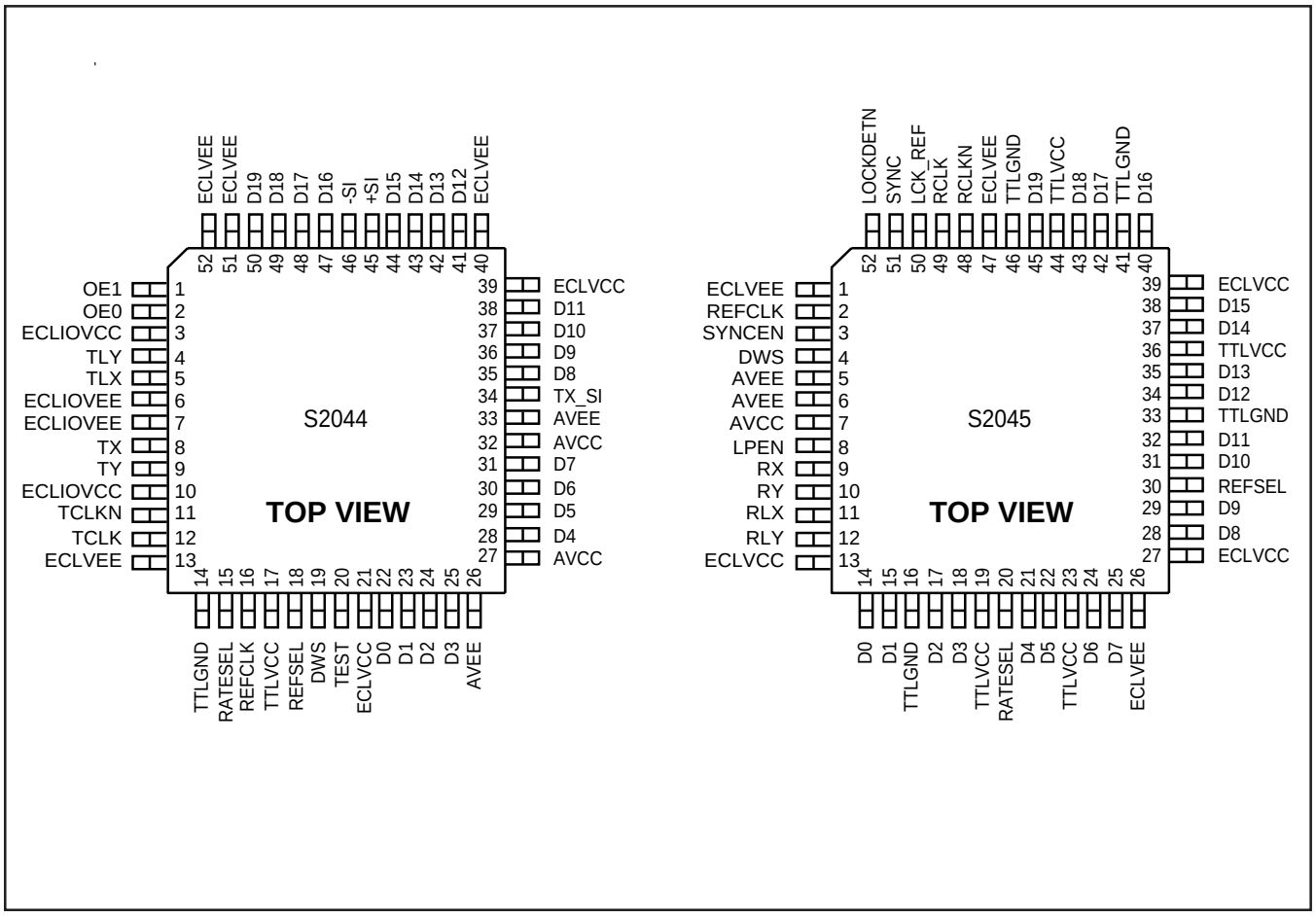
***S2045 Pin Assignment and Descriptions***

| Pin Name | Level | I/O | Pin # | Description |
|---|---|---|---|---|
| D19<br>D18<br>D17<br>D16<br>D15<br>D14<br>D13<br>D12<br>D11<br>D10<br>D9<br>D8<br>D7<br>D6<br>D5<br>D4<br>D3<br>D2<br>D1<br>D0 | TTL | O | 45<br>43<br>42<br>40<br>38<br>37<br>35<br>34<br>32<br>31<br>29<br>28<br>25<br>24<br>22<br>21<br>18<br>17<br>15<br>14 | Outputs parallel data. The width of the parallel data bus is selected by the state of the DWS pin. Parallel data on this bus is clocked out on the falling edge of RCLK. In 20-bit mode, D0 is the first bit received. In 10-bit mode, D10-D19 are used and D0-D9 are driven to the high state. In 10-bit mode, D10 is the first bit received. |
| LOCKDETN | TTL | O | 52 | When LOW, LOCKDETN indicates that the PLL is locked to the incoming data stream. When HIGH, it provides a system flag indicating that the PLL is locked to the local reference clock. |
| LPEN | TTL | I | 8 | When HIGH, LPEN selects the loopback differential serial input pins. When LOW, LPEN selects RX and RY (normal operation). |
| DWS | Static TTL | I | 4 | The level on this pin selects the parallel data bus width. When LOW, a 20-bit parallel bus width is selected, and D(0-19) are active. When HIGH, a 10-bit parallel data bus is selected, D(10-19) are active and D(0-9) will go HIGH. (See Table 4.) A rising edge will reset the internal counters (used for test). |
| RCLK<br>RCLKN | Diff. TTL | O | 49<br>48 | The falling edge of RCLK outputs a new word on the data bus. After a sync word is detected, the period of the current RCLK and RCLKN is stretched to align with the word boundary. (See Table 4 for frequency.) |
| REFCLK | PECL | I | 2 | (Externally capacitively coupled.) A free-running crystal-controlled reference clock for the PLL clock multiplier. The frequency of REFCLK is set by the REFSEL pin. (See Table 4.) |
| SYNC | TTL | O | 51 | Upon detection of a valid sync symbol, this output goes high for one RCLK period. When sync is active, the sync symbol shall be present on the parallel data bus bits D0-D9 in 20-bit mode or D10-D19 in 10-bit mode. |
| RLX<br>RLY | Diff. PECL | I | 11<br>12 | (Externally capacitively coupled.) The serial loopback data inputs. RLX is the positive input, and RLY is the negative input. |
| RX<br>RY | Diff. PECL | I | 9<br>10 | (Externally capacitively coupled.) The received serial data inputs. RX is the positive input, and RY is the negative input. |

***S2045 Pin Assignment and Descriptions (Continued)***

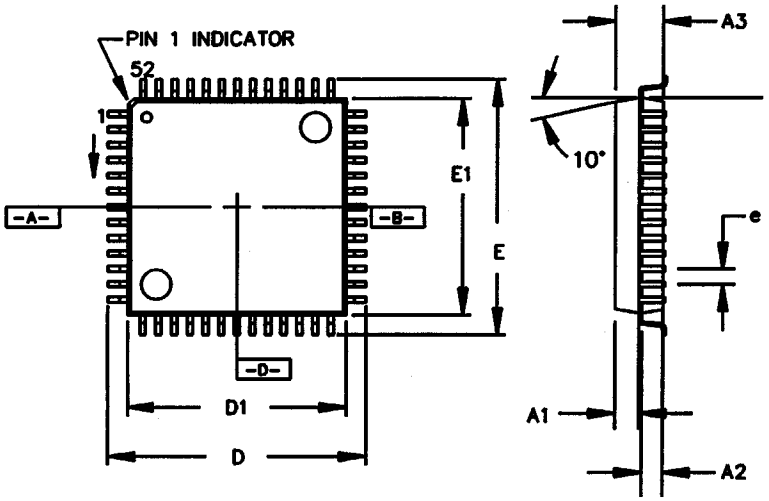
| Pin Name | Level | I/O | Pin # | Description |
|---|---|---|---|---|
| SYNCEN | Static TTL | I | 3 | (Multilevel.) When HIGH, enables sync detection. Detection of the sync pattern (K28.5:0011111010, positive running disparity) will determine the word boundary for the data to follow. When open (not connected), REFCLK replaces internal bit clock to facilitate factory testing. In this mode of operation, sync detection is always enabled. When LOW, data is treated as unframed data. |
| REFSEL | Static TTL | I | 30 | (Multilevel.) Input used to select the reference clock frequency. (See Table 4.) |
| RATESEL | Static TTL | I | 20 | (Multilevel.) Input used to select the operating speed of the receiver. (See Table 4.) |
| LOCK_REF | TTL | I | 50 | When LOW, forces the PLL to lock to the REFCLK input and ignore the serial data inputs. |
| ECLVCC | +3.3V | – | 13, 27, 39 | Core Power Supply |
| TTLGND | GND | – | 16, 33, 41, 46 | TTL Ground (0V) |
| TTLVCC | +5V or +3.3V | – | 19, 23, 36, 44 | TTL Power Supply (+5V or +3.3V) |
| AVCC | +3.3V | – | 7 | Analog Power Supply (+3.3V) |
| AVEE | GND | – | 5, 6 | Analog Ground (0V) |
| ECLVEE | GND | – | 1, 26, 47 | Core Ground (0V) |

***Figure 7. S2044 and S2045 52 PQFP Pinouts***



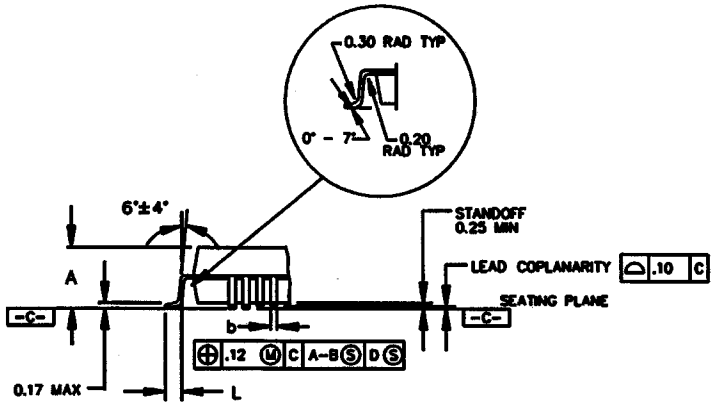

TTLVCC = +5V or +3.3V
AVCC = +3.3V
ECLVCC = +3.3V
ECLIOVCC = +3.3V
ECLIOVEE = 0V
TTLGND = 0V
ECLVEE = 0V
AVEE = 0V

*Figure 8. 52 PQFP — (10mm x 10mm) Plastic Quad Flat Pack*




DIMENSIONS ARE IN MM

| BODY SIZE PLUS LEADS / DIM LTR / TOL | 3.2 MM FOOTPRINT 52 |
|---|---|
| e | BASIC 0.65 |
| b | ±.05 0.30 |
| A | MAX 2.45 |
| $A_1$ | ±.10 0.64 |
| $A_2$ | ±.10 0.64 |
| $A_3$ | ±.10 2.00 |
| D | ±.25 13.20 |
| $D_1$ | ±.10 10.00 |
| E | ±.25 13.20 |
| $E_1$ | ±.10 10.00 |
| L | ±.15 0.88 |



### *Absolute Maximum Ratings*

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Case Temperature under Bias | -55 | | 125 | °C |
| Junction Temperature under Bias | -55 | | 150 | °C |
| Storage Temperature | -65 | | 150 | °C |
| Voltage on VCC with Repect to GND | -0.5 | | +7.0 | V |
| Voltage on any TTL Input Pin | -0.7 | | VCC +.6V | V |
| Voltage on any PECL Input Pin | 0 | | ECL/ VCC | V |
| TTL Output Sink Current | | | 8 | mA |
| TTL Output Source Current | | | 8 | mA |
| High Speed PECL Output Source Current | | | 50 | mA |
| Static Discharge Voltage | | 500 | | V |

### *Recommended Operating Conditions*

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Ambient Temperature under Bias | 0 | | 70 | °C |
| Junction Temperature under Bias | | | 130 | °C |
| Voltage on TTLVCC with Respect to GND<br>5V Operation<br>3.3V Operation | <br>4.75<br>3.13 | <br>5.0<br>3.3 | <br>5.25<br>3.47 | <br>V<br>V |
| Voltage on any TTL Input Pin | 0 | | 5.25 | V |
| Voltage on ECLVCC with respect to GND | 3.13 | 3.3 | 3.47 | V |
| Voltage on any PECL Input Pin | ECL/VCC -2.0 | | ECL/VCC | V |

### *S2044 DC Characteristics*

| Parameters | Description | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage (TTL)<br>– 3.3V Power Supply<br>– 3.3V Power Supply<br>– 5V Power Supply | <br>2.1<br>2.2<br>2.7 | | | <br>V<br>V<br>V | <br>$V_{CC}$ = min, $I_{OH}$ = -2.4mA<br>$V_{CC}$ = min, $I_{OH}$ = -.1mA<br>$V_{CC}$ = min, $I_{OH}$ = -1mA |
| $V_{OL}$ | Output LOW Voltage (TTL)<br>– 3.3V Power Supply<br>– 5V Power Supply | | | <br>.5<br>.5 | <br>V<br>V | <br>$V_{CC}$ = min, $I_{OL}$ = 2.4mA<br>$V_{CC}$ = min, $I_{OL}$ = 4mA |
| $V_{IH}$ | Input HIGH Voltage (TTL) | 2.0 | — | 5.5 | V | $I_H \leq$ 1mA at $V_{IH}$ = 5.5V |
| $V_{IL}$ | Input LOW Voltage (TTL) | 0 | — | 0.8 | V | — |
| $I_{IH}$ | Input HIGH Current (TTL) | — | — | 50 | µA | $V_{IN}$ = 2.4V |
| $I_{IL}$ | Input LOW Current (TTL) | -500 | — | -50 | µA | $V_{IN}$ = 0.5V |
| $I_{CC}$ | Supply Current | | 123 | 160 | mA | Outputs open, $V_{CC} = V_{CC}$ max |
| $P_D$ | Power Dissipation | | .406 | .554 | W | Outputs open, $V_{CC} = V_{CC}$ max |
| $\Delta V_{INCLK}$ | Single-ended REFCLK input swing | 440 | — | 1300 | mV | AC coupled |
| $\Delta V_{OUT}$ | Serial Output Voltage Swing | 600 | — | 1600 | mV | 50Ω to $V_{CC}$ -2.0V |

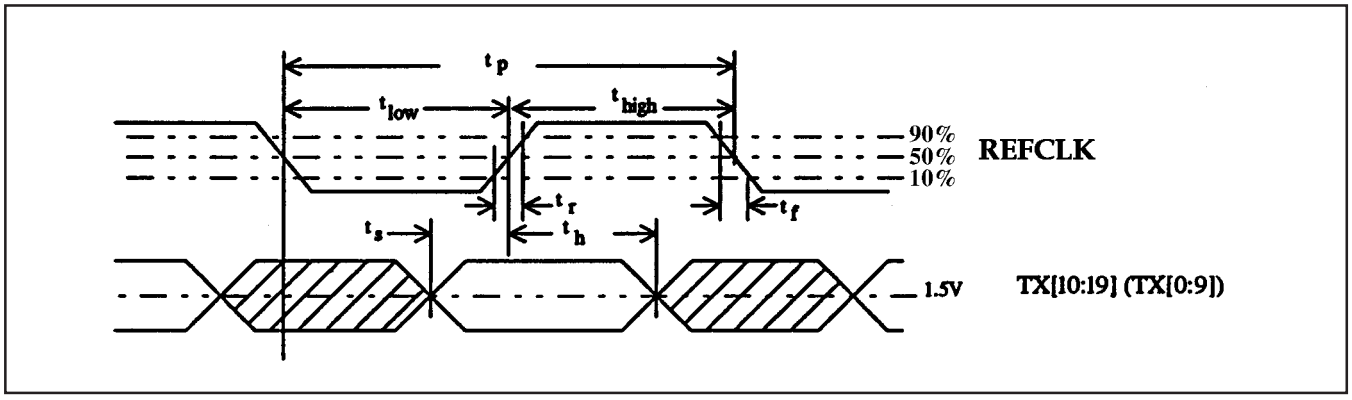
### *S2045 DC Characteristics*

| Parameters | Description | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage (TTL)<br>– 3.3V Power Supply<br>– 3.3V Power Supply<br>– 5V Power Supply | <br>2.1<br>2.2<br>2.7 | | | <br>V<br>V<br>V | <br>$V_{CC}$ = min, $I_{OH}$ = -2.4mA<br>$V_{CC}$ = min, $I_{OH}$ = -.1mA<br>$V_{CC}$ = min, $I_{OH}$ = -1mA |
| $V_{OL}$ | Output LOW Voltage (TTL)<br>– 3.3V Power Supply<br>– 5V Power Supply | | | <br>.5<br>.5 | <br>V<br>V | <br>$V_{CC}$ = min, $I_{OL}$ = 2.4mA<br>$V_{CC}$ = min, $I_{OL}$ = 8mA |
| $V_{IH}$ | Input HIGH Voltage (TTL) | 2.0 | — | 5.5 | V | $I_H \leq$ 1mA at $V_{IH}$ = 5.5V |
| $V_{IL}$ | Input LOW Voltage (TTL) | 0 | — | 0.8 | V | — |
| $I_{IH}$ | Input HIGH Current (TTL) | — | — | 50 | µA | $V_{IN}$ = 2.4V |
| $I_{IL}$ | Input LOW Current (TTL) | -500 | — | -50 | µA | $V_{IN}$ = 0.5V |
| $I_{CC}$ | Supply Current<br>– 10-Bit Mode<br>– 20-Bit Mode | | <br>187<br>194 | <br>256<br>267 | <br>mA<br>mA | <br>Outputs open, $V_{CC} = V_{CC}$ max<br>Outputs open, $V_{CC} = V_{CC}$ max |
| $P_D$ | Power Dissipation<br>– 3.3V Supply, 10-Bit Mode<br>– 3.3V Supply, 20-Bit Mode<br>– 5V Supply, 10-Bit Mode<br>– 5V Supply, 20-Bit Mode | | <br>.617<br>.640<br>.728<br>.778 | <br>.887<br>.925<br>1.08<br>1.142 | <br>W<br>W<br>W<br>W | <br>Outputs open, $V_{CC} = V_{CC}$ max<br>Outputs open, $V_{CC} = V_{CC}$ max<br>Outputs open, $V_{CC} = V_{CC}$ max<br>Outputs open, $V_{CC} = V_{CC}$ max |
| $\Delta V_{INCLK}$ | Single-ended REFCLK input swing | 440 | — | 1300 | mV | AC coupled |
| $V_{DIFF}$ | Min. differential input voltage swing for differential PECL inputs | 100 | | 1300 | mV | |

### Timing

The data on the TX[00:09] (TX[00:19]) data bus will be sampled on every rising edge of REFCLK. The data will be serialized and transmitted onto the serial link if EWRAP is low and TX_SI is low. The figure below illustrates the timing requirements of REFCLK with respect to the TX[10:19] (TX[0:9]) signals, minimum high and low durations, and the rising and falling slew rate magnitudes. In addition, this system supplied clock must not have more jitter than ±20% of a baud interval.

***REFCLK Timing Diagram***



***REFCLK Timing Table***

| Parameter | Symbol | Min. | Max. | Units | Comments[1] |
|---|---|---|---|---|---|
| Frequency 26.5625 MHz<br>53.125 MHz | f | 25.5598<br>53.119 | 26.5652<br>53.131 | MHz | This is dependent on the link rate and the data path width. |
| Jitter 265.625 MBaud<br>531.25 MBaud<br>1062.5 MBaud | | | 753<br>376<br>188 | ps<br>pk-pk | This is the maximum total jitter allowed by the Fiber Channel standard. |
| Period (f=26.5625 MHz) | $t_p$ | 37.64 | 37.66 | ns | |
| Period (f=53.125 MHz) | $t_p$ | 18.82 | 18.83 | ns | |
| REFCLK Low Time | $t_{low}$ | 6 | | ns | |
| REFCLK High Time | $t_{high}$ | 6 | | ns | |
| TX Setup to REFCLK (GLM, HGLM) | $t_s$ | 2 | | ns | |
| TX Setup to REFCLK (QGLM, EGLM) | $t_s$ | 6 | | ns | |
| TX Hold From REFCLK | $t_h$ | 3.3 | | ns | |
| REFCLK Rise Time | $t_r$ | 0.5 | 3.2 | ns | This applies to the REFCLK input. |
| REFCLK Fall Time | $t_f$ | 0.5 | 3.2 | ns | This applies to the REFCLK input. |

1. All parameters are for outputs driven into a 35pF lumped capacitive load.

***Serial Data Timing Table (TLX, TLY; TX, TY)***

| Parameters | Description | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| $T_{JRMS}$ | Serial data output random jitter (RMS) | — | 20 | ps | RMS, tested on a sample basis. Measured with 1010 pattern. |
| $T_{DJ}$ | Serial data output deterministic jitter (p-p) | — | 100 | ps | Peak-to-peak, tested on a sample basis. Measured with IDLE pattern. |
| $T_{SDR}$, $T_{SDF}$ | Serial data rise and fall | — | 300 | ps | 20% to 80%, tested on a sample basis. |

Tested per Figure 10.

### Timing

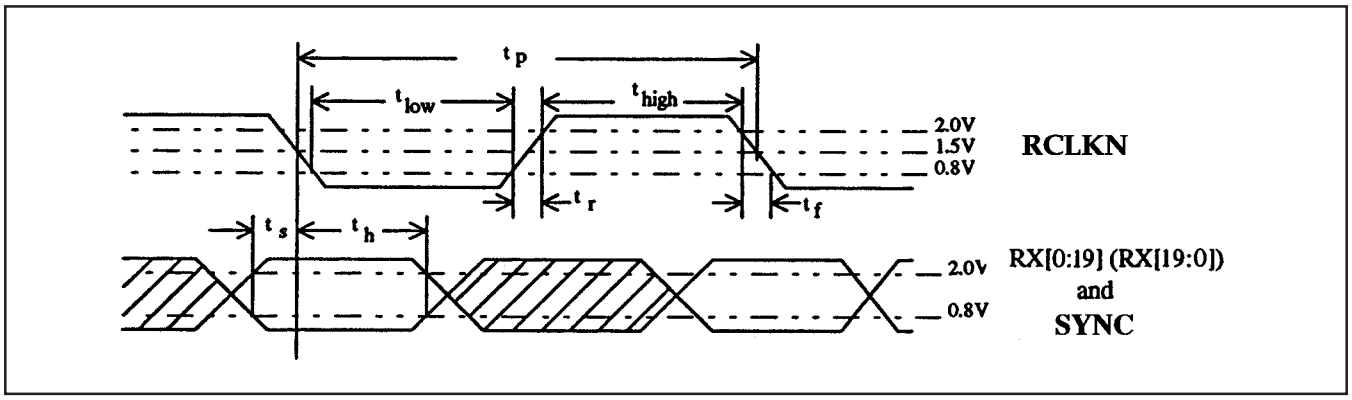
This section will detail the timing requirements of all of the signals on the GLM interface. All timing is measured into a lumped 35pf capacitive load.

### RBC[0] Timing

When -LCK_REF is pulled low, RCLKN should be in local phase lock with TBC within 500µs. -LCK_REF, when activated, shall stay low for a duration of at least 500µs if receiver frequency lock is to be expected. After local phase lock has been acquired, and when EWRAP is high, 2500 baud times after -LCK_REF is driven high, RCLKN shall be in phase lock with REFCLK. After local phase lock has been acquired, and when EWRAP is low, 250 baud times after -LCK_REF is driven high, RCLKN shall be in phase lock with the incoming serial data stream.

When a 53 MHz GLM family module is in frequency lock (either with REFCLK or a serial data stream) RCLKN shall never have a high level duration (>2.0v) which is less than 6.5 ns, nor a low level duration (<0.8v) which is less than 5.8 ns (no clock shivering shall occur). At byte realignment, RCLKN clock states are to be extended rather than truncated). When the GLM family module is in frequency lock (either with REFCLK or a serial data stream) and -LCK_REF has been inactive for at least 2500 baud times the minimum instantaneous period shall always be greater that 18.36 ns. When the PLL in the GLM is adjusting to a new phase or a new frequency, where both the old and new frequencies are valid Fibre Channel frequencies, RCLKN shall never have a period less than 18.36 ns. In response to an input data phase jump, the GLM shall meet the requirements of FC-PH clause 5.3 transparent to the host.

***RCLKN Timing Diagram***




***Serial Data Input Timing Table (RLX, RLY; RX, RY)***

| Parameters | Description | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| $R_{SDR}$ , $R_{SDF}$ | Serial data input rise and fall | — | 300 | ps | 20% to 80%. |
| $T_{LOCK}$ | Data acquisition lock time @ <1.0625Gb/s | — | 2.4 | µs | 8B/10B IDLE pattern sample basis |
| Input Jitter Tolerance | Input data eye opening allocation at receiver input for BER ≤1E–12 | 30% | — | bit time | As specified in Fibre Channel FC–PH standard eye diagram jitter mask. (See Figure 12.) For BER ≤ IE-9 see Figure 13. |

***RCLKN Timing Table***

| Parameter | Symbol | Min. | Max. | Units | Comments[2] |
|---|---|---|---|---|---|
| Frequency 26.5625 MHz<br>53.125 MHz | f | 25.5598<br>53.119 | 25.5652<br>53.131 | MHz | This is dependent on the link rate and the data path width. |
| Period in Lock | $t_p$ | 18.36 | | ns | In frequency lock[3]. |
| Out of Lock Period (f=26.5625 MHz) | $t_{oolp}$ | 18.83 | | ns | Not in frequency lock. |
| Out of Lock Period (f=53.125 MHz) | $t_{oolp}$ | 9.412 | | ns | Not in frequency lock. |
| RCLKN Low Time (f=53.125 MHz) | $t_{low}$ | 5.8 | | ns | |
| RCLKN High Time (f=53.125 MHz) | $t_{high}$ | 6.5 | | ns | |
| RCLKN Duty Cycle (f=26.5625 MHz) | | 40% | 60% | period | In frequency lock. |
| RX Setup to RCLKN (f=53.125 MHz) | $t_s$ | 2.5 | | ns | |
| RX Setup to RCLKN (f=26.5625 MHz) | $t_s$ | 6.0 | | ns | |
| RX Hold From RCLKN | $t_h$ | 7.5 | | ns | |
| RCLK/RCLKN Rise Time | $t_r$ | .75 | 2.4 | ns | This applies to the RCLKN output. |
| RCLKN Fall Time | $t_f$ | 0.7 | 3.0 | ns | This applies to the RCLKN output. |

2. All parameters are for outputs driven into a 35pf lumped capacitive load.
3. This is the absolute minimum RCLKN period while in frequency lock and must account for any adjustments to the clock to allow for a change in phase or frequency on the received serial link.

***Figure 9. Serial Input Rise and Fall Time***

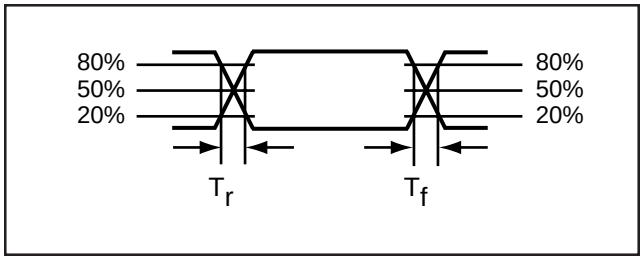



***Figure 10. Serial Output Load***

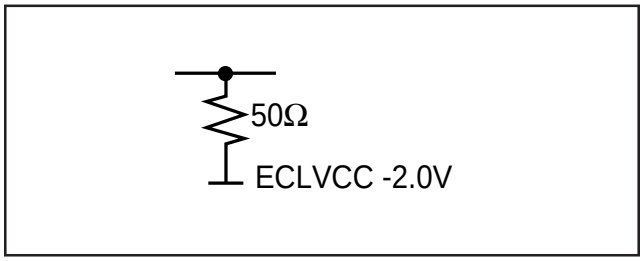



***Figure 11. TTL Input Rise and Fall Time***

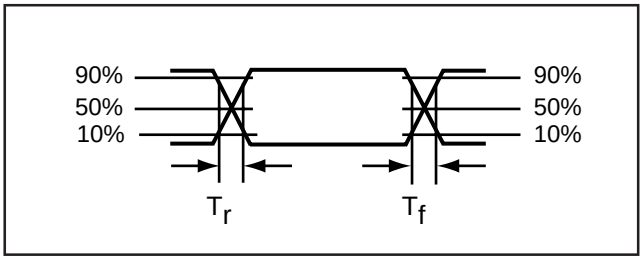
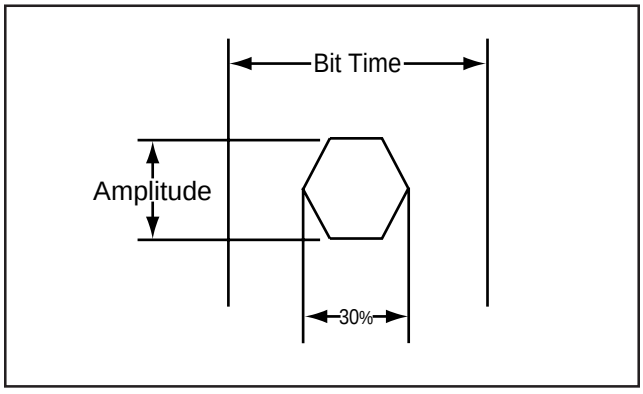


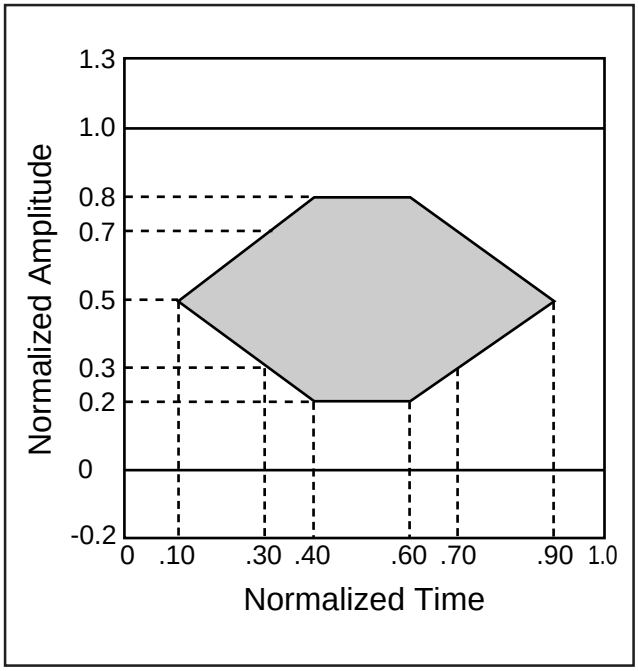

***Figure 12. Receiver Input Eye Diagram Jitter Mask***




## ACQUISITION TIME

With the input eye diagram shown in Figure 13, the S2045 will recover data with a $10^{-9}$ BER within 50 bit times after an instantaneous phase shift of the incoming data. Note: This is only valid after a 10 ms initial reset has been applied on power up.

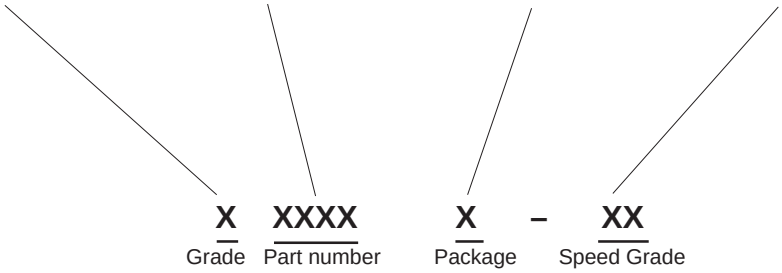
***Figure 13. Acquisition Time Eye Diagram***



***Ordering Information***

| GRADE | TRANSMITTER | PACKAGE | SPEED GRADE |
|---|---|---|---|
| S – commercial | 2044 | B – 52 PQFP | 5 – 531, 266 Mbit/s<br>10 – 1062, 531 and 266 Mbit/s |

| GRADE | RECEIVER | PACKAGE | SPEED GRADE |
|---|---|---|---|
| S – commercial | 2045 | B – 52 PQFP | 5 – 531, 266 Mbit/s<br>10 – 1062, 531 and 266 Mbit/s |




Example: S2044B-5—S2044 in a 52 PQFP package operating at 531 or 266 Mbits/sec rates.

**Applied Micro Circuits Corporation • 6195 Lusk Blvd., San Diego, CA 92121**
**Phone: (619) 450-9333 Fax: (619) 450-9885**
**http://www.amcc.com**