IDC Low Inductance Capacitors (RoHS)

0612/0508 IDC (InterDigitated Capacitors)

GENERAL DESCRIPTION

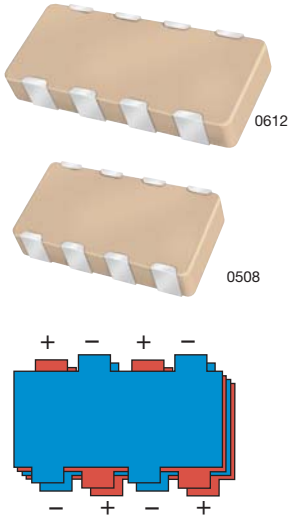
Inter-Digitated Capacitors (IDCs) are used for both semiconductor package and board level decoupling. The equivalent series inductance (ESL) of a single capacitor or an array of capacitors in parallel determines the response time of a Power Delivery Network (PDN). The lower the ESL of a PDN, the faster the response time. A designer can use many standard MLCCs in parallel to reduce ESL or a low ESL Inter-Digitated Capacitor (IDC) device. These IDC devices are available in versions with a maximum height of 0.95mm or 0.55mm.

IDCs are typically used on packages of semiconductor products with power levels of 15 watts or greater. Inter-Digitated Capacitors are used on CPU, GPU, ASIC, and ASSP devices produced on 0.13µ, 90nm, 65nm, and 45nm processes. IDC devices are used on both ceramic and organic package substrates. These low ESL surface mount capacitors can be placed on the bottom side or the top side of a package substrate. The low profile 0.55mm maximum height IDCs can easily be used on the bottom side of BGA packages or on the die side of packages under a heat spreader.

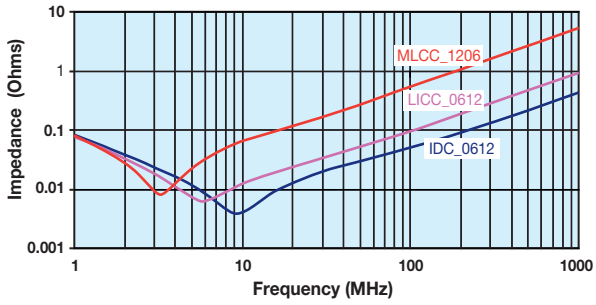
IDCs are used for board level decoupling of systems with speeds of 300MHz or greater. Low ESL IDCs free up valuable board space by reducing the number of capacitors required versus standard MLCCs. There are additional benefits to reducing the number of capacitors beyond saving board space including higher reliability from a reduction in the number of components and lower placement costs based on the need for fewer capacitors.

The Inter-Digitated Capacitor (IDC) technology was developed by AVX. This is the second family of Low Inductance MLCC products created by AVX. IDCs are a cost effective alternative to AVX's first generation low ESL family for high-reliability applications known as LICA (Low Inductance Chip Array).

AVX IDC products are available with a lead-free finish of plated Nickel/Tin.



TYPICAL IMPEDANCE



HOW TO ORDER

W	3	L	1	6	D	225	M	A	T	3	A
Style	**IDC Case Size** 2 = 0508 3 = 0612	**Low Inductance**	**Number of Terminals** 1 = 8 Terminals	**Voltage** 4 = 4V 6 = 6.3V Z = 10V Y = 16V 3 = 25V	**Dielectric** C = X7R D = X5R Z = X7S	**Capacitance Code (In pF)** 2 Sig. Digits + Number of Zeros	**Capacitance Tolerance** M = ±20%	**Failure Rate** A = N/A	**Termination** T = Plated Ni and Sn	**Packaging** Available 1=7" Reel 3=13" Reel	**Thickness** Max. Thickness mm (in.) A=0.95 (0.037) S=0.55 (0.022)

NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Numbers.

PERFORMANCE CHARACTERISTICS

Capacitance Tolerance	±20% Preferred
Operation Temperature Range	X7R = -55°C to +125°C X5R = -55°C to +85°C X7S = -55°C to +125°C
Temperature Coefficient	±15% (0VDC)
Voltage Ratings	4, 6.3, 10, 16 VDC
Dissipation Factor	4V, 6.3V = 6.5% max; 10V = 5.0% max; 16V = 3.5% max
Insulation Resistance (@+25°C, RVDC)	100,000MΩ min, or 1,000MΩ per µF min.,whichever is less

Dielectric Strength	No problems observed after 2.5 x RVDC for 5 seconds at 50mA max current
CTE (ppm/C)	12.0
Thermal Conductivity	4-5W/M K
Terminations Available	Plated Nickel and Solder
Max. Thickness	0.037" (0.95mm)

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SIZE		Thin 0508					0508					Thin 0612				0612			
Length	mm (in.)	2.03 ± 0.20 (0.080 ± 0.008)					2.03 ± 0.20 (0.080 ± 0.008)					3.20 ± 0.20 (0.126 ± 0.008)				3.20 ± 0.20 (0.126 ± 0.008)			
Width	mm (in.)	1.27 ± 0.20 (0.050 ± 0.008)					1.27 ± 0.20 (0.050 ± 0.008)					1.60 ± 0.20 (0.063 ± 0.008)				1.60 ± 0.20 (0.063 ± 0.008)			
Terminal Pitch	mm (in.)	0.50 ± 0.05 (0.020 ± 0.002)					0.50 ± 0.05 (0.020 ± 0.002)					0.80 ± 0.10 (0.031 ± 0.004)				0.80 ± 0.10 (0.031 ± 0.004)			
Thickness	mm (in.)	0.55 MAX. (0.022) MAX.					0.95 MAX. (0.037) MAX.					0.55 MAX. (0.022) MAX.				0.95 MAX. (0.037) MAX.			
WVDC		4	6.3	10	16	25	4	6.3	10	16	25	4	6.3	10	16	4	6.3	10	16
Cap (µF)	0.01																		
	0.033																		
	0.047																		
	0.068																		
	0.10																		
	0.22																		
	0.33																		
	0.47																		
	0.68																		
	1.0																		
	1.5																		
	2.2																		
	3.3																		

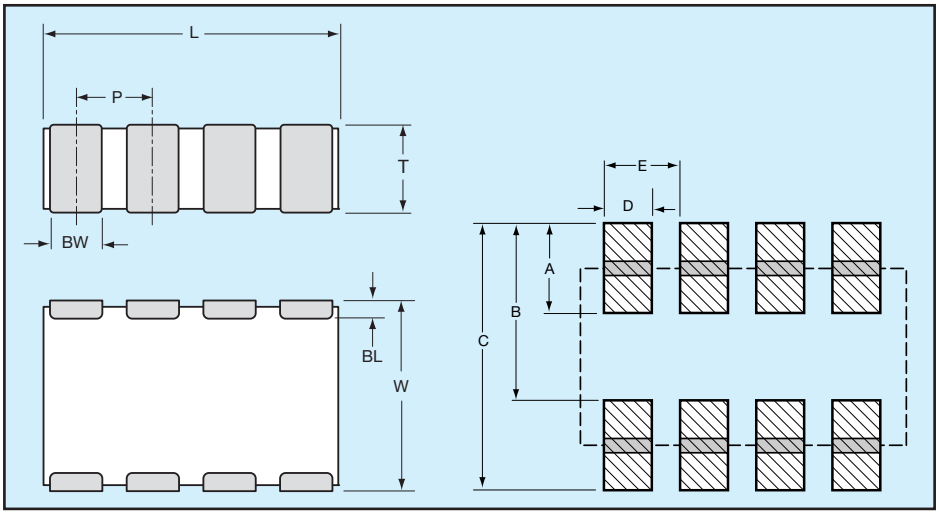
Consult factory for additional requirements

= X7R

= X5R

= X7S

PHYSICAL DIMENSIONS AND PAD LAYOUT



PHYSICAL CHIP DIMENSIONS millimeters (inches)

0612

L	W	BW	BL	P
3.20 ± 0.20 (0.126 ± 0.008)	1.60 ± 0.20 (0.063 ± 0.008)	0.41 ± 0.10 (0.016 ± 0.004)	0.18 $^{+0.25}_{-0.08}$ (0.007 $^{+0.010}_{-0.003}$)	0.80 ± 0.10 (0.031 ± 0.004)

0508

L	W	BW	BL	P
2.03±0.20 (0.080±0.008)	1.27±0.20 (0.050±0.008)	0.254±0.10 (0.010±0.004)	0.18 $^{+0.25}_{-0.08}$ (0.007 $^{+0.010}_{-0.003}$)	0.50 ± 0.05 (0.020 ± 0.002)

PAD LAYOUT DIMENSIONS

0612

A	B	C	D	E
0.89 (0.035)	1.65 (0.065)	2.54 (0.100)	0.46 (0.018)	0.80 (0.031)

0508

A	B	C	D	E
0.64 (0.025)	1.27 (0.050)	1.91 (0.075)	0.28 (0.011)	0.50 (0.020)