Automotive Inductive Load Driver

This MicroIntegration ™ part provides a single component solution to switch inductive loads such as relays, solenoids, and small DC motors without the need of a free—wheeling diode. It accepts logic level inputs, thus allowing it to be driven by a large variety of devices including logic gates, inverters, and microcontrollers.

Features

- Provides Robust Interface between D.C. Relay Coils and Sensitive Logic
- Capable of Driving Relay Coils Rated up to 150 mA at 12 Volts
- Replaces 3 or 4 Discrete Components for Lower Cost
- Internal Zener Eliminates Need for Free-Wheeling Diode
- Meets Load Dump and other Automotive Specs

Typical Applications

- Automotive and Industrial Environment
- Drives Window, Latch, Door, and Antenna Relays

Benefits

- Reduced PCB Space
- Standardized Driver for Wide Range of Relays
- Simplifies Circuit Design and PCB Layout
- Compliance with Automotive Specifications

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MARKING DIAGRAMS





SOT-23 CASE 318 STYLE 21





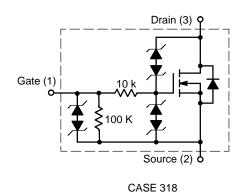


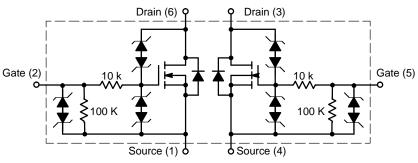
SC-74 CASE 318F STYLE 7

JW6 = Specific Device Code

D = Date Code

INTERNAL CIRCUIT DIAGRAMS





CASE 318F

ORDERING INFORMATION

Device	Package	Shipping
NUD3124LT1	SOT-23	3000/Tape & Reel
NUD3124DMT1	SC-74	3000/Tape & Reel

MAXIMUM RATINGS ($T_J = 25$ °C unless otherwise specified)

Symbol	Rating	Value	Unit
V _{DSS}	Drain-to-Source Voltage - Continuous (T _J = 125°C)	28	V
V_{GSS}	Gate-to-Source Voltage - Continuous (T _J = 125°C)	12	V
I _D	Drain Current – Continuous (T _J = 125°C)	150	mA
E _Z	Single Pulse Drain–to–Source Avalanche Energy (For Relay's Coils/Inductive Loads of 80 Ω or Higher) (T _J Initial = 85°C)	250	mJ
P _{PK}	Peak Power Dissipation, Drain-to-Source (Notes 1 and 2) (T _J Initial = 85°C)	20	W
E _{LD1}	Load Dump Suppressed Pulse, Drain–to–Source (Notes 3 and 4) (Suppressed Waveform: $V_s = 45$ V, $R_{SOURCE} = 0.5 \Omega$, $T = 200$ ms) (For Relay's Coils/Inductive Loads of 80Ω or Higher) (T_J Initial = 85° C)	80	V
E _{LD2}	Inductive Switching Transient 1, Drain–to–Source (Waveform: R_{SOURCE} = 10 Ω , T = 2.0 ms) (For Relay's Coils/Inductive Loads of 80 Ω or Higher) (T _J Initial = 85°C)	100	V
E _{LD3}	Inductive Switching Transient 2, Drain–to–Source (Waveform: R_{SOURCE} = 4.0 Ω , T = 50 μ s) (For Relay's Coils/Inductive Loads of 80 Ω or Higher) (T _J Initial = 85°C)	300	V
Rev-Bat	Reverse Battery, 10 Minutes (Drain–to–Source) (For Relay's Coils/Inductive Loads of 80 Ω or more)	-14	V
Dual-Volt	Dual Voltage Jump Start, 10 Minutes (Drain-to-Source)	28	V
ESD	Human Body Model (HBM) According to EIA/JESD22/A114 Specification	2,000	V

- 1. Nonrepetitive current square pulse 1.0 ms duration. 2. For different square pulse durations, see Figure 2. 3. Nonrepetitive load dump suppressed pulse per Figure 3. 4. For relay's coils/inductive loads higher than 80 Ω , see Figure 4.

THERMAL CHARACTERISTICS

Symbol	Rating	Value	Unit
T _A	Operating Ambient Temperature	-40 to 125	°C
TJ	Maximum Junction Temperature	150	°C
T _{STG}	Storage Temperature Range	-65 to 150	°C
P _D	Total Power Dissipation (Note 5) SOT–23 Derating above 25°C	225 1.8	mW mW/°C
P _D	Total Power Dissipation (Note 5) SC–74 Derating above 25°C	380 1.5	mW mW/°C
$R_{ heta JA}$	Thermal Resistance Junction–to–Ambient (Note 5) SOT–23 SC–74		°C/W

5. Mounted onto minimum pad board.

ELECTRICAL CHARACTERISTICS (T_{.I} = 25°C unless otherwise specified)

ELECTRICAL CHARACTERISTICS (T _J = 25°C unless otherwise specifical Characteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS	- Cy		.,,,	max	O
Drain to Source Sustaining Voltage (I _D = 10 mA)	V _{BRDSS}	28	34	38	V
Drain to Source Leakage Current $ (V_{DS} = 12 \text{ V}, V_{GS} = 0 \text{ V}) \\ (V_{DS} = 12 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125^{\circ}\text{C}) \\ (V_{DS} = 28 \text{ V}, V_{GS} = 0 \text{ V}) \\ (V_{DS} = 28 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125^{\circ}\text{C}) $	I _{DSS}	- - - -	- - - -	0.5 1.0 50 80	μΑ
Gate Body Leakage Current $ (V_{GS} = 3.0 \text{ V}, V_{DS} = 0 \text{ V}) \\ (V_{GS} = 3.0 \text{ V}, V_{DS} = 0 \text{ V}, T_{J} = 125^{\circ}\text{C}) \\ (V_{GS} = 5.0 \text{ V}, V_{DS} = 0 \text{ V}) \\ (V_{GS} = 5.0 \text{ V}, V_{DS} = 0 \text{ V}, T_{J} = 125^{\circ}\text{C}) $	lgss		- - -	60 80 90 110	μΑ
ON CHARACTERISTICS					
Gate Threshold Voltage $ (V_{GS} = V_{DS}, I_D = 1.0 \text{ mA}) $ $ (V_{GS} = V_{DS}, I_D = 1.0 \text{ mA}, T_J = 125^{\circ}\text{C}) $	V _{GS(th)}	1.3 1.3	1.8 -	2.0 2.0	V
Drain to Source On–Resistance (I_D = 150 mA, V_{GS} = 3.0 V) (I_D = 150 mA, V_{GS} = 3.0 V, T_J = 125°C) (I_D = 150 mA, V_{GS} = 5.0 V) (I_D = 150 mA, V_{GS} = 5.0 V, T_J = 125°C)	R _{DS(on)}	- - - -	- - - -	1.4 1.7 0.8 1.1	Ω
Output Continuous Current (V_{DS} = 0.25 V, V_{GS} = 3.0 V) (V_{DS} = 0.25 V, V_{GS} = 3.0 V, T_{J} = 125°C)	I _{DS(on)}	150 140	200 -	-	mA
Forward Transconductance $(V_{DS} = 12 \text{ V}, I_D = 150 \text{ mA})$	9FS	_	500	_	mmho
DYNAMIC CHARACTERISTICS	•	-	•		
Input Capacitance $(V_{DS} = 12 \text{ V}, V_{GS} = 0 \text{ V}, f = 10 \text{ kHz})$	Ciss	-	32	-	pf
Output Capacitance $(V_{DS} = 12 \text{ V}, V_{GS} = 0 \text{ V}, f = 10 \text{ kHz})$	Coss	_	21	-	pf
Transfer Capacitance $(V_{DS} = 12 \text{ V}, V_{GS} = 0 \text{ V}, f = 10 \text{ kHz})$	Crss	-	8.0	-	pf
SWITCHING CHARACTERISTICS					
Propagation Delay Times: High to Low Propagation Delay; Figure 1, $(V_{DS} = 12 \text{ V}, V_{GS} = 3.0 \text{ V})$ Low to High Propagation Delay; Figure 1, $(V_{DS} = 12 \text{ V}, V_{GS} = 3.0 \text{ V})$	^t PHL ^t PLH	- -	890 912	_ _	ns
High to Low Propagation Delay; Figure 1, $(V_{DS} = 12 \text{ V}, V_{GS} = 5.0 \text{ V})$ Low to High Propagation Delay; Figure 1, $(V_{DS} = 12 \text{ V}, V_{GS} = 5.0 \text{ V})$	^t PHL ^t PLH	- -	324 1280	_ _	
Transition Times: Fall Time; Figure 1, $(V_{DS} = 12 \text{ V}, V_{GS} = 3.0 \text{ V})$ Rise Time; Figure 1, $(V_{DS} = 12 \text{ V}, V_{GS} = 3.0 \text{ V})$	t _f t _r	- -	2086 708	_ _	ns
Fall Time; Figure 1, (V_{DS} = 12 V, V_{GS} = 5.0 V) Rise Time; Figure 1, (V_{DS} = 12 V, V_{GS} = 5.0 V)	t _f t _r	- -	556 725	_ _	

TYPICAL PERFORMANCE CURVES

 $(T_J = 25^{\circ}C \text{ unless otherwise noted})$

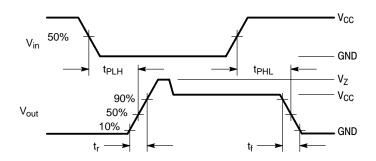


Figure 1. Switching Waveforms

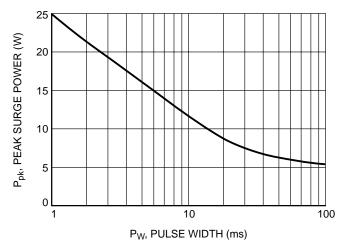


Figure 2. Maximum Non-repetitive Surge Power versus Pulse Width

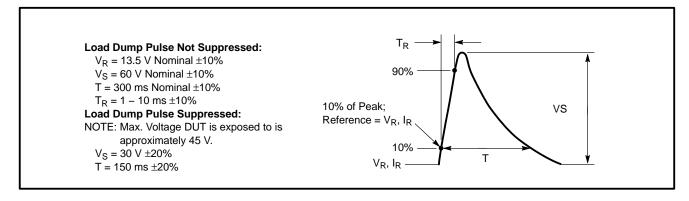


Figure 3. Load Dump Waveform Definition

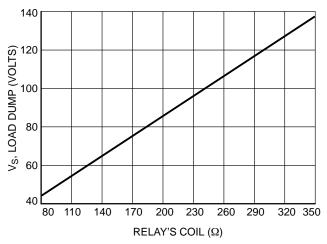


Figure 4. Load Dump Capability versus Relay's Coil dc Resistance

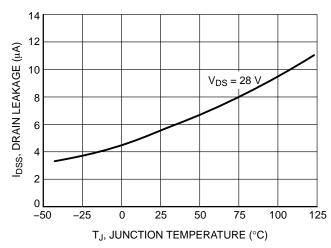


Figure 5. Drain-to-Source Leakage versus Junction Temperature

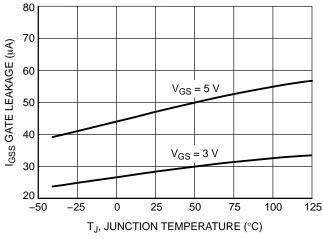


Figure 6. Gate-to-Source Leakage versus Junction Temperature

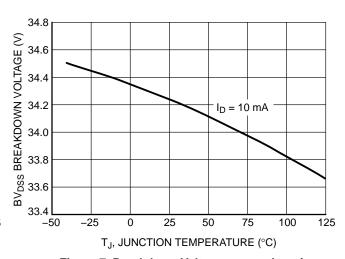


Figure 7. Breakdown Voltage versus Junction Temperature

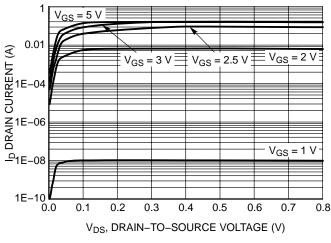


Figure 8. Output Characteristics

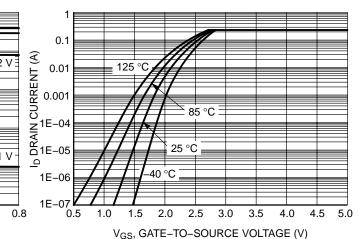


Figure 9. Transfer Function

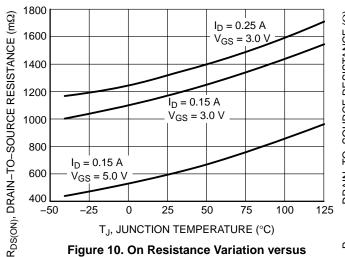


Figure 10. On Resistance Variation versus **Junction Temperature**

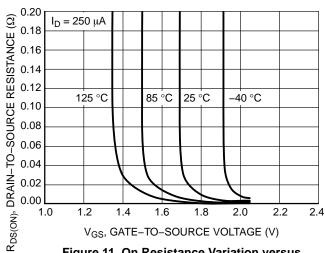


Figure 11. On Resistance Variation versus Gate-to-Source Voltage

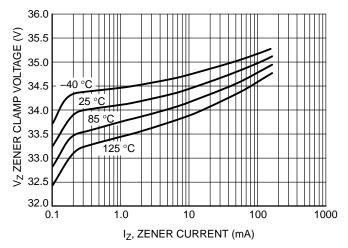


Figure 12. Zener Clamp Voltage versus Zener Current

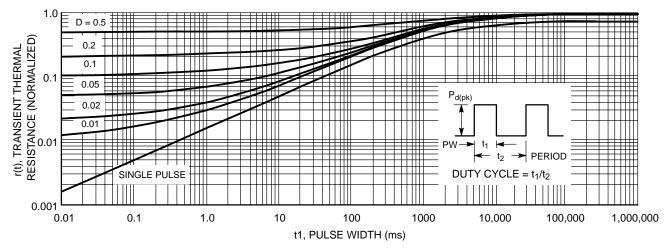


Figure 13. Transient Thermal Response for NUD3124LT1

APPLICATIONS INFORMATION

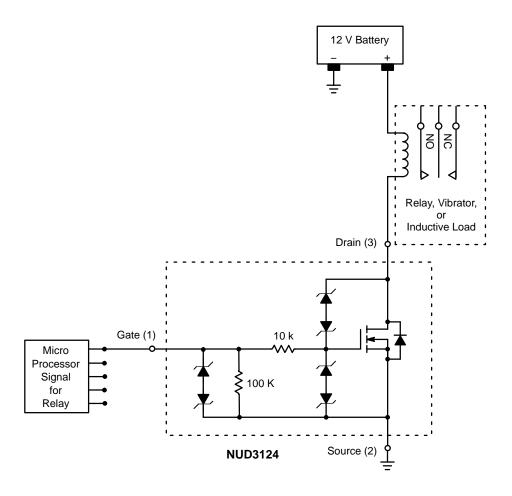
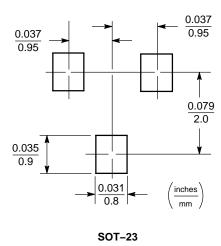


Figure 14. Applications Diagram

INFORMATION FOR USING THE SOT-23 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT-23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A . Using the values provided on the data sheet for the SOT–23 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150^{\circ}C - 25^{\circ}C}{556^{\circ}C/W} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT-23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT-23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad[®]. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

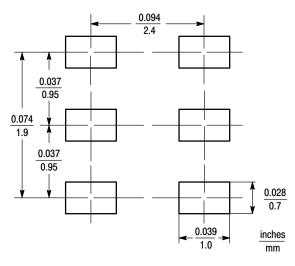
- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.
- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient should be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes.
 Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling
- * Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

INFORMATION FOR USING THE SC-74 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection

interface between the board and the package. With the correct pad geometry, the packages will self-align when subjected to a solder reflow process.



SC-74

SC-74 POWER DISSIPATION

The power dissipation of the SC-74 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A . Using the values provided on the data sheet for the SC-74 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta, I\Delta}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C,

one can calculate the power dissipation of the device which in this case is 380 milliwatts.

$$P_D = \frac{150^{\circ}C - 25^{\circ}C}{329^{\circ}C/W} = 380 \text{ milliwatts}$$

The 329°C/W for the SC-74 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 380 milliwatts. There are other alternatives to achieving higher power dissipation from the SC-74 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad[®]. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the

SC-59, SC-74, SC-70/SOT-323, SOD-123, SOT-23, SOT-143, SOT-223, SO-8, SO-14, SO-16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration.

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.

- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient should be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes.
 Gradual cooling should be used since the use of forced cooling will increase the temperature gradient and will result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.
- * Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 15 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows

temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

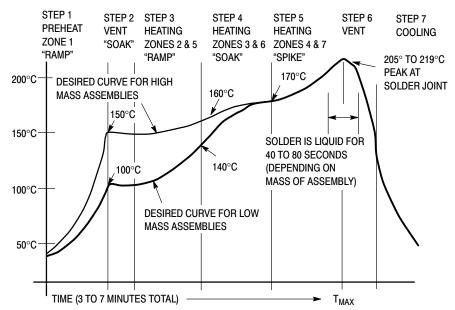
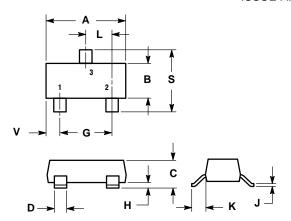


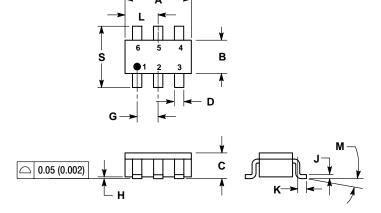
Figure 15. Typical Solder Heating Profile

PACKAGE DIMENSIONS

SOT-23 (TO-236) CASE 318-09 **ISSUE AH**



SC-74 CASE 318F-04 **ISSUE J**



NOTES:

- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: INCH.

 3. MAXIUMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE
- MATERIAL.
 4. 318-01, -02, AND -06 OBSOLETE, NEW STANDARD 318-09.

	INCHES		MILLIN	ETERS
DIM	MIN	MAX	MIN MAX	
Α	0.1102	0.1197	2.80	3.04
В	0.0472	0.0551	1.20	1.40
С	0.0385	0.0498	0.99	1.26
D	0.0140	0.0200	0.36	0.50
G	0.0670	0.0826	1.70	2.10
Н	0.0040	0.0098	0.10	0.25
J	0.0034	0.0070	0.085	0.177
K	0.0180	0.0236	0.45	0.60
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.0984	2.10	2.50
٧	0.0177	0.0236	0.45	0.60

STYLE 21: PIN 1. GATE

SOURCE 3. DRAIN

- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
 4. 318F-01, -02, -03 OBSOLETE. NEW STANDARD 318F-04.

	INCHES		MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.1142	0.1220	2.90	3.10
В	0.0512	0.0669	1.30	1.70
С	0.0354	0.0433	0.90	1.10
D	0.0098	0.0197	0.25	0.50
G	0.0335	0.0413	0.85	1.05
Н	0.0005	0.0040	0.013	0.100
J	0.0040	0.0102	0.10	0.26
K	0.0079	0.0236	0.20	0.60
L	0.0493	0.0649	1.25	1.65
M	0 °	10°	0 °	10°
S	0.0985	0.1181	2.50	3.00

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