## **Power MOSFET**

## 30 V, 2.5 A, Single N-Channel, SOT-23

## **Features**

- Leading Planar Technology for Low Gate Charge / Fast Switching
- 4.5 V Rated for Low Voltage Gate Drive
- SOT–23 Surface Mount for Small Footprint (3 x 3 mm)
- Pb-Free Package for Green Manufacturing

## **Applications**

- DC-DC Conversion
- Load/Power Switch for Portables
- Load/Power Switch for Computing

## MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		V <sub>DSS</sub>	30	V	
Gate-to-Source Voltage			$V_{GS}$	±20	V
Continuous Drain	Steady $T_A = 25^{\circ}C$		I <sub>D</sub>	2.0	Α
Current (Note 1)	State	T <sub>A</sub> = 85°C		1.5	
	t ≤ 10 s	T <sub>A</sub> = 25°C		2.5	
Power Dissipation (Note 1)	Steady State	T <sub>A</sub> = 25°C	P <sub>D</sub>	0.73	W
Continuous Drain	Steady	T <sub>A</sub> = 25°C	I <sub>D</sub>	1.5	Α
Current (Note 2)	State T <sub>A</sub>	T <sub>A</sub> = 85°C		1.1	
Power Dissipation (Note 2)		T <sub>A</sub> = 25°C	P <sub>D</sub>	0.42	W
Pulsed Drain Current	tp = 10 μs		I <sub>DM</sub>	6.0	Α
ESD Capability (Note 3)	C = 100 pF, RS = 1500 Ω		ESD	125	V
Operating Junction and Storage Temperature		T <sub>J</sub> , T <sub>STG</sub>	–55 to 150	°C	
Source Current (Body Diode)		IS	2.0	Α	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		TL	260	°C	

## THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	170	°C/W
Junction-to-Ambient - t < 10 s (Note 1)	$R_{\theta JA}$	100	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	300	

- 1. Surface-mounted on FR4 board using 1 in sq pad size.
- 2. Surface—mounted on FR4 board using the minimum recommended pad size.
- 3. ESD Rating Information: HBM Class 0.

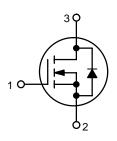


## ON Semiconductor®

## http://onsemi.com

V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> TYP	I <sub>D</sub> MAX
30 V	85 mΩ @ 10 V	2.5 A
	105 mΩ @ 4.5 V	2.071

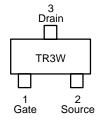
## **N-Channel**



## MARKING DIAGRAM/ PIN ASSIGNMENT



SOT-23 CASE 318 STYLE 21



TR3 = Specific Device Code W = Work Week

## **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NTR4503NT1	SOT-23	3000/Tape & Reel
NTR4503NT1G	SOT-23 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# **ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Units
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30	36		V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 24 V			1.0	μΑ
		V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 24 V, T <sub>J</sub> = 125°C			10	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			±100	nA
ON CHARACTERISTICS (Note 4)						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_D = 250 \mu A$	1.0	1.75	3.0	V
Drain-to-Source On-Resistance	R <sub>DS(on)</sub>	$V_{GS} = 10 \text{ V}, I_D = 2.5 \text{ A}$		85	110	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 2.0 A		105	140	
Forward Transconductance	9FS	$V_{DS} = 4.5 \text{ V}, I_D = 2.5 \text{ A}$		5.3		S
CHARGES AND CAPACITANCES	•					
Input Capacitance	C <sub>ISS</sub>			135		pF
Output Capacitance	C <sub>OSS</sub>	$V_{GS} = 0 \text{ V, f} = 1.0 \text{ MHz,}$ $V_{DS} = 15 \text{ V}$		52		
Reverse Transfer Capacitance	C <sub>RSS</sub>	VDS = 13 V		15		1
Input Capacitance	C <sub>ISS</sub>			130	250	pF
Output Capacitance	C <sub>OSS</sub>	$V_{GS} = 0 \text{ V, f} = 1.0 \text{ MHz,}$ $V_{DS} = 24 \text{ V}$		42	75	
Reverse Transfer Capacitance	C <sub>RSS</sub>	VDS - 24 V		13	25	
Total Gate Charge	Q <sub>G(TOT)</sub>			3.6	7.0	nC
Threshold Gate Charge	Q <sub>G(TH)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 15 V,		0.3		
Gate-to-Source Charge	Q <sub>GS</sub>	I <sub>D</sub> = 2.5 A		0.6		
Gate-to-Drain Charge	$Q_{GD}$			0.7		
Total Gate Charge	Q <sub>G(TOT)</sub>			1.9		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>	$V_{GS} = 4.5 \text{ V}, V_{DS} = 24 \text{ V},$		0.3		
Gate-to-Source Charge	Q <sub>GS</sub>	$V_{GS} = 4.5 \text{ V}, V_{DS} = 24 \text{ V},$ $I_{D} = 2.5 \text{ A}$		0.6		
Gate-to-Drain Charge	$Q_{GD}$			0.9		
SWITCHING CHARACTERISTICS (Note	e 5)					
Turn-On Delay Time	t <sub>d(ON)</sub>			5.8	12	ns
Rise Time	t <sub>r</sub>	$V_{GS} = 10 \text{ V}, V_{DD} = 15 \text{ V},$		5.8	10	
Turn-Off Delay Time	t <sub>d(OFF)</sub>	$V_{GS} = 10 \text{ V}, V_{DD} = 15 \text{ V},$ $I_{D} = 1 \text{ A}, R_{G} = 6 \Omega$		14	25	
Fall Time	t <sub>f</sub>			1.6	5.0	
Turn-On Delay Time	t <sub>d(ON)</sub>			4.8		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 10 V, V <sub>DD</sub> = 24 V,		6.7		
Turn-Off Delay Time	t <sub>d(OFF)</sub>	$I_D = 2.5 \text{ A}, R_G = 2.5 \Omega$		13.6		
Fall Time	t <sub>f</sub>			1.8		1
DRAIN-SOURCE DIODE CHARACTER	ISTICS			-	-	-
Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0 \text{ V}, I_S = 2.0 \text{ A}$		0.85	1.2	V
Reverse Recovery Time	t <sub>RR</sub>	$V_{GS} = 0 \text{ V, } I_{S} = 2.0 \text{ A,}$		9.2		ns
Reverse Recovery Charge	Q <sub>RR</sub>	$dl_{S}/dt = 100 A/\mu s$		4.0		nC

<sup>4.</sup> Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

## **TYPICAL PERFORMANCE CURVES**

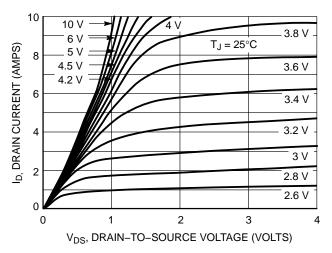
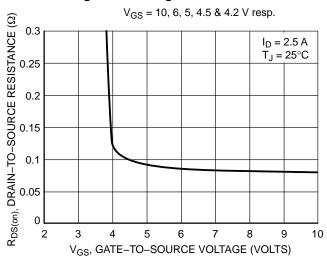


Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics



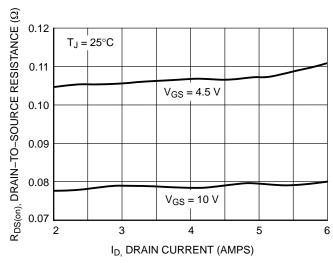
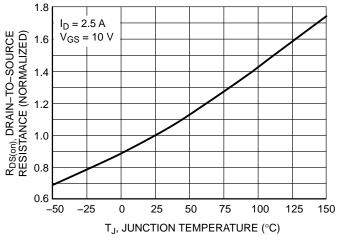


Figure 3. On-Resistance vs. Gate-to-Source Voltage

Figure 4. On–Resistance vs. Drain Current and Gate Voltage



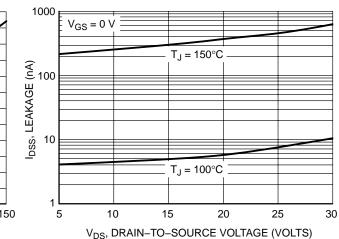
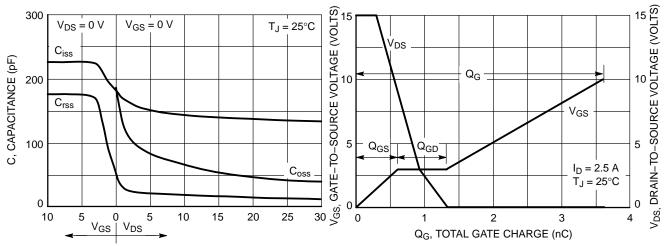


Figure 5. On–Resistance Variation with Temperature

Figure 6. Drain-to-Source Leakage Current vs. Voltage

## **TYPICAL PERFORMANCE CURVES**



GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 7. Capacitance Variation

Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

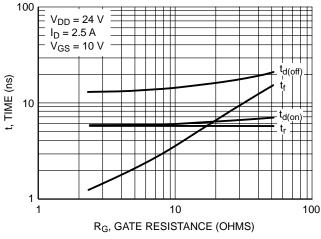


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

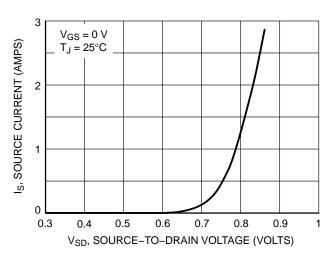
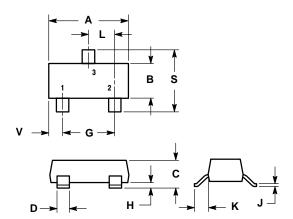


Figure 10. Diode Forward Voltage vs. Current

## **PACKAGE DIMENSIONS**

SOT-23 CASE 318-09 **ISSUE AH** 



- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. MAXIUMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
  4. 318-01, -02, AND -06 OBSOLETE, NEW STANDARD 318-09.

	INCHES		MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.1102	0.1197	2.80	3.04	
В	0.0472	0.0551	1.20	1.40	
C	0.0385	0.0498	0.99	1.26	
D	0.0140	0.0200	0.36	0.50	
G	0.0670	0.0826	1.70	2.10	
Н	0.0040	0.0098	0.10	0.25	
7	0.0034	0.0070	0.085	0.177	
K	0.0180	0.0236	0.45	0.60	
L	0.0350	0.0401	0.89	1.02	
S	0.0830	0.0984	2.10	2.50	
٧	0.0177	0.0236	0.45	0.60	

- STYLE 21:
  PIN 1. GATE
  2. SOURCE
  3. DRAIN

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