

NTR4502P

Power MOSFET

–30 V, –1.95 A, Single, P–Channel,
SOT–23

Features

- Leading Planar Technology for Low Gate Charge / Fast Switching
- Low $R_{DS(ON)}$ for Low Conduction Losses
- SOT–23 Surface Mount for Small Footprint (3 X 3 mm)
- Pb–Free Package May be Available. The G–Suffix Denotes a Pb–Free Lead Finish

Applications

- DC to DC Conversion
- Load/Power Switch for Portables and Computing
- Motherboard, Notebooks, Camcorders, Digital Camera's, etc.
- Battery Charging Circuits

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain–to–Source Voltage			V_{DSS}	–30	V
Gate–to–Source Voltage			V_{GS}	–20	V
Drain Current (Note 1)	t < 10 s	$T_A = 25^{\circ}\text{C}$	I_D	–1.95	A
		$T_A = 70^{\circ}\text{C}$		–1.56	
Power Dissipation (Note 1)	t < 10 s		P_D	1.25	W
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	–1.13	A
		$T_A = 70^{\circ}\text{C}$		–0.90	
Power Dissipation (Note 1)	Steady State		P_D	0.4	W
Pulsed Drain Current	$t_p = 10\text{ }\mu\text{s}$		I_{DM}	–6.8	A
Operating Junction and Storage Temperature			T_J , T_{STG}	–55 to 150	$^{\circ}\text{C}$
Source Current (Body Diode)			I_S	–1.25	A
Lead Temperature for Soldering Purposes (1/8 in from case for 10 s)			T_L	260	$^{\circ}\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction–to–Ambient – Steady State (Note 1)	$R_{\theta JA}$	300	$^\circ\text{C}/\text{W}$
Junction–to–Ambient – $t = 10$ s (Note 1)	$R_{\theta JA}$	100	

1. Surface–mounted on FR4 board using 1 in sq. pad size (Cu area = 1.127 in sq. [1 oz] including traces).

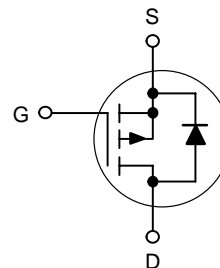


ON Semiconductor®

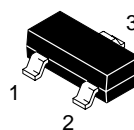
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D Max (Note 1)
–30 V	155 m Ω @ –10 V	–1.95 A
	240 m Ω @ –4.5 V	

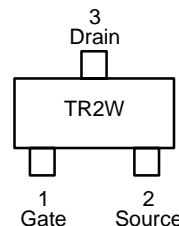
P–Channel MOSFET



MARKING DIAGRAM/ PIN ASSIGNMENT



SOT–23
CASE 318
Style 21



TR2 = Specific Device Code
W = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NTR4502PT1	SOT–23	3000 / Tape & Reel
NTR4502PT3	SOT–23	10000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTR4502P

Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = -30\text{ V}$	$T_J = 25^\circ\text{C}$		-1	μA
			$T_J = 55^\circ\text{C}$		-10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\text{ }\mu\text{A}$	-1.0		-3.0	V
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -1.95\text{ A}$		155	200	$\text{m}\Omega$
		$V_{GS} = -4.5\text{ V}, I_D = -1.5\text{ A}$		240	350	
Forward Transconductance	g_{FS}	$V_{DS} = -10\text{ V}, I_D = -1.25\text{ A}$		3		S

CHARGES AND CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = -15\text{ V}$		200		pF
Output Capacitance	C_{OSS}			80		
Reverse Transfer Capacitance	C_{RSS}			50		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -10\text{ V}, V_{DS} = -15\text{ V}; I_D = -1.95\text{ A}$		6	10	nC
Threshold Gate Charge	$Q_{G(TH)}$			0.3		
Gate-to-Source Charge	Q_{GS}			1		
Gate-to-Drain Charge	Q_{GD}			1.7		

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -10\text{ V}, V_{DD} = -15\text{ V}, I_D = -1.95\text{ A}, R_G = 6\text{ }\Omega$		5.2	10	ns
Rise Time	t_r			12	20	
Turn-Off Delay Time	$t_{d(OFF)}$			19	35	
Fall Time	t_f			17.5	30	

DRAIN-SOURCE DIODE CHARACTERISTICS (Note 3)

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = -1.25\text{ A}$		-0.8	-1.2	V
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_{SD}/dt = 100\text{ A}/\mu\text{s}, I_S = -1.25\text{ A}$		23		ns

- Surface-mounted on FR4 board using 1 in sq. pad size (Cu area = 1.127 in sq. [1 oz] including traces).
- Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Switching characteristics are independent of operating junction temperatures.

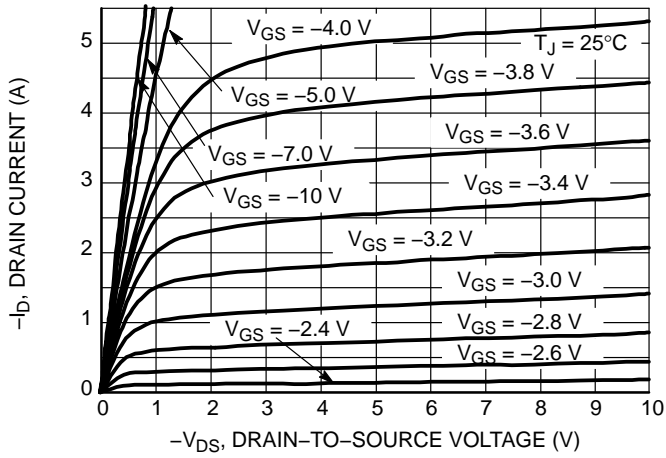


Figure 1. On-Region Characteristics

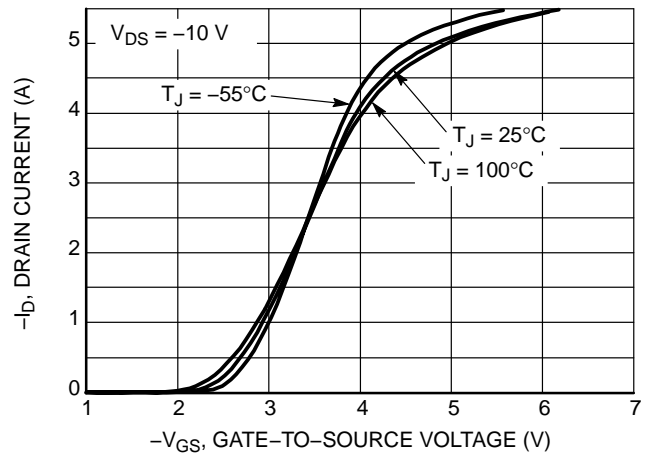


Figure 2. Transfer Characteristics

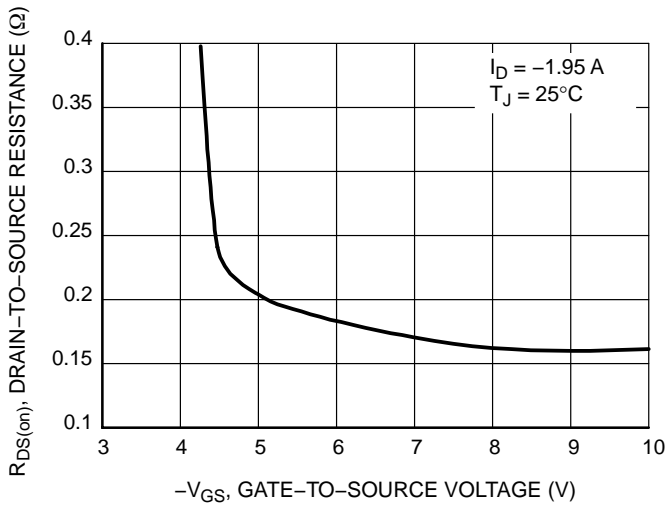


Figure 3. On-Resistance versus Gate-to-Source Voltage

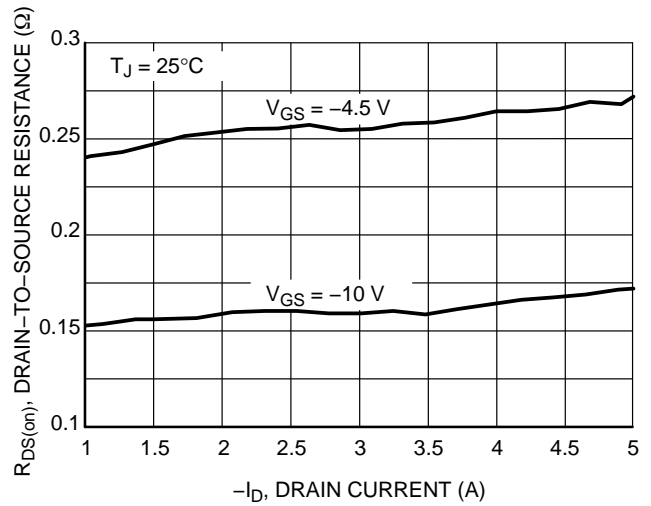


Figure 4. On-Resistance versus Drain Current and Gate Voltage

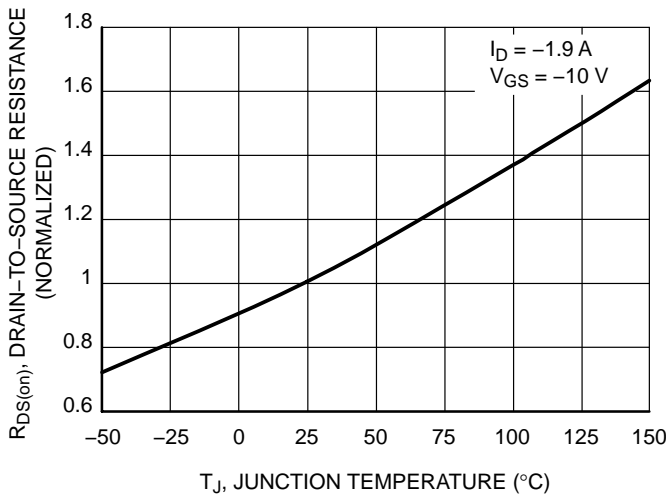


Figure 5. On-Resistance Variation with Temperature

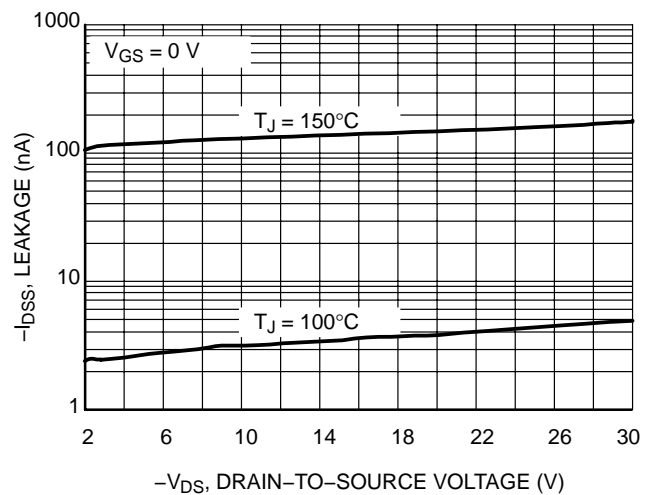


Figure 6. Drain-to-Source Leakage Current versus Voltage

NTR4502P

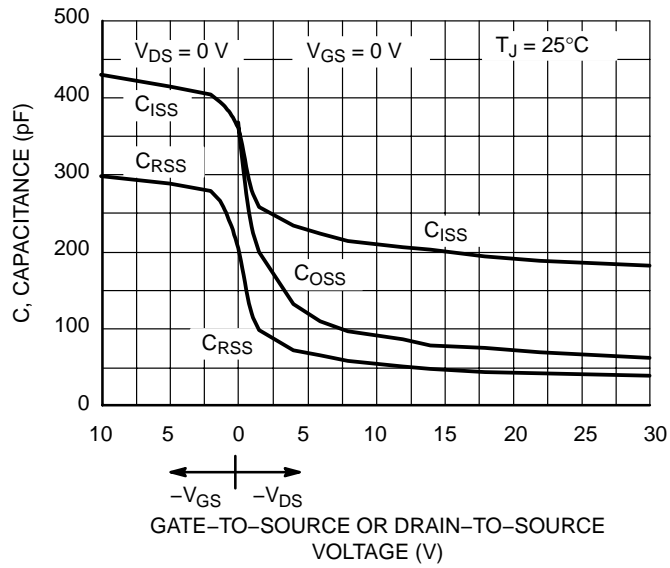


Figure 7. Capacitance Variation

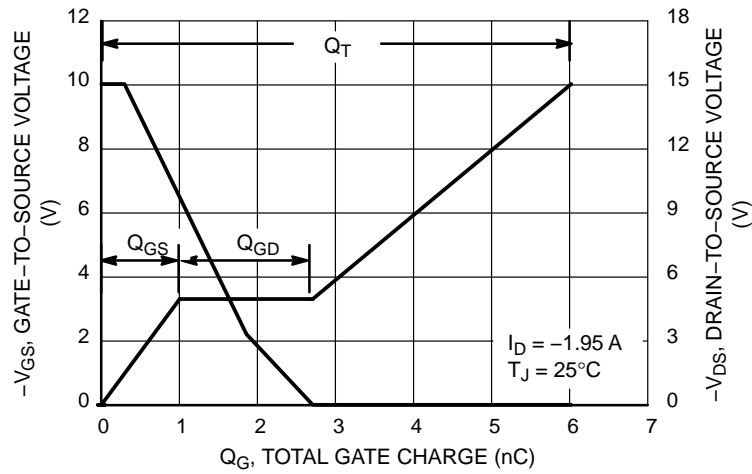


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

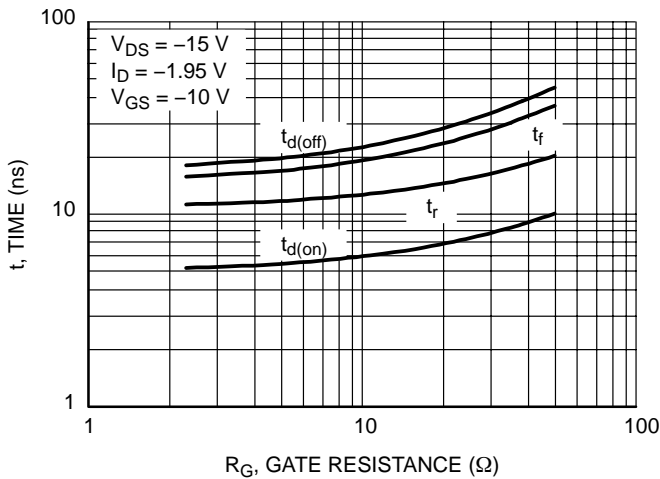


Figure 9. Resistive Switching Time Variation versus Gate Resistance

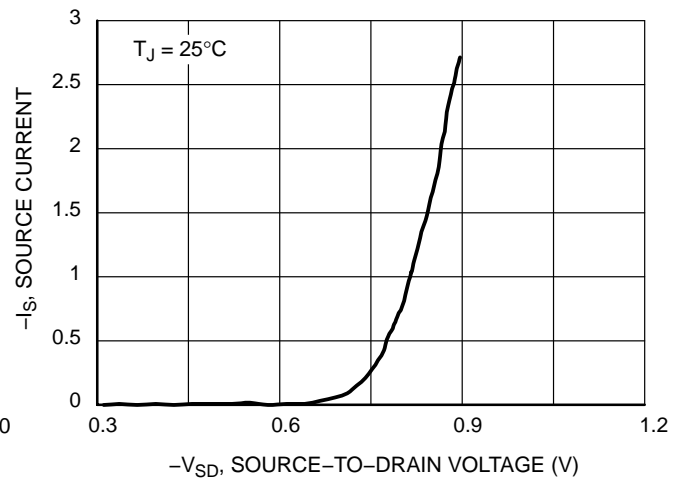
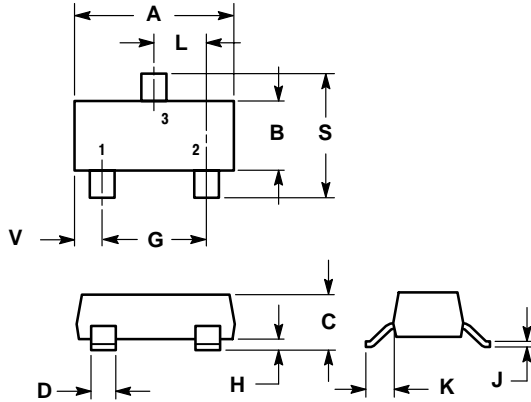


Figure 10. Diode Forward Voltage versus Current

PACKAGE DIMENSIONS

SOT-23
CASE 318-09
ISSUE AH



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318-01, -02, AND -06 OBSOLETE, NEW STANDARD 318-09.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0385	0.0498	0.99	1.26
D	0.0140	0.0200	0.36	0.50
G	0.0670	0.0826	1.70	2.10
H	0.0040	0.0098	0.10	0.25
J	0.0034	0.0070	0.085	0.177
K	0.0180	0.0236	0.45	0.60
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.0984	2.10	2.50
V	0.0177	0.0236	0.45	0.60

STYLE 21:

- PIN 1. GATE
2. SOURCE
3. DRAIN

SOLDERING FOOTPRINT*

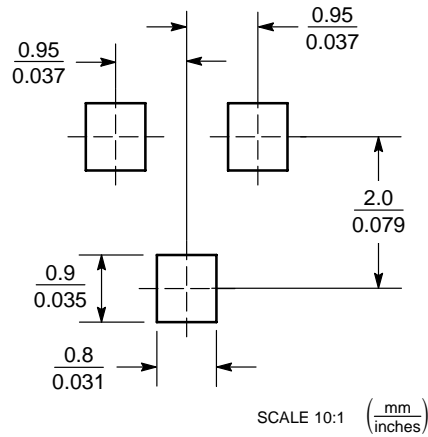



Figure 11. SOT-23

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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