

NTR4501N

Power MOSFET

20 V, 3.2 A, Single N-Channel, SOT-23

Features

- Leading Planar Technology for Low Gate Charge / Fast Switching
- 2.5 V Rated for Low Voltage Gate Drive
- SOT-23 Surface Mount for Small Footprint
- Pb-Free Package May be Available. The G-Suffix Denotes a Pb-Free Lead Finish

Applications

- Load/Power Switch for Portables
- Load/Power Switch for Computing
- DC to DC Conversion

Maximum Ratings ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	20	V
Gate-to-Source Voltage			V_{GS}	± 12	V
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	3.2	A
		$T_A = 85^{\circ}\text{C}$		2.4	A
Steady State Power Dissipation (Note 1)	Steady State		P_D	1.25	W
Pulsed Drain Current	$t_p = 10\text{ }\mu\text{s}$		I_{DM}	10.0	A
Operating Junction and Storage Temperature			T_J, T_{STG}	-55 to 150	$^{\circ}\text{C}$
Continuous Source Current (Body Diode)			I_S	1.6	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^{\circ}\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Max	Unit
Junction-to-Ambient (Note 1)	$R_{\theta JA}$	100	$^\circ\text{C/W}$
Junction-to-Ambient (Note 2)	$R_{\theta JA}$	300	

1. Surface-mounted on FR4 board using 1 in sq. pad size (Cu area = 1.127 in sq. [1 oz] including traces).
2. Surface-mounted on FR4 board using the minimum recommended pad size.

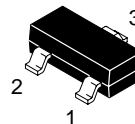
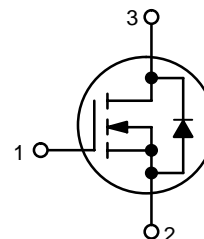


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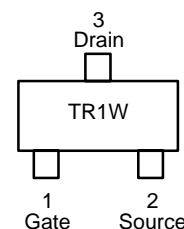
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX (Note 1)
20 V	70 m Ω @ 4.5 V	3.6 A
	85 m Ω @ 2.5 V	3.1 A

N-Channel



**SOT-23
CASE 318
Style 21**

MARKING DIAGRAM/ PIN ASSIGNMENT



TR1 = Specific Device Code
W = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NTR4501NT1	SOT-23	3000 / Tape & Reel
NTR4501NT3	SOT-23	10000 / Tape & Reel
NTR4501NT1G	SOT-23 Pb-Free	3000 / Tape & Reel
NTR4501NT3G	SOT-23 Pb-Free	10000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTR4501N

Electrical Characteristics (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3)	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	20	24.5		V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			22		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, T _J = 25°C			1.5	μA
		V _{DS} = 16 V, T _J = 85°C			10	μA
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±12 V			±100	nA

ON CHARACTERISTICS

Gate Threshold Voltage (Note 3)	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	0.65			V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J			-2.3		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 3.6 A		70	80	mΩ
		V _{GS} = 2.5 V, I _D = 3.1 A		85	105	
Forward Transconductance	g _{FS}	V _{DS} = 5.0 V, I _D = 3.6 A		9		S

CHARGES AND CAPACITANCES

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 10 V		200		pF
Output Capacitance	C _{OSS}			80		
Reverse Transfer Capacitance	C _{RSS}			50		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 10 V, I _D = 3.6 A		2.4	6.0	nC
Gate-to-Source Gate Charge	Q _{GS}			0.5		
Gate-to-Drain Charge	Q _{GD}			0.6		

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t _{d(on)}	V _{GS} = 4.5 V, V _{DS} = 10 V, I _D = 3.6 A, R _G = 6.0 Ω		6.5		ns
Rise Time	t _r			12		
Turn-Off Delay Time	t _{d(OFF)}			12		
Fall Time	t _f			3		

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _{SD} = 1.6 A		0.8	1.2	V
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 1.6 A		7.1		ns
Charge Time	t _a			5		
Discharge Time	t _b			1.9		
Reverse Recovery Charge	Q _{RR}			3.0		nC

3. Pulse Test: Pulse width ≤ 300 μs, duty cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

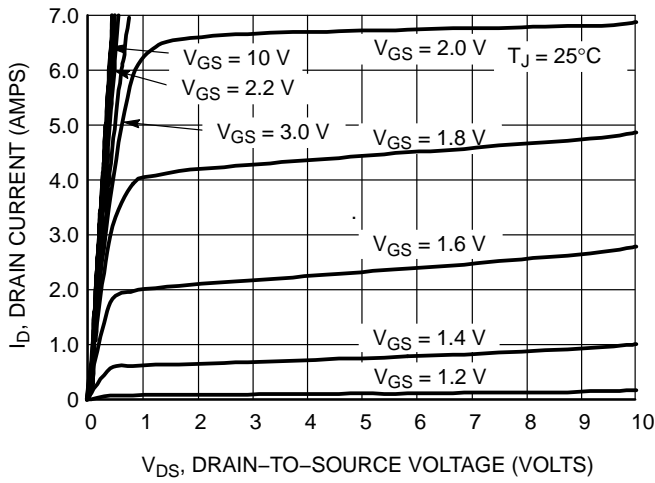


Figure 1. On-Region Characteristics

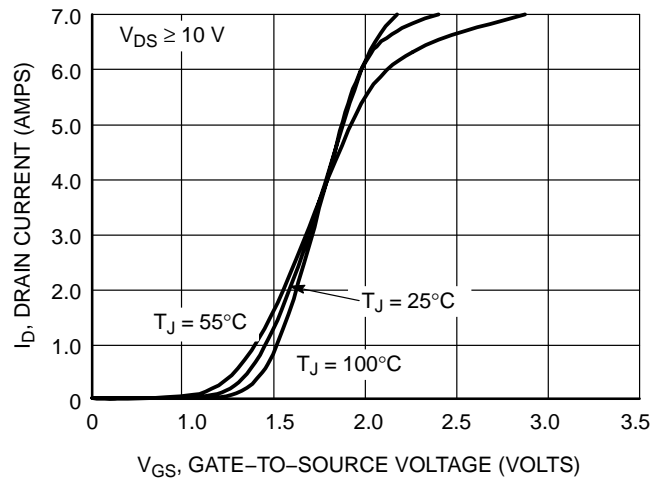


Figure 2. Transfer Characteristics

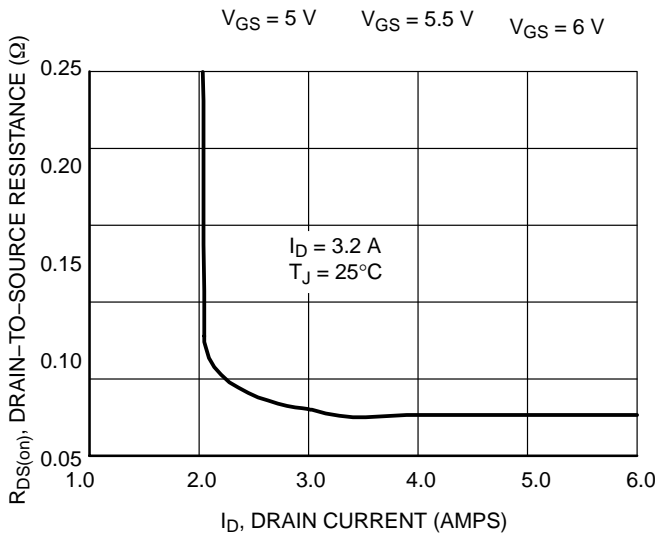


Figure 3. On-Resistance versus Gate-to-Source Voltage

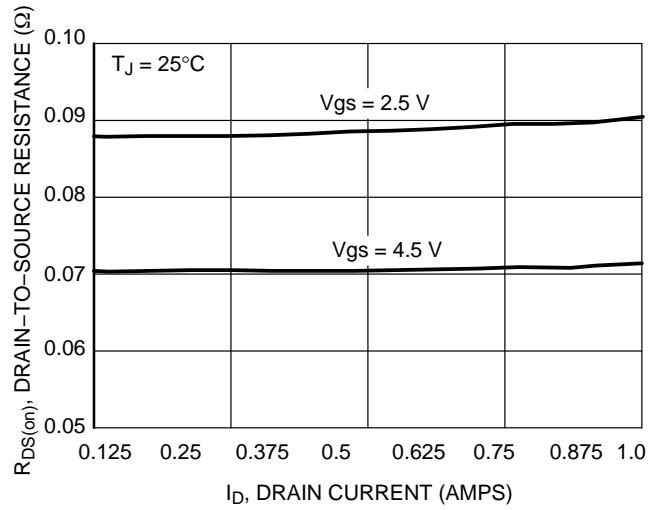


Figure 4. On-Resistance versus Drain Current and Gate Voltage

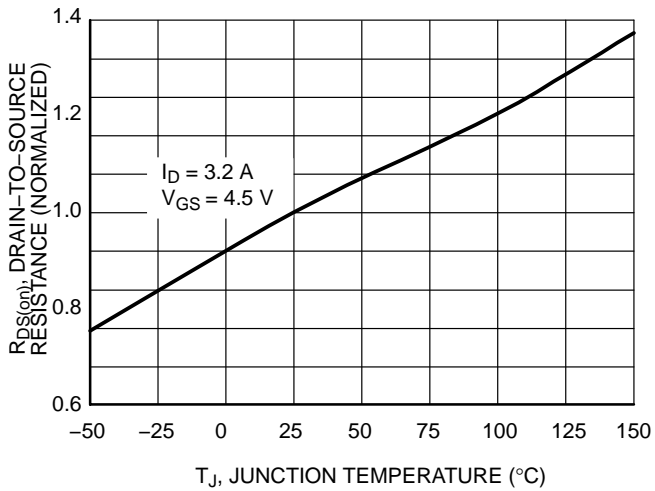


Figure 5. On-Resistance Variation with Temperature

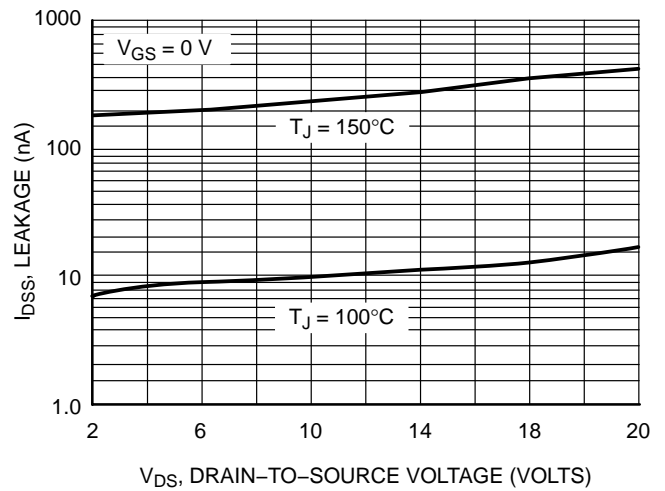


Figure 6. Drain-to-Source Leakage Current versus Voltage

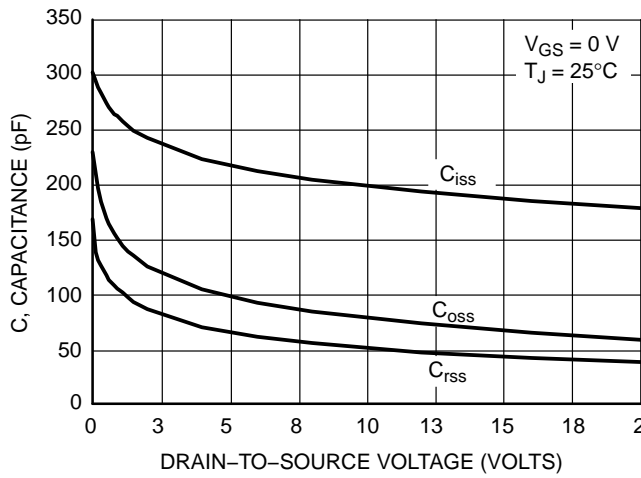


Figure 7. Capacitance Variation

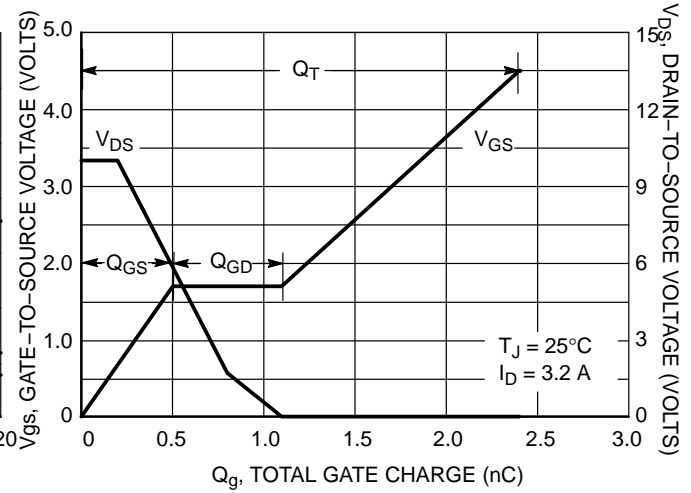


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Gate Charge

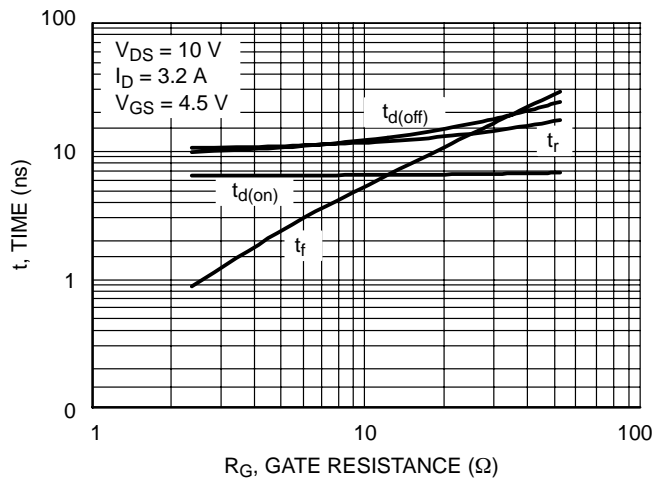


Figure 9. Resistive Switching Time Variation versus Gate Resistance

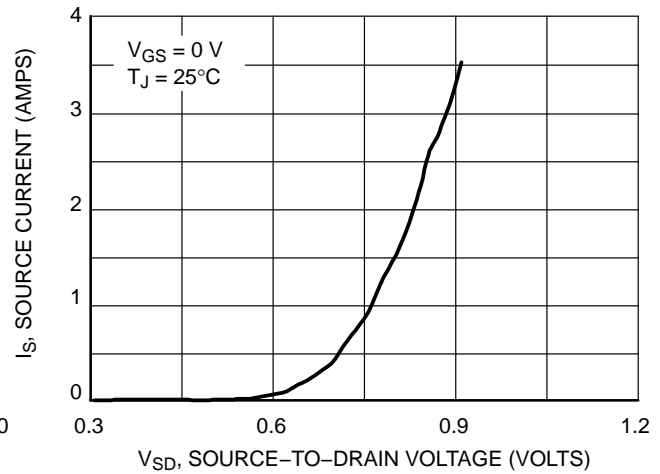
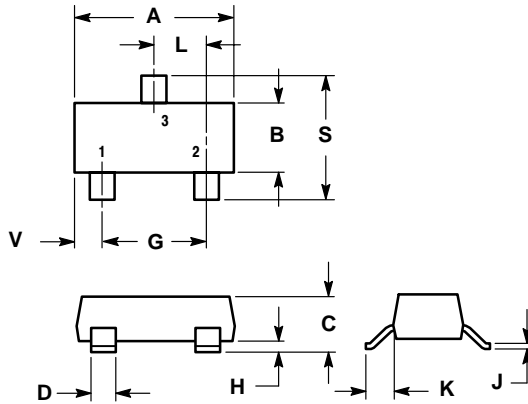


Figure 10. Diode Forward Voltage versus Current

NTR4501N

PACKAGE DIMENSIONS

SOT-23
CASE 318-09
ISSUE AH




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318-01, -02, AND -06 OBSOLETE, NEW STANDARD 318-09.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0385	0.0498	0.99	1.26
D	0.0140	0.0200	0.36	0.50
G	0.0670	0.0826	1.70	2.10
H	0.0040	0.0098	0.10	0.25
J	0.0034	0.0070	0.085	0.177
K	0.0180	0.0236	0.45	0.60
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.0984	2.10	2.50
V	0.0177	0.0236	0.45	0.60

STYLE 21:

- PIN 1. GATE
2. SOURCE
3. DRAIN

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