

NTHS2101P

8.0 V, P-Channel Power MOSFET ChipFET™ Single Package

Features

- Offers an Ultra Low $R_{DS(on)}$ Solution in the ChipFET Package
- Miniature ChipFET Package 40% Smaller Footprint than TSOP-6 making it an Ideal Device for Applications where Board Space is at a Premium
- Low Profile (<1.1 mm) Allows it to Fit Easily into Extremely Thin Environments such as Portable Electronics
- Designed to Provide Low $R_{DS(on)}$ at Gate Voltage as Low as 1.8 V, the Operating Voltage used in many Logic ICs in Portable Electronics
- Simplifies Circuit Design since Additional Boost Circuits for Gate Voltages are not Required
- Operated at Standard Logic Level Gate Drive, Facilitating Future Migration to Lower Levels using the same Basic Topology

Applications

- Optimized for Battery and Load Management Applications in Portable Equipment such as MP3 Players, Cell Phones, Digital Cameras, Personal Digital Assistant and other Portable Applications
- Charge Control in Battery Chargers
- Buck and Boost Converters

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	-8.0	V_{dc}
Gate-to-Source Voltage – Continuous	V_{GS}	± 8.0	V_{dc}
Drain Current – Continuous – 5 seconds	I_D	-5.4	A
	I_D	-7.5	A
Total Power Dissipation Continuous @ $T_A = 25^\circ\text{C}$ (5 sec) @ $T_A = 25^\circ\text{C}$ Continuous @ 85°C (5 sec) @ 85°C	P_D	1.3	W
		2.5	
		0.7	
		1.3	
Continuous Source Current	I_S	-1.1	A
Thermal Resistance (Note 1) Junction-to-Ambient, 5 sec Junction-to-Ambient, Continuous	$R_{\theta JA}$	50	$^\circ\text{C/W}$
	$R_{\theta JA}$	95	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	$^\circ\text{C}$

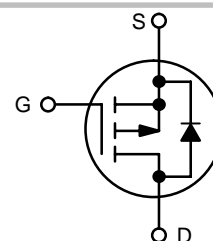
1. When surface mounted to a 1" x 1" FR4 board.



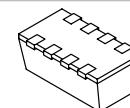
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$V_{(BR)DSS}$	Ultra Low $R_{DS(on)}$ TYP	I_D MAX
8.0 V	19 m Ω @ -4.5 VGS	5.4 A
	25 m Ω @ -2.5 VGS	
	34 m Ω @ -1.8 VGS	

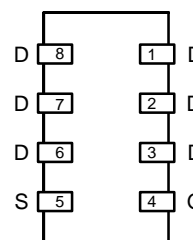


P-Channel MOSFET



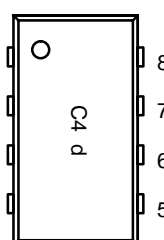
ChipFET
CASE 1206A
STYLE 1

PIN CONNECTIONS



C4 = Specific Device Code
d = Date Code

MARKING DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping†
NTHS2101PT1	ChipFET	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTHS2101P

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 2) Temperature Coefficient (Positive)	$V_{(Br)DSS}$	$V_{GS} = 0\text{ V}_{dc}, I_D = -250\text{ }\mu\text{A}_{dc}$	-8.0	-	-	V_{dc}
Gate-Body Leakage Current Zero	I_{GSS}	$V_{DS} = 0\text{ V}_{dc}, V_{GS} = \pm 8.0\text{ V}_{dc}$	-	-	± 100	nA_{dc}
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -6.4\text{ V}_{dc}, V_{GS} = 0\text{ V}_{dc}$ $V_{DS} = -6.4\text{ V}_{dc}, V_{GS} = 0\text{ V}_{dc},$ $T_J = 85^\circ\text{C}$	-	-	-1.0 -5.0	μA_{dc}

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}_{dc}$	-0.45	-	-1.5	V_{dc}
Static Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}_{dc}, I_D = -5.4\text{ A}_{dc}$ $V_{GS} = -2.5\text{ V}_{dc}, I_D = -4.5\text{ A}_{dc}$ $V_{GS} = -1.8\text{ V}_{dc}, I_D = -2.0\text{ A}_{dc}$	- - -	19 25 34	25 36 48	$\text{m}\Omega$
Forward Transconductance	g_{FS}	$V_{DS} = -5.0\text{ V}_{dc}, I_D = -5.2\text{ A}_{dc}$	-	20	-	S
Diode Forward Voltage	V_{SD}	$I_S = -1.1\text{ A}_{dc}, V_{GS} = 0\text{ V}_{dc}$	-	-0.62	-1.2	V

DYNAMIC CHARACTERISTICS

Input Capacitance	C_{iss}	$V_{DS} = -6.4\text{ V}_{dc}$ $V_{GS} = 0\text{ V}$ $f = 1.0\text{ MHz}$	-	2400	-	pF
Output Capacitance	C_{oss}		-	550	-	
Transfer Capacitance	C_{rss}		-	420	-	

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6.4\text{ V}_{dc}$ $V_{GS} = -4.5\text{ V}_{dc}$ $I_D = -5.4\text{ A}_{dc}$ $R_G = 2.0\text{ }\Omega$ (Note 2)	-	7.0	-	ns
Rise Time	t_r		-	28	-	
Turn-Off Delay Time	$t_{d(off)}$		-	73	-	
Fall Time	t_f		-	60	-	
Gate Charge	Q_g	$V_{GS} = -2.5\text{ V}_{dc}$ $I_D = -5.4\text{ A}_{dc}$ $V_{DS} = -6.4\text{ V}_{dc}$	-	15	30	nC
	Q_{gs}		-	4.0	-	
	Q_{gd}		-	8.0	-	
Source-Drain Reverse Recovery Time	T_{rr}	$I_F = -1.1\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	-	90	-	ns

2. Pulse Test: Pulse Width = 250 μs , Duty Cycle = 2%.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL ELECTRICAL CHARACTERISTICS

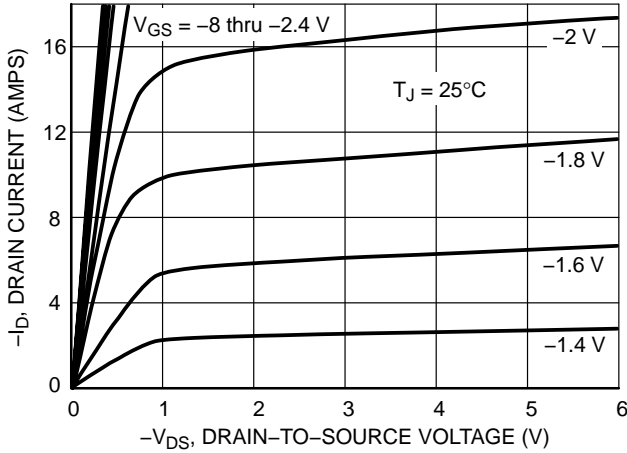


Figure 1. On-Region Characteristics

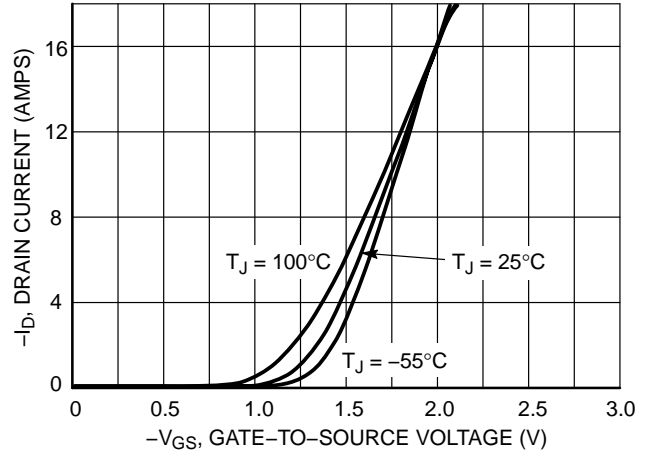


Figure 2. Transfer Characteristics

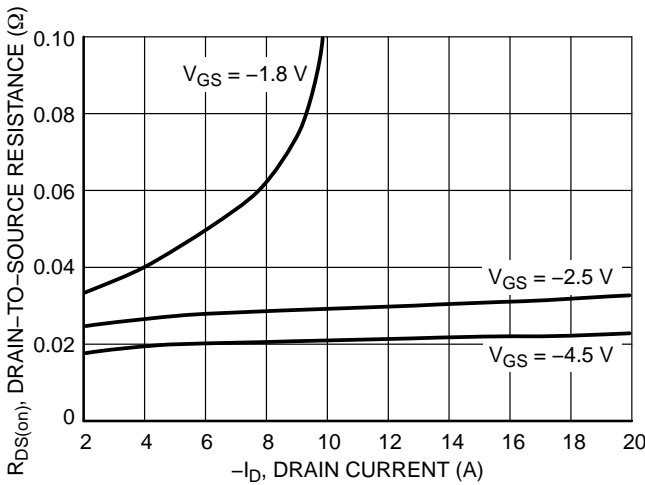


Figure 3. On-Resistance versus Drain Current and Gate Voltage

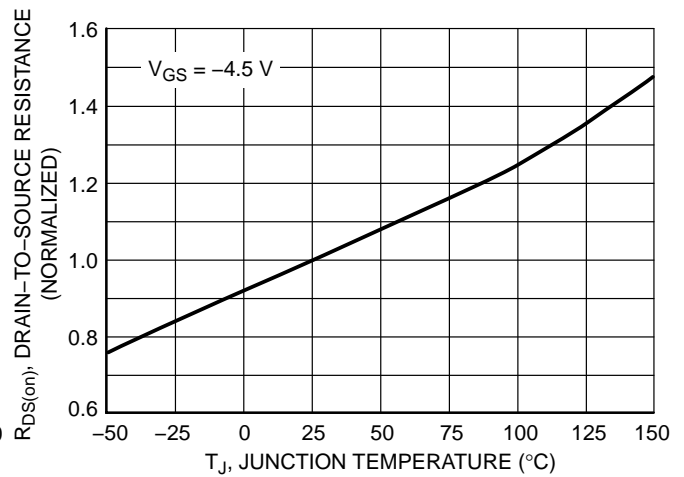


Figure 4. On-Resistance Variation with Temperature

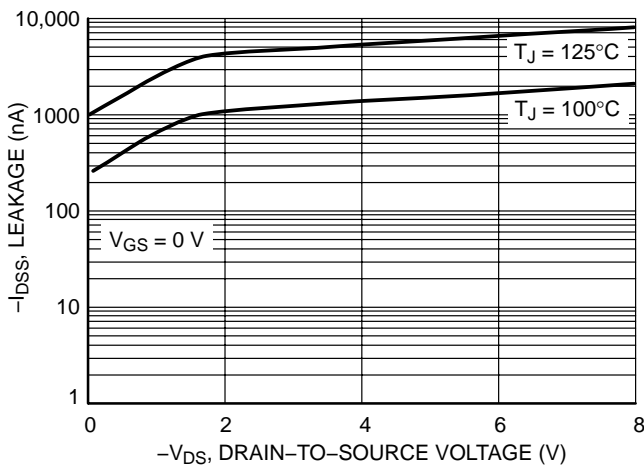


Figure 5. Drain-to-Source Leakage Current versus Voltage

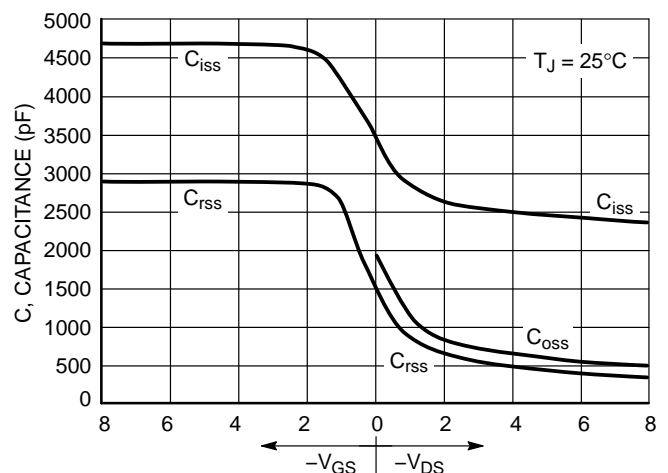


Figure 6. Capacitance Variation

TYPICAL ELECTRICAL CHARACTERISTICS

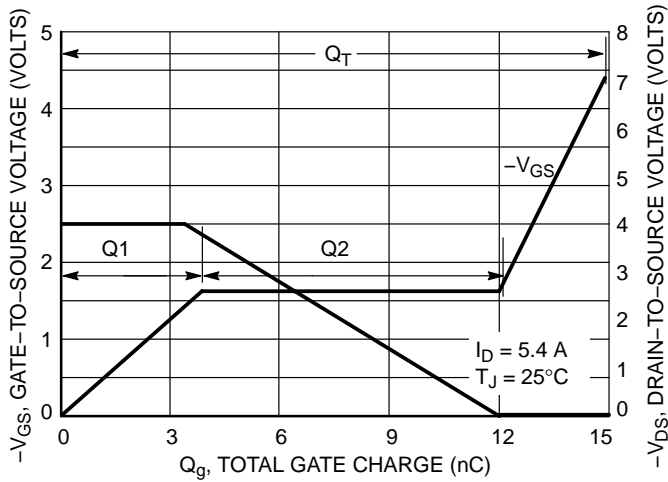


Figure 7. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

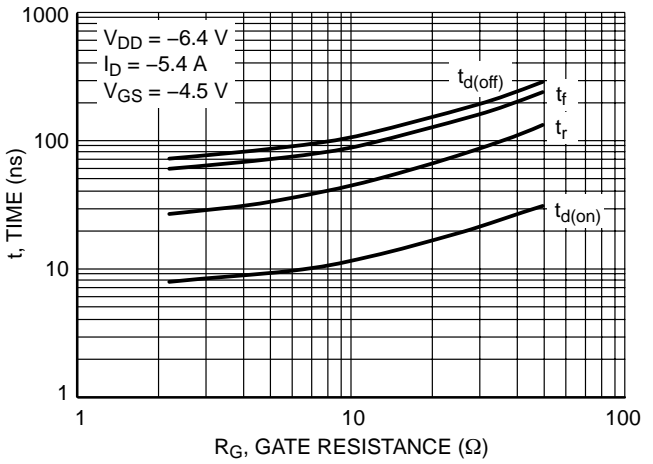


Figure 8. Resistive Switching Time Variation versus Gate Resistance

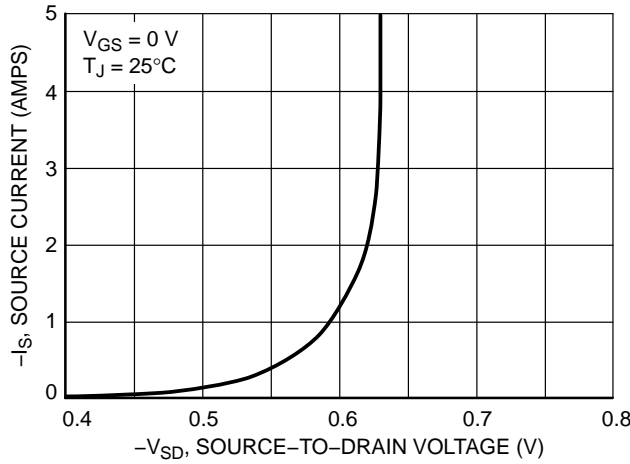


Figure 9. Diode Forward Voltage versus Current

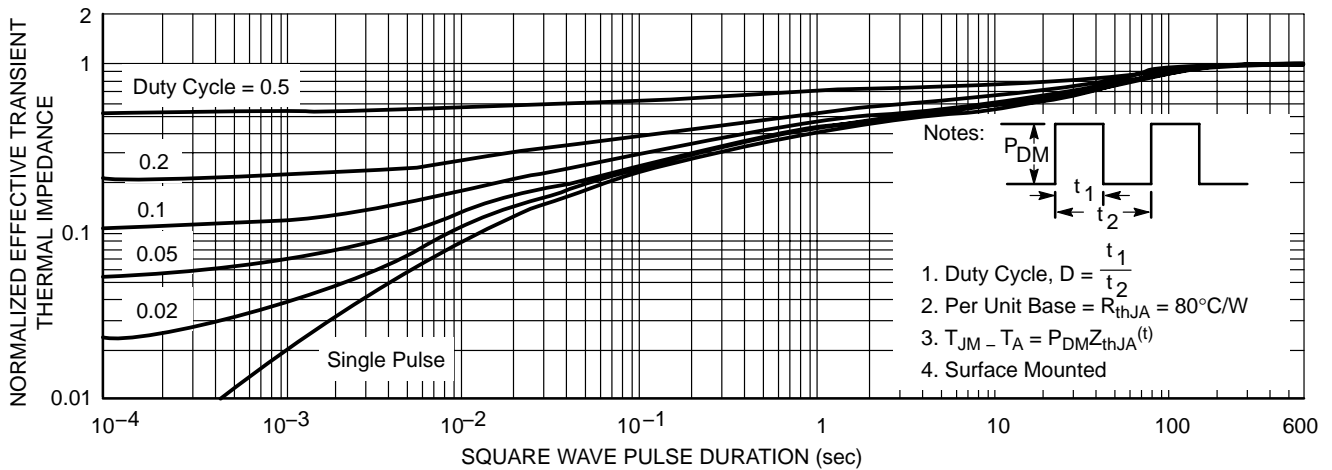
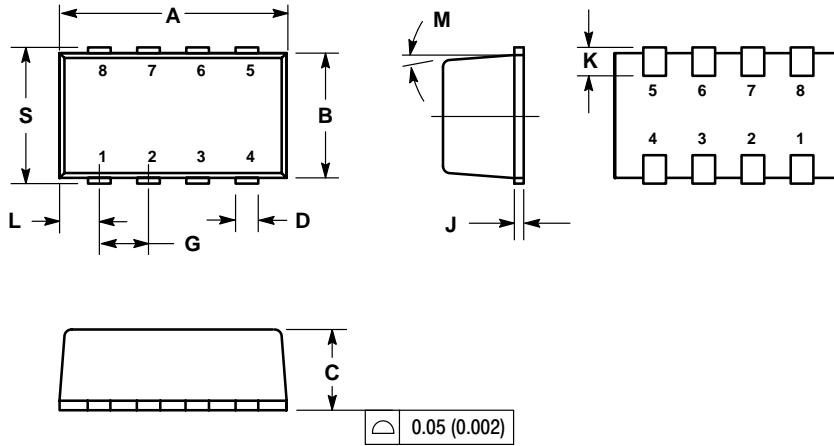


Figure 10. Normalized Thermal Transient Impedance, Junction-to-Ambient

NTHS2101P

PACKAGE DIMENSIONS

ChipFET CASE 1206A-03 ISSUE E



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.
7. 1206A-01 AND 1206A-02 OBSOLETE. NEW STANDARD IS 1206A-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.95	3.10	0.116	0.122
B	1.55	1.70	0.061	0.067
C	1.00	1.10	0.039	0.043
D	0.25	0.35	0.010	0.014
G	0.65 BSC		0.025 BSC	
J	0.10	0.20	0.004	0.008
K	0.28	0.42	0.011	0.017
L	0.55 BSC		0.022 BSC	
M	5 ° NOM		5 ° NOM	
S	1.80	2.00	0.072	0.080

STYLE 1:

- PIN 1: DRAIN
2: DRAIN
3: DRAIN
4: GATE
5: SOURCE
6: DRAIN
7: DRAIN
8: DRAIN

SOLDERING FOOTPRINT*

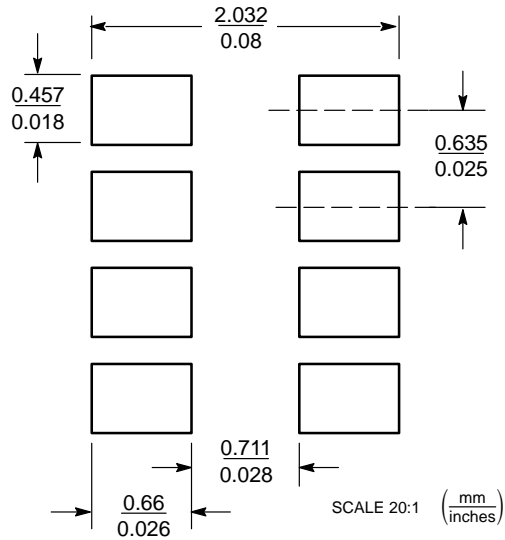


Figure 11. Basic

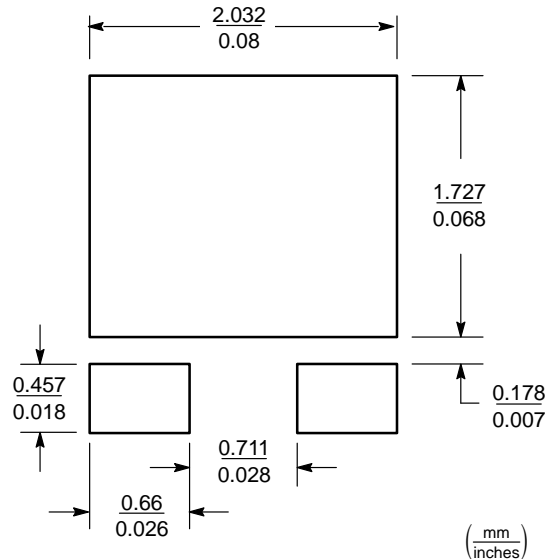



Figure 12. Style 1

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