NTHD2102P

Trench Power MOSFET 8.0 V, 3.4 A Dual P-Channel ChipFET™

ON Semiconductor®

http://onsemi.com

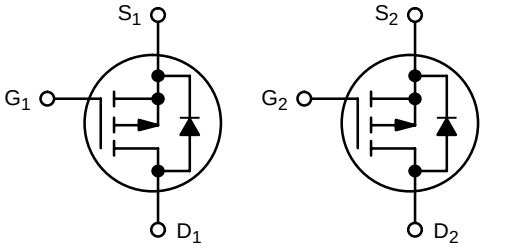
Features

- Offers an Ultra Low $R_{DS(on)}$ Solution in the ChipFET Package
- Miniature ChipFET Package 40% Smaller Footprint than TSOP−6 making it an Ideal Device for Applications where Board Space is at a Premium
- Low Profile (<1.1 mm) Allows it to Fit Easily into Extremely Thin Environments such as Portable Electronics
- Designed to Provide Low $R_{DS(on)}$ at Gate Voltage as Low as 1.8 V, the Operating Voltage used in many Logic ICs in Portable Electronics
- Simplifies Circuit Design since Additional Boost Circuits for Gate Voltages are not Required
- Operated at Standard Logic Level Gate Drive, Facilitating Future Migration to Lower Levels using the same Basic Topology

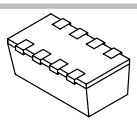
Applications

- Optimized for Battery and Load Management Applications in Portable Equipment such as MP3 Players, Cell Phones, Digital Cameras, Personal Digital Assistant and other Portable Applications
- Charge Control in Battery Chargers
- Buck and Boost Converters

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
8 V	50 mΩ @ −4.5 V	3.4 A
	68 mΩ @ −2.5 V	
	100 mΩ @ −1.8 V	



P−Channel MOSFET P−Channel MOSFET



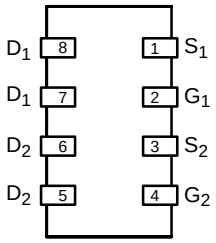
ChipFET
CASE 1206A
Style 2

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

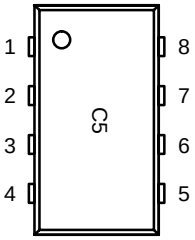
Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	−8.0	V_{dc}
Gate−to−Source Voltage − Continuous	V_{GS}	±8.0	V_{dc}
Drain Current − Continuous − 5 seconds	I_D I_D	−3.4 −4.6	A
Total Power Dissipation Continuous @ T_A = 25°C (5 sec) @ T_A = 25°C Continuous @ 85°C (5 sec) @ 85°C	P_D	 1.1 2.1 0.6 1.1	W
Continuous Source Current (Diode Conduction)	Is	−1.1	A
Thermal Resistance (Note 1) Junction−to−Ambient, 5 sec Junction−to−Ambient, Continuous	 $R_{\theta JA}$ $R_{\theta JA}$	 60 113	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

1. When surface mounted to a 1″ x 1″ FR4 board.

PIN CONNECTIONS



MARKING DIAGRAM



C5 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
NTHD2102PT1	ChipFET	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (Note 2) Temperature Coefficient (Positive)	$V_{(Br)DSS}$	V_{GS} = 0 V_{dc}, I_D = −250 μA_{dc}	−8.0	−	−	V_{dc}
Gate−Body Leakage Current Zero	I_{GSS}	V_{DS} = 0 V_{dc}, V_{GS} = ±8.0 V_{dc}	−	−	±100	nA_{dc}
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −6.4 V_{dc}, V_{GS} = 0 V_{dc} V_{DS} = −6.4 V_{dc}, V_{GS} = 0 V_{dc}, T_J = 85°C	− −	− −	−1.0 −5.0	μA_{dc}
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 μA_{dc}	−0.45	−	−1.5	V_{dc}
Static Drain−to−Source On−Resistance	$R_{DS(on)}$	V_{GS} = −4.5 V_{dc}, I_D = −3.4 A_{dc} V_{GS} = −2.5 V_{dc}, I_D = −2.7 A_{dc} V_{GS} = −1.8 V_{dc}, I_D = −1.0 A_{dc}	− − −	50 68 100	58 85 160	mΩ
Forward Transconductance	g_{FS}	V_{DS} = −5.0 V_{dc}, I_D = −3.4 A_{dc}	−	8.0	−	S
Diode Forward Voltage	V_{SD}	I_S = −1.1 A_{dc}, V_{GS} = 0 V_{dc}	−	−0.8	−1.2	V
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}	V_{DS} = −6.4 V_{dc} V_{GS} = 0 V f = 1.0 MHz	−	715	−	pF
Output Capacitance	C_{oss}		−	160	−	
Transfer Capacitance	C_{rss}		−	120	−	
SWITCHING CHARACTERISTICS (Note 3)						
Turn−On Delay Time	$t_{d(on)}$	V_{DD} = −6.4 V_{dc} V_{GS} = −4.5 V_{dc} I_D = −3.2 A_{dc} R_G = 2.0 Ω	−	8.0	−	ns
Rise Time	t_r		−	20	−	
Turn−Off Delay Time	$t_{d(off)}$		−	20	−	
Fall Time	t_f		−	15	−	
Gate Charge	Q_g	V_{GS} = −2.5 V_{dc} I_D = −3.2 A_{dc} V_{DS} = −6.4 V_{dc}	−	8.0	16	nC
	Q_{gs}		−	2.2	−	
	Q_{gd}		−	4.0	−	
Source−Drain Reverse Recovery Time	t_{rr}	I_F = −0.9 A_{dc}, di/dt = 100	−	15	30	nA_{dc}

2. Pulse Test: Pulse Width = 250 μs, Duty Cycle = 2%.
3. Switching characteristics are independent of operating junction temperatures.

TYPICAL ELECTRICAL CHARACTERISTICS

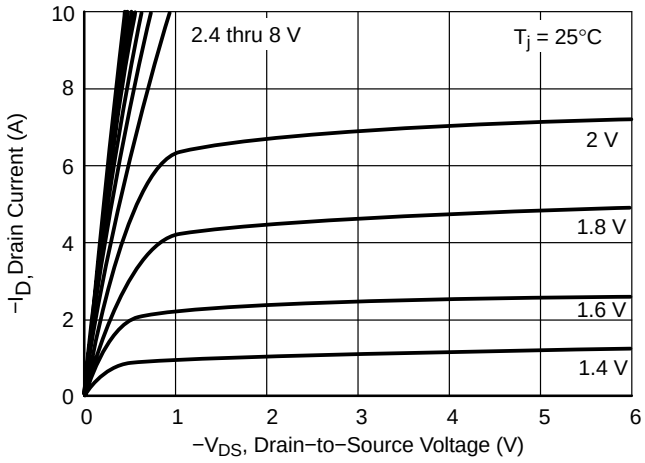


Figure 1. On−Region Characteristics

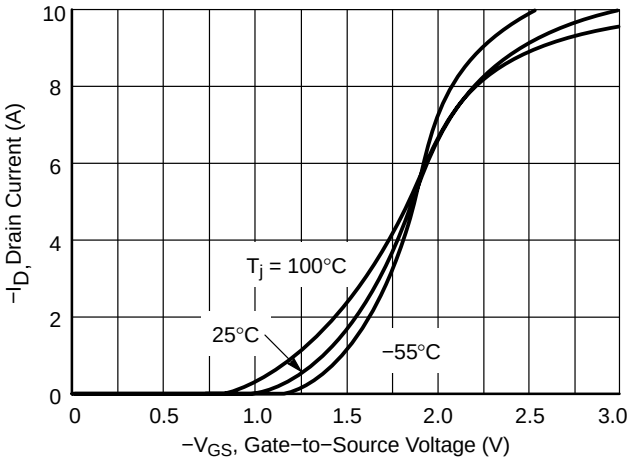


Figure 2. Transfer Characteristics

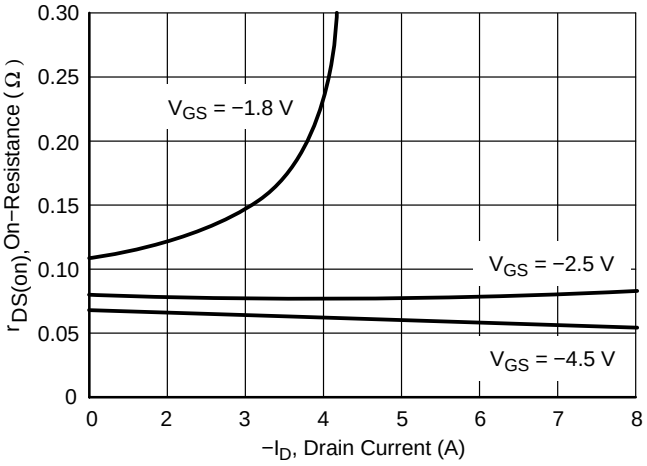


Figure 3. On−Resistance vs. Drain Current and Gate Voltage

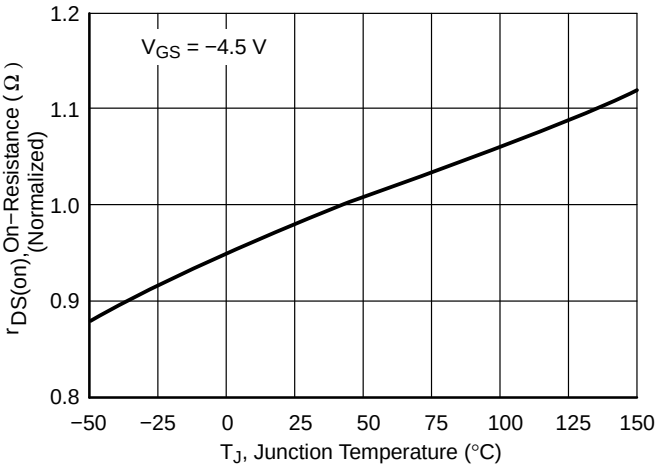


Figure 4. On−Resistance Variation vs. Temperature

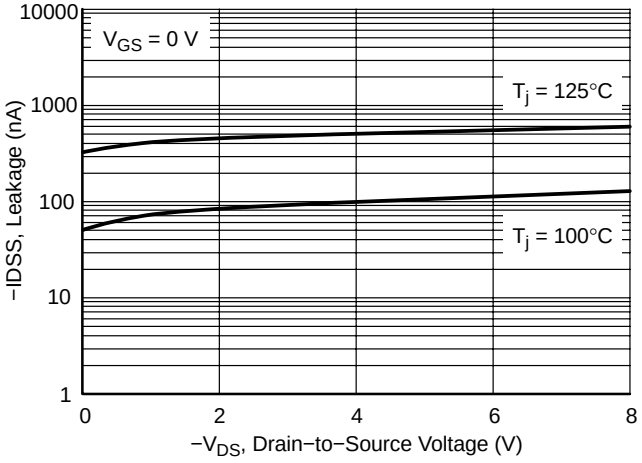


Figure 5. Drain−to−Source Leakage Current vs. Voltage

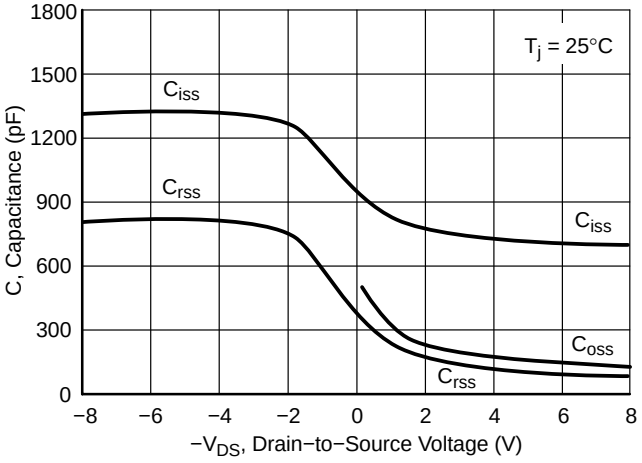


Figure 6. Capacitance Variation

TYPICAL ELECTRICAL CHARACTERISTICS

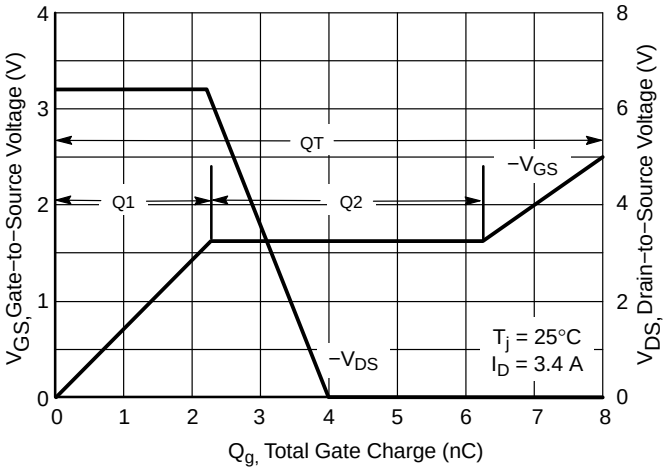


Figure 7. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

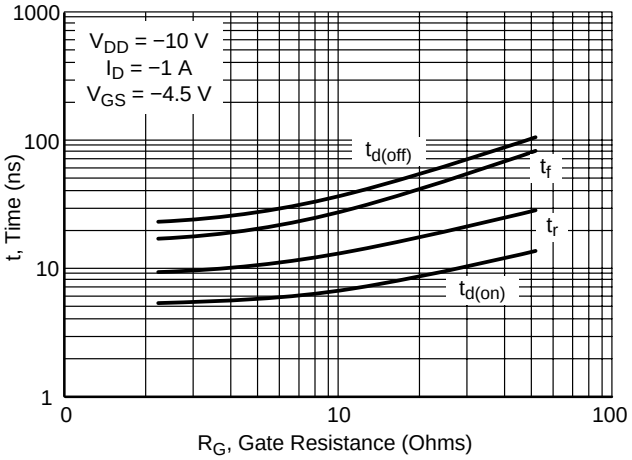


Figure 8. Resistive Switching Time Variation vs. Gate Resistance

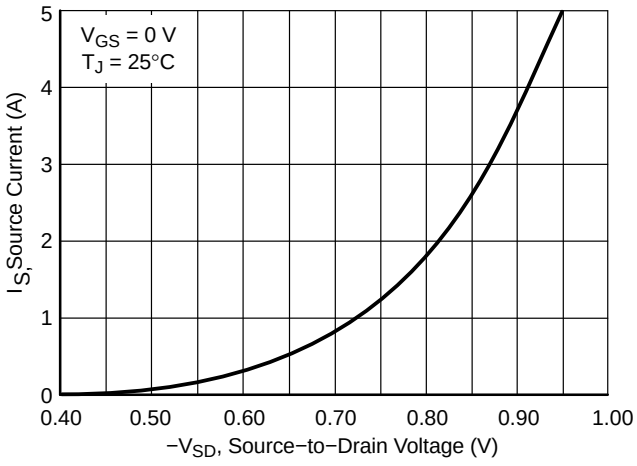


Figure 9. Diode Forward Voltage vs. Current

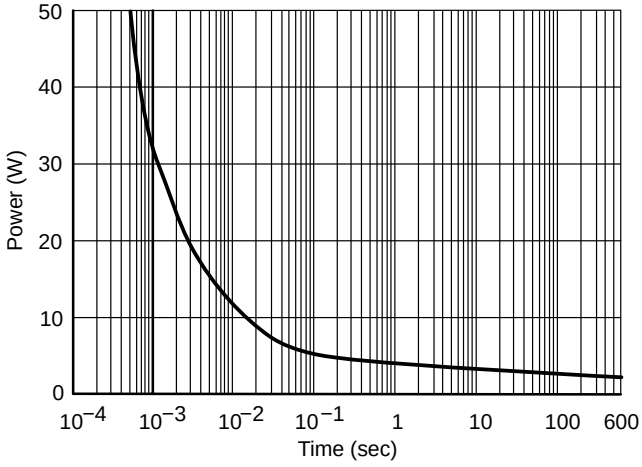


Figure 10. Single Pulse Power

TYPICAL ELECTRICAL CHARACTERISTICS

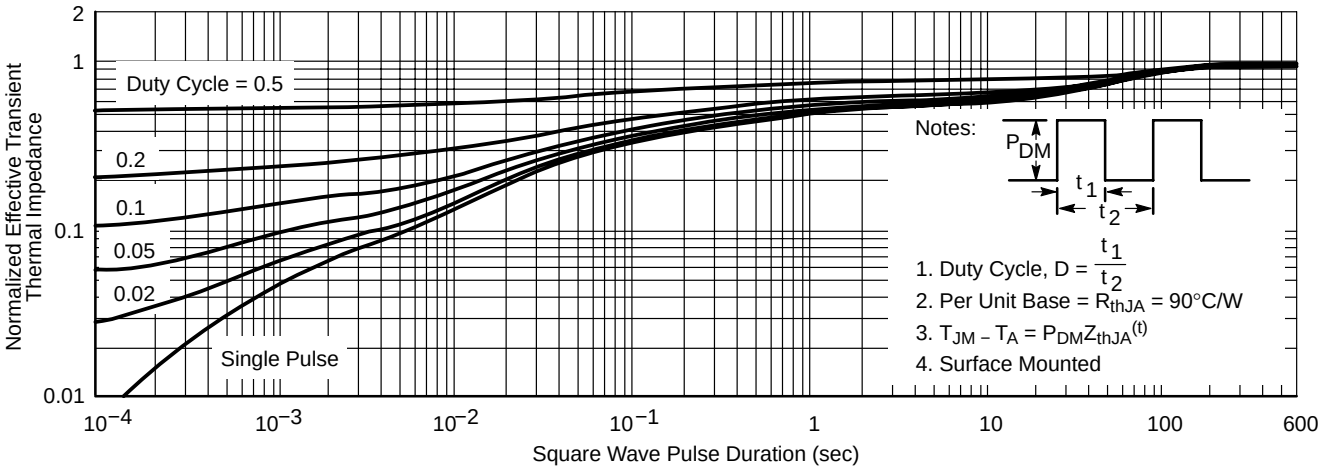


Figure 11. Normalized Thermal Transient Impedance, Junction−to−Ambient

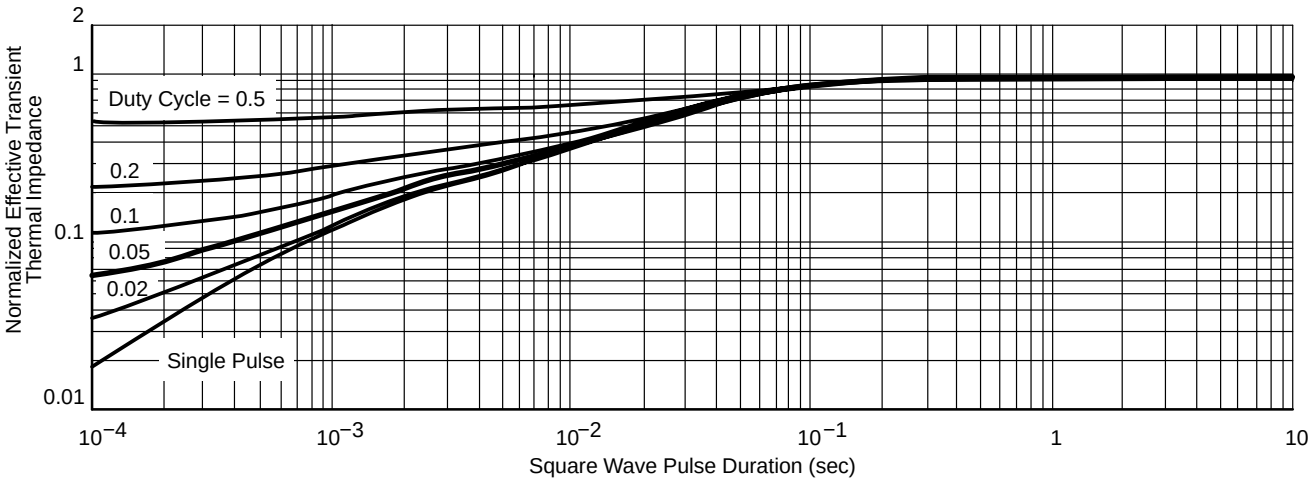


Figure 12. Normalized Thermal Transient Impedance, Junction−to−Foot

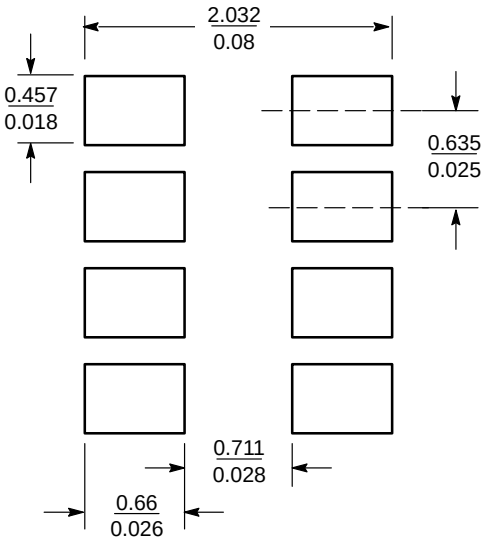


Figure 13. Basic

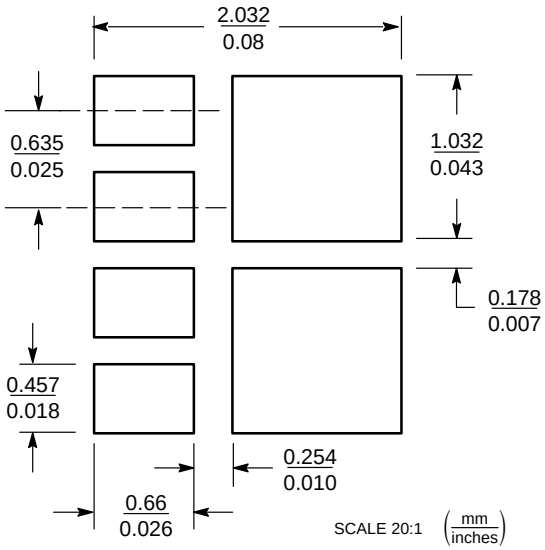


Figure 14. Style 2

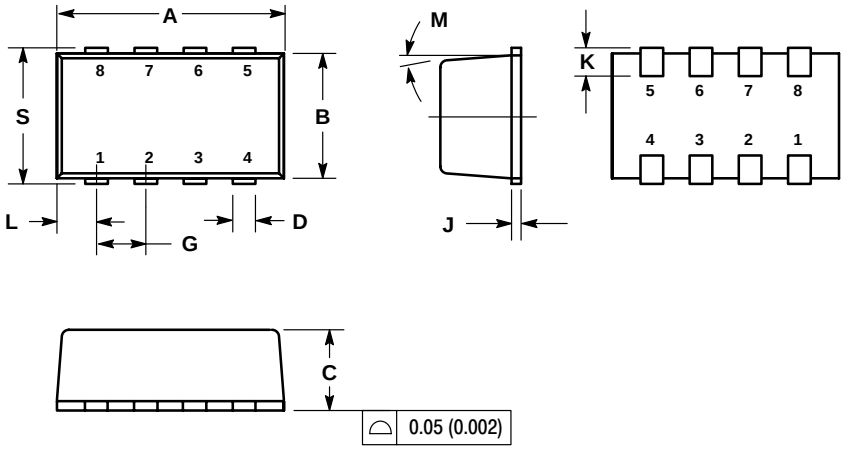
BASIC PAD PATTERNS

The basic pad layout with dimensions is shown in Figure 14. This is sufficient for low power dissipation MOSFET applications, but power semiconductor performance requires a greater copper pad area, particularly for the drain leads.

The minimum recommended pad pattern shown in Figure 13 improves the thermal area of the drain connections (pins 5, 6, 7, 8) while remaining within the confines of the basic footprint. The drain copper area is 0.0019 sq. in. (or 1.22 sq. mm). This will assist the power dissipation path away from the device (through the copper leadframe) and into the board and exterior chassis (if applicable) for the single device. The addition of a further copper area and/or the addition of vias to other board layers will enhance the performance still further.

PACKAGE DIMENSIONS

ChipFET
CASE 1206A−03
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.
7. 1206A−01 AND 1206A−02 OBSOLETE. NEW STANDARD IS 1206A−03.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.95	3.10	0.116	0.122
B	1.55	1.70	0.061	0.067
C	1.00	1.10	0.039	0.043
D	0.25	0.35	0.010	0.014
G	0.65 BSC		0.025 BSC	
J	0.10	0.20	0.004	0.008
K	0.28	0.42	0.011	0.017
L	0.55 BSC		0.022 BSC	
M	5 ° NOM		5 ° NOM	
S	1.80	2.00	0.072	0.080

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

ChipFET is a trademark of Vishay Siliconix

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2−9−1 Kamimeguro, Meguro−ku, Tokyo, Japan 153−0051
Phone: 81−3−5773−3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.