

NTHC5513

Power MOSFET

Complementary, 20 V, +3.1 A / -2.1 A,
ChipFET™

Features

- Complementary N Channel and P Channel MOSFET
- Small Size, 40% Smaller than TSOP-6 Package
- Leadless SMD package Featuring Complementary Pair
- ChipFET Package Provides Great Thermal Characteristics Similar to Larger Packages
- Low $R_{DS(on)}$ in a ChipFET Package for High Efficiency Performance
- Low Profile (< 1.10 mm) Allows Placement in Extremely Thin Environments Such as Portable Electronics

Applications

- Load Switch Applications Requiring Level Shift
- DC-to-DC Conversion Circuits
- Drive Small Brushless DC Motors
- Designed for Power Management Applications in Portable, Battery Powered Products

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	20	V
Gate-to-Source Voltage			V_{GS}	± 12	V
Continuous Drain Current (Note 1)	N-Ch Steady State	$T_A = 25^{\circ}\text{C}$	I_D	3.1	A
		$T_A = 85^{\circ}\text{C}$		2.15	
	P-Ch Steady State	$T_A = 25^{\circ}\text{C}$		-2.1	
		$T_A = 85^{\circ}\text{C}$		-1.5	
Pulsed Drain Current (Note 1)	N-Ch	$t = 10\ \mu\text{s}$	I_{DM}	10	A
	P-Ch	$t = 10\ \mu\text{s}$		-7.0	
Power Dissipation –Steady State (Note 1)		$T_A = 25^{\circ}\text{C}$	P_D	1.1	W
Operating Junction and Storage Temperature			T_J, T_{STG}	-55 to 150	$^{\circ}\text{C}$
Lead Temperature for Soldering Purposes (1/8" from case for 10 seconds)			T_L	260	$^{\circ}\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient Steady-State (Note 1)	$R_{\theta JA}$	110	$^\circ\text{C/W}$

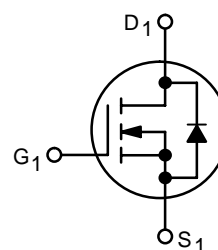
1. Surface-mounted on FR4 board using 1 in sq. pad size (Cu area = 1.127 in sq. [1 oz] including traces).



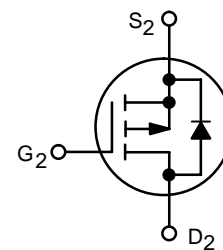
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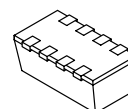
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
N-Channel 20 V	60 m Ω @ 4.5 V	3.1 A
	80 m Ω @ 2.5 V	
P-Channel -20 V	130 m Ω @ -4.5 V	-2.1 A
	200 m Ω @ -2.5 V	



N-Channel MOSFET

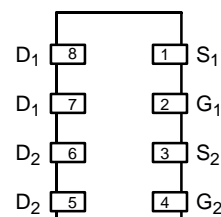


P-Channel MOSFET



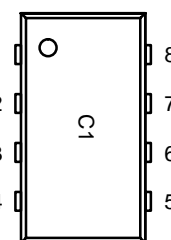
ChipFET
CASE 1206A
STYLE 2

PIN CONNECTIONS



Bottom View

MARKING DIAGRAM



Top View

C1 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
NTHC5513T1	ChipFET	3000/Tape & Reel
NTHC5513T1G	ChipFET (Pb-Free)	3000/Tape & Reel

NTHC5513

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS (Note 2)

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	N	V _{GS} = 0 V	I _D = 250 μA	20		V
		P		I _D = -250 μA	-20		
Zero Gate Voltage Drain Current	I _{DSS}	N	V _{GS} = 0 V, V _{DS} = 16 V			1.0	μA
		P	V _{GS} = 0 V, V _{DS} = -16 V			-1.0	
		N	V _{GS} = 0 V, V _{DS} = 16 V, T _J = 85 °C			5	
		P	V _{GS} = 0 V, V _{DS} = -16 V, T _J = 85 °C			-5	
Gate-to-Source Leakage Current	I _{GSS}		V _{DS} = 0 V, V _{GS} = ±12 V			±100	nA

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	V _{GS(TH)}	N	V _{GS} = V _{DS}	I _D = 250 μA	0.6	1.2	V
		P		I _D = -250 μA	-0.6	-1.2	
Drain-to-Source On Resistance	R _{DS(on)}	N	V _{GS} = 4.5 V, I _D = 3.1 A		0.058	0.080	Ω
		P	V _{GS} = -4.5 V, I _D = -2.1 A		0.130	0.155	
		N	V _{GS} = 2.5 V, I _D = 2.3 A		0.077	0.115	
		P	V _{GS} = -2.5 V, I _D = -1.7 A		0.200	0.240	
Forward Transconductance	g _{FS}	N	V _{DS} = 10 V, I _D = 3.0 A		6.0		S
		P	V _{DS} = -10 V, I _D = -2.1 A		6.0		

CHARGES AND CAPACITANCES

Input Capacitance	C _{ISS}	N	f = 1 MHz, V _{GS} = 0 V	V _{DS} = 10 V	180		pF
		P		V _{DS} = -10 V	185		
Output Capacitance	C _{OSS}	N		V _{DS} = 10 V	80		
		P		V _{DS} = -10 V	95		
Reverse Transfer Capacitance	C _{RSS}	N		V _{DS} = 10 V	25		
		P		V _{DS} = -10 V	30		
Total Gate Charge	Q _{G(TOT)}	N		V _{GS} = 4.5 V, V _{DS} = 10 V, I _D = 3.1 A	2.6	4.0	nC
		P		V _{GS} = -4.5 V, V _{DS} = -10 V, I _D = -2.1 A	3.0	6.0	
Gate-to-Source Gate Charge	Q _{GS}	N		V _{GS} = 4.5 V, V _{DS} = 10 V, I _D = 3.1 A	0.6		
		P		V _{GS} = -4.5 V, V _{DS} = -10 V, I _D = -2.1 A	0.5		
Gate-to-Drain "Miller" Charge	Q _{GD}	N		V _{GS} = 4.5 V, V _{DS} = 10 V, I _D = 3.1 A	0.7		
		P		V _{GS} = -4.5 V, V _{DS} = -10 V, I _D = -2.1 A	0.9		

NOTES:

- Pulse Test: pulse width ≤ 250 μs, duty cycle ≤ 2%.
- Switching characteristics are independent of operating junction temperatures.

NTHC5513

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions	Min	Typ	Max	Unit
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SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	t _{d(ON)}	N	V _{DD} = 16 V, V _{GS} = 4.5 V, I _D = 3.1 A, R _G = 2.5 Ω		5.0	10	ns
Rise Time	t _r				9.0	18	
Turn-Off Delay Time	t _{d(OFF)}				10	20	
Fall Time	t _f				3.0	6.0	
Turn-On Delay Time	t _{d(ON)}	P	V _{DD} = -16 V, V _{GS} = -4.5 V, I _D = -2.1 A, R _G = 2.5 Ω		7.0	12	
Rise Time	t _r				13	25	
Turn-Off Delay Time	t _{d(OFF)}				33	50	
Fall Time	t _f				27	40	

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage (Note 2)5	V _{SD}	N	V _{GS} = 0 V	I _S = 3.1 A		0.8	1.15	V
		P		I _S = -2.1 A		-0.8	-1.15	
Reverse Recovery Time (Note 3)	t _{RR}	N	V _{GS} = 0 V, dI _S / dt = 100 A/μs	I _S = 1.5 A		12.5		ns
		P		I _S = -1.5 A		32		
Charge Time	t _a	N		I _S = 1.5 A		9.0		
		P		I _S = -1.5 A		10		
Discharge Time	t _b	N		I _S = 1.5 A		3.5		
		P		I _S = -1.5 A		22		
Reverse Recovery Charge	Q _{RR}	N		I _S = 1.5 A		6.0		nC
		P		I _S = -1.5 A		15		

NOTES:

- Pulse Test: pulse width ≤ 250 μs, duty cycle ≤ 2%.
- Switching characteristics are independent of operating junction temperatures.

TYPICAL N-CHANNEL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)

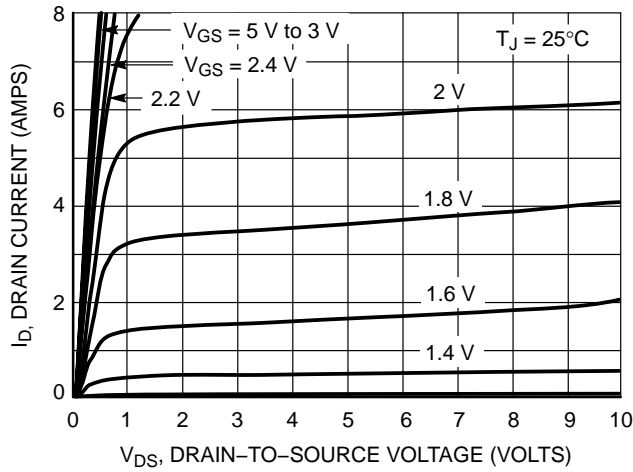


Figure 1. On-Region Characteristics

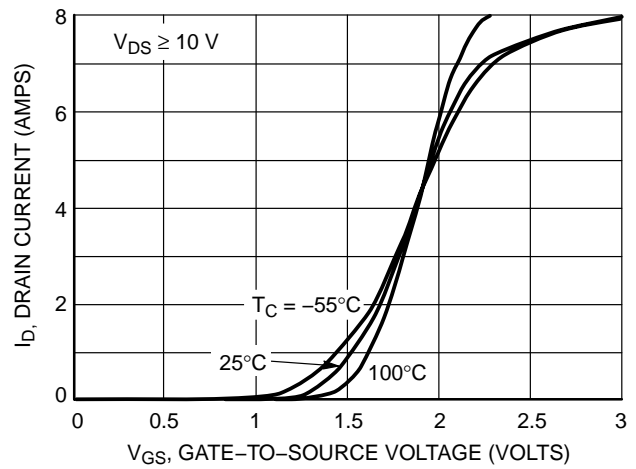


Figure 2. Transfer Characteristics

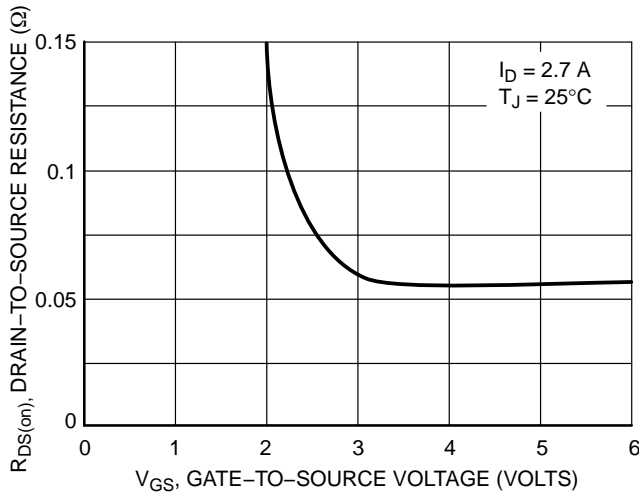


Figure 3. On-Resistance vs. Gate-to-Source Voltage

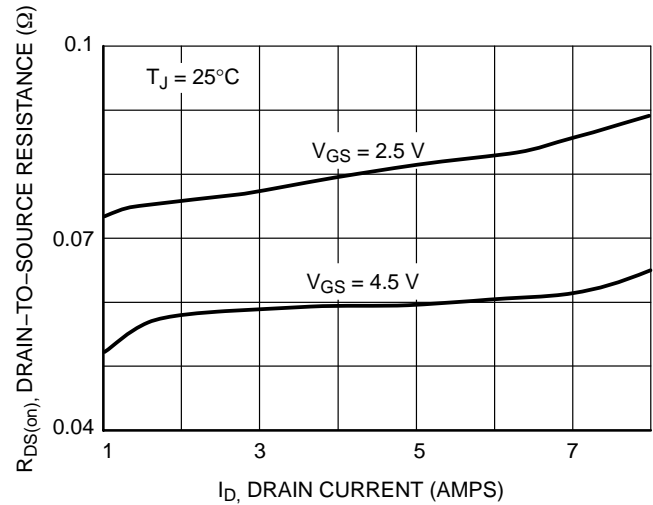


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

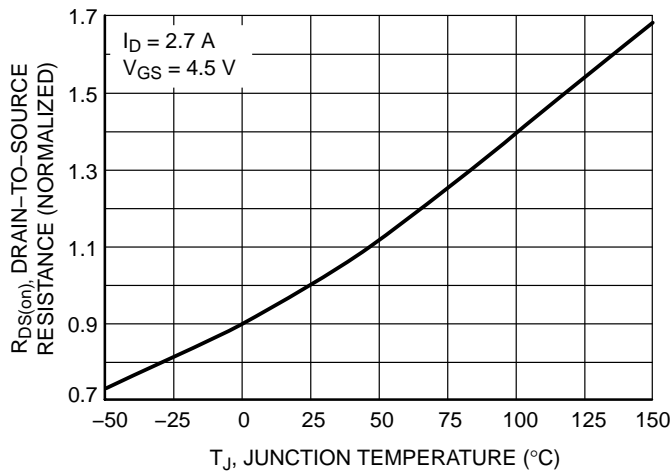


Figure 5. On-Resistance Variation with Temperature

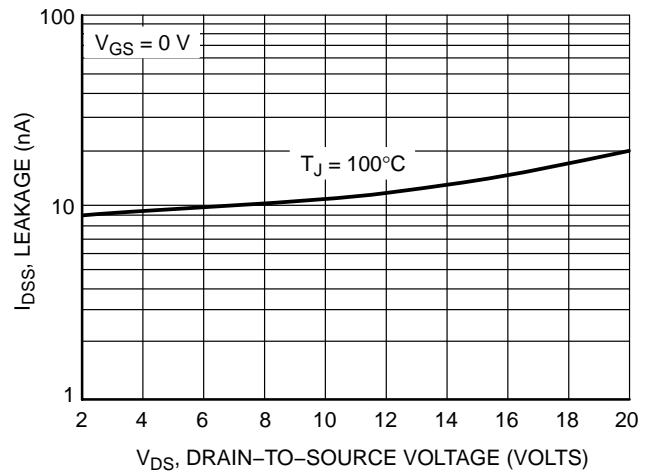
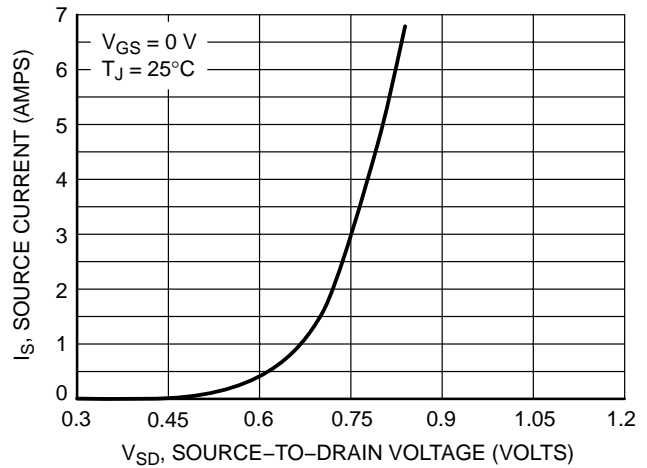
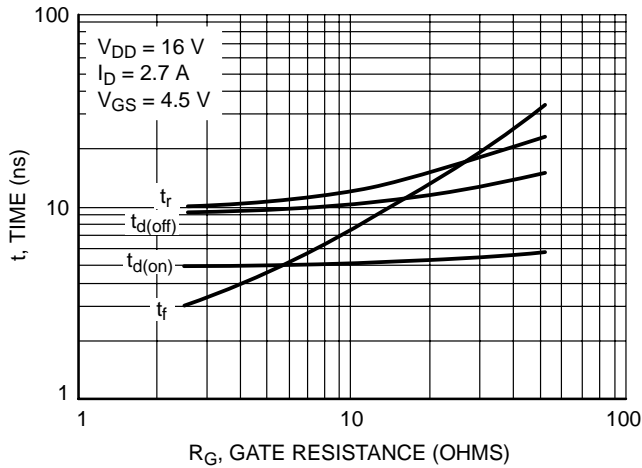
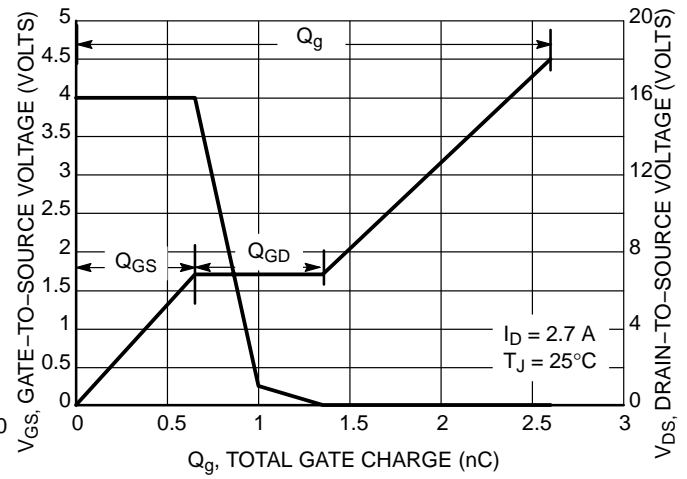
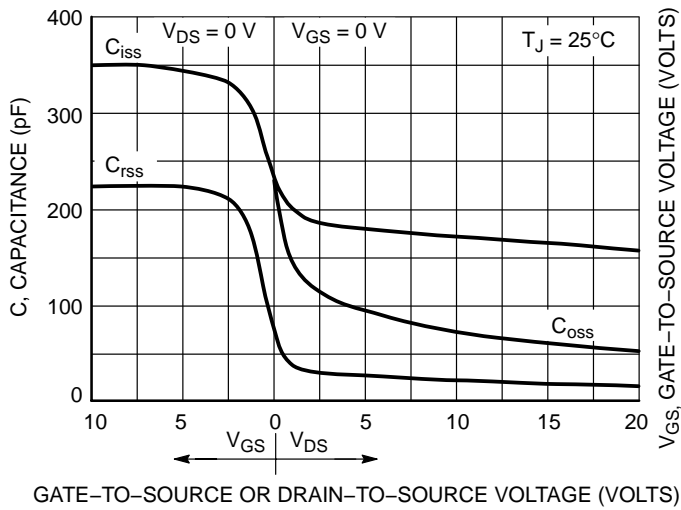


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL N-CHANNEL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)



TYPICAL P-CHANNEL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)

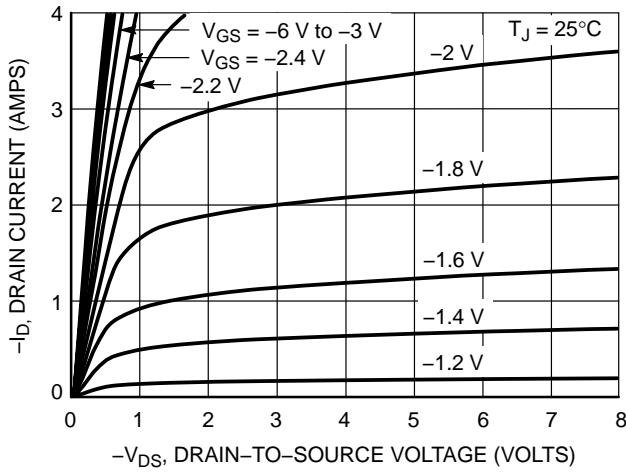


Figure 11. On-Region Characteristics

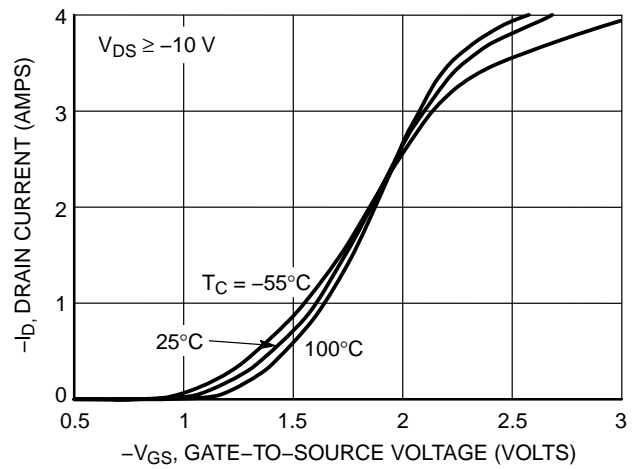


Figure 12. Transfer Characteristics

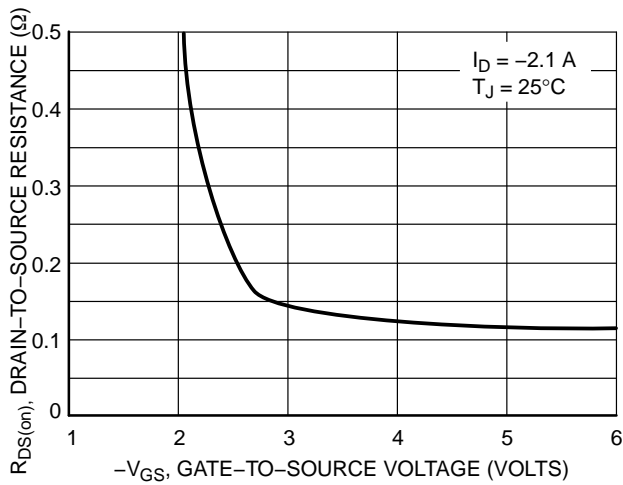


Figure 13. On-Resistance vs. Gate-to-Source Voltage

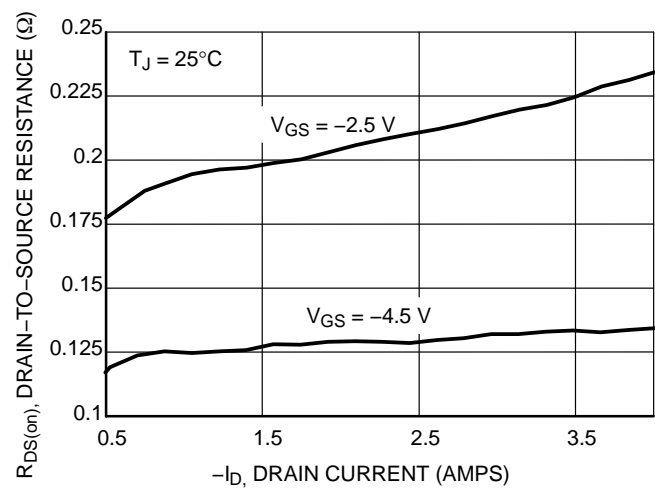


Figure 14. On-Resistance vs. Drain Current and Gate Voltage

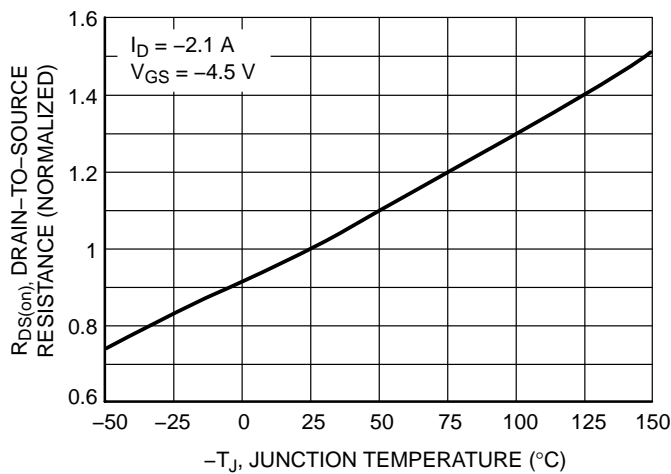


Figure 15. On-Resistance Variation with Temperature

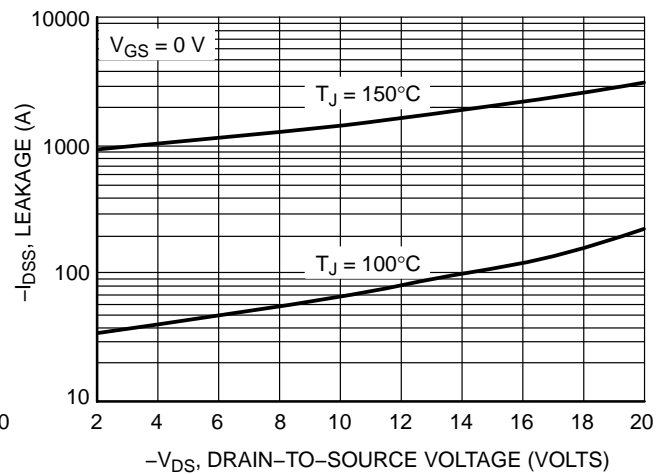


Figure 16. Drain-to-Source Leakage Current vs. Voltage

TYPICAL P-CHANNEL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)

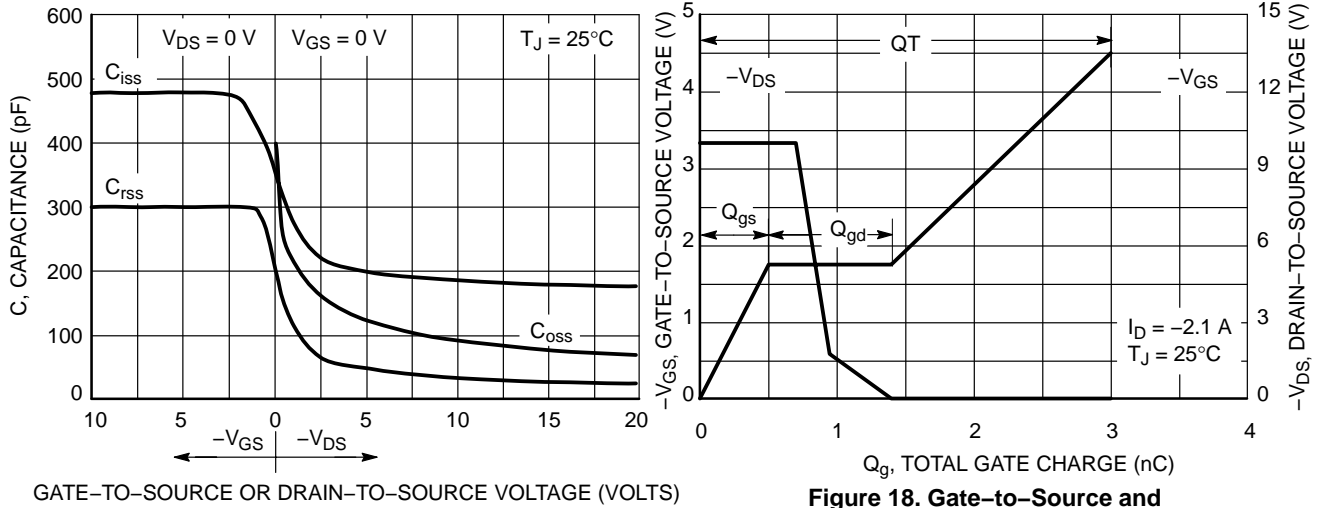


Figure 17. Capacitance Variation

Figure 18. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

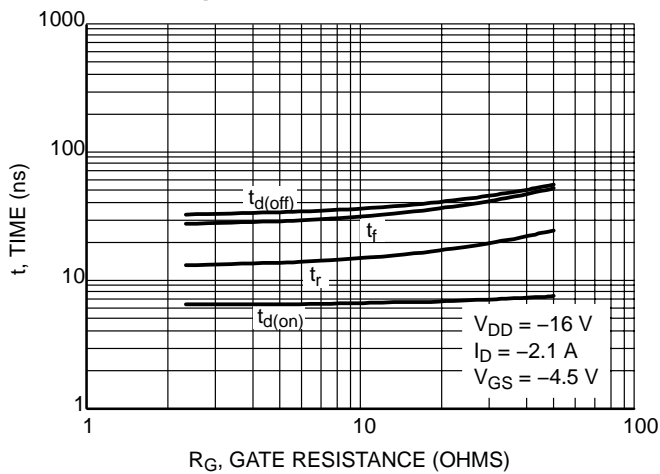


Figure 19. Resistive Switching Time Variation vs. Gate Resistance

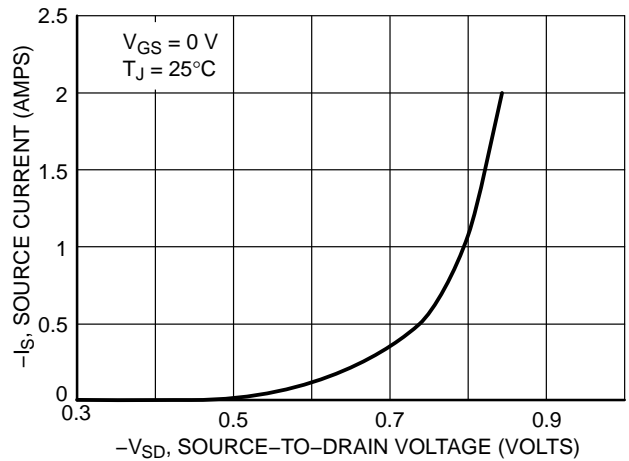


Figure 20. Diode Forward Voltage vs. Current

TYPICAL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)

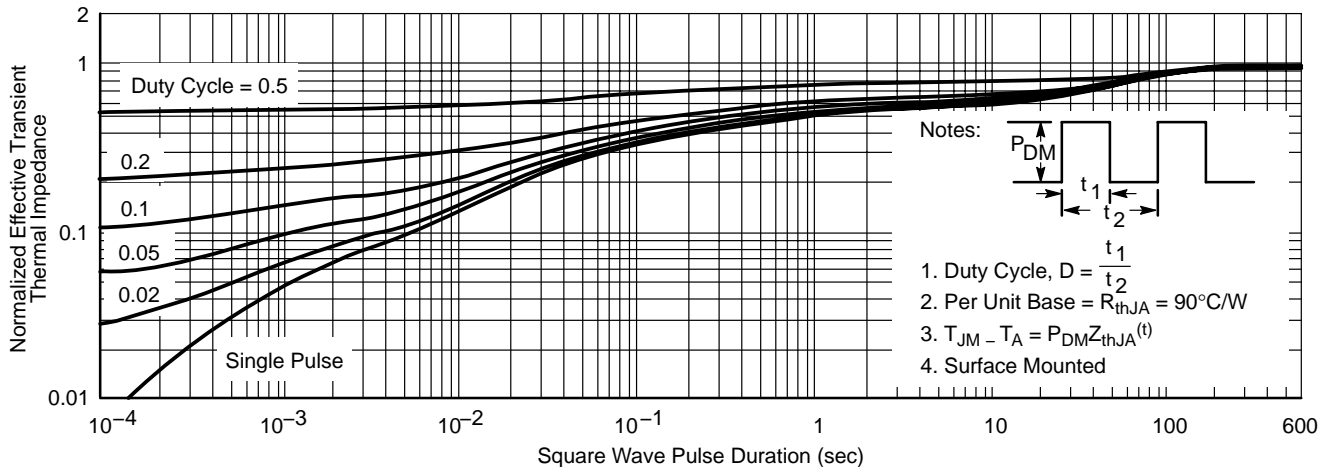


Figure 21. Thermal Response

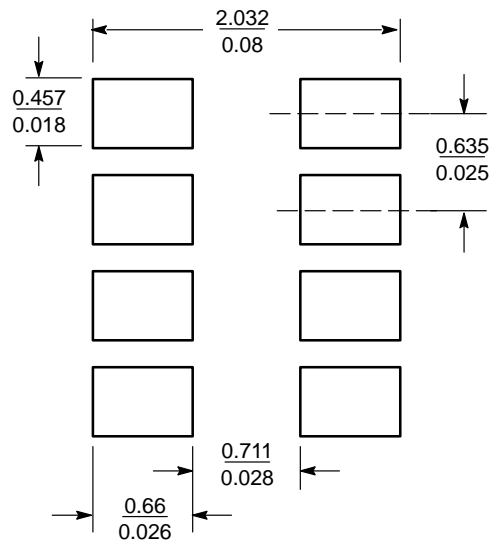


Figure 22. Basic

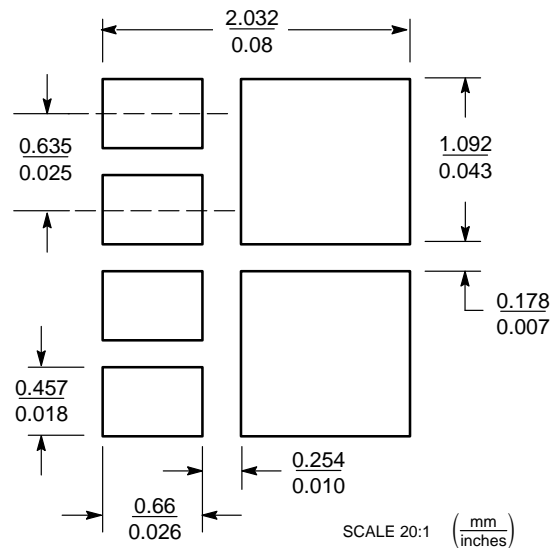


Figure 23. Style 2

BASIC PAD PATTERNS

The basic pad layout with dimensions is shown in Figure 22. This is sufficient for low power dissipation MOSFET applications, but power semiconductor performance requires a greater copper pad area, particularly for the drain leads.

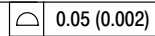
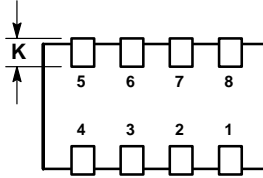
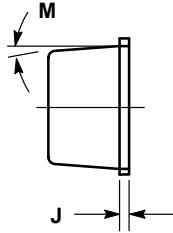
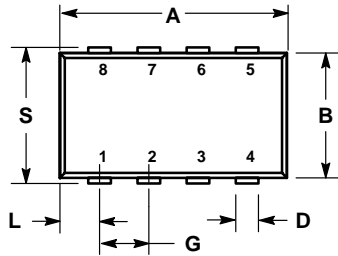
The minimum recommended pad pattern shown in Figure 23 improves the thermal area of the drain connections (pins 5, 6, 7, 8) while remaining within the

confines of the basic footprint. The drain copper area is 0.0019 sq. in. (or 1.22 sq. mm). This will assist the power dissipation path away from the device (through the copper lead-frame) and into the board and exterior chassis (if applicable) for the single device. The addition of a further copper area and/or the addition of vias to other board layers will enhance the performance still further.

NTHC5513

PACKAGE DIMENSIONS

ChipFET CASE 1206A-03 ISSUE E




- STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.
7. 1206A-01 AND 1206A-02 OBSOLETE. NEW STANDARD IS 1206A-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.95	3.10	0.116	0.122
B	1.55	1.70	0.061	0.067
C	1.00	1.10	0.039	0.043
D	0.25	0.35	0.010	0.014
G	0.65 BSC		0.025 BSC	
J	0.10	0.20	0.004	0.008
K	0.28	0.42	0.011	0.017
L	0.55 BSC		0.022 BSC	
M	5 ° NOM		5 ° NOM	
S	1.80	2.00	0.072	0.080

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