NTD110N02R

Power MOSFET
110 Amps, 24 Volts

N−Channel DPAK

Features

- Planar HD3e Process for Fast Switching Performance
- Low $R_{DS(on)}$ to Minimize Conduction Loss
- Low C_{iss} to Minimize Driver Loss
- Low Gate Charge
- Optimized for High Side Switching Requirements in High−Efficiency DC−DC Converters

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	24	Vdc
Gate−to−Source Voltage − Continuous	V_{GS}	±20	Vdc
Thermal Resistance − Junction−to−Case Total Power Dissipation @ T_C = 25°C Drain Current − Continuous @ T_C = 25°C, Chip − Continuous @ T_C = 25°C, Limited by Package − Continuous @ T_A = 25°C, Limited by Wires − Single Pulse (t_p = 10 μs)	$R_{\theta JC}$ P_D I_D I_D I_D I_D	1.35 92.5 110 110 32 110	°C/W W A A A A
Thermal Resistance − Junction−to−Ambient (Note 1) − Total Power Dissipation @ T_A = 25°C − Drain Current − Continuous @ T_A = 25°C	 $R_{\theta JA}$ P_D I_D	 52 2.4 17	 °C/W W A
Thermal Resistance − Junction−to−Ambient (Note 2) − Total Power Dissipation @ T_A = 25°C − Drain Current − Continuous @ T_A = 25°C	 $R_{\theta JA}$ P_D I_D	 100 1.25 12	 °C/W W A
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = 50 Vdc, V_{GS} = 10 Vdc, I_L = 15.5 Apk, L = 1.0 mH, R_G = 25 Ω)	E_{AS}	120	mJ
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

1. When surface mounted to an FR4 board using 0.5 sq. in. drain pad size.
2. When surface mounted to an FR4 board using the minimum recommended pad size.

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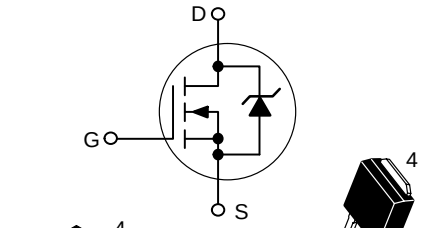
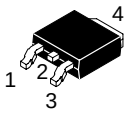
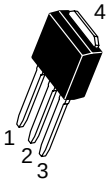
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
24 V	3.7 mΩ @ 4.5 V	110 A

N−Channel



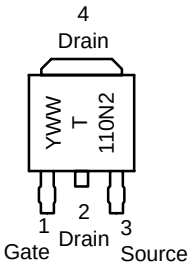


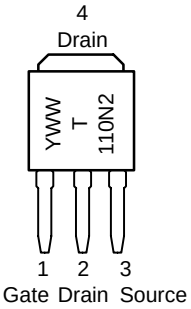
CASE 369AA
DPAK
(Surface Mount)
STYLE 2



CASE 369D
DPAK
(Straight Lead)
STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENTS





Y = Year
WW = Work Week
T110N2 = Device Code

ORDERING INFORMATION

Device	Package	Shipping
NTD110N02R	DPAK	75 Units/Rail
NTD110N02RT4	DPAK	2500/Tape & Reel
NTD110N02R−1	DPAK Straight Lead	75 Units/Rail

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (Note 3) (V_{GS} = 0 Vdc, I_D = 250 μAdc) Positive Temperature Coefficient		$V_{(BR)DSS}$	 24 −	 28 15	 − −	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	 − −	 − −	 1.5 10	μAdc
Gate−Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	−	−	±100	nAdc
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage (Note 3) (V_{DS} = V_{GS}, I_D = 250 μAdc) Negative Threshold Temperature Coefficient		$V_{GS(th)}$	 1.0 −	 1.5 5.0	 2.0 −	Vdc mV/°C
Static Drain−to−Source On−Resistance (Note 3) (V_{GS} = 10 Vdc, I_D = 110 Adc) (V_{GS} = 4.5 Vdc, I_D = 55 Adc) (V_{GS} = 10 Vdc, I_D = 20 Adc) (V_{GS} = 4.5 Vdc, I_D = 20 Adc)		$R_{DS(on)}$	 − − − −	 3.7 4.9 3.7 4.7	 − − 4.6 6.2	mΩ
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 15 Adc) (Note 3)		g_{FS}	−	44	−	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	−	2710	3440	pF
Output Capacitance		C_{oss}	−	1105	1670	
Transfer Capacitance		C_{rss}	−	227	640	
SWITCHING CHARACTERISTICS (Note 4)						
Turn−On Delay Time	(V_{GS} = 10 Vdc, V_{DD} = 10 Vdc, I_D = 40 Adc, R_G = 3.0 Ω)	$t_{d(on)}$	−	11	22	ns
Rise Time		t_r	−	39	80	
Turn−Off Delay Time		$t_{d(off)}$	−	27	40	
Fall Time		t_f	−	21	40	
Gate Charge	(V_{GS} = 4.5 Vdc, I_D = 40 Adc, V_{DS} = 10 Vdc) (Note 3)	Q_T	−	23.6	28	nC
		Q1	−	5.1	−	
		Q2	−	11	−	
SOURCE−DRAIN DIODE CHARACTERISTICS						
Forward On−Voltage	(I_S = 20 Adc, V_{GS} = 0 Vdc) (Note 3) (I_S = 55 Adc, V_{GS} = 0 Vdc) (I_S = 20 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	 − −	 0.82 0.99 0.65	 1.2 − −	Vdc
Reverse Recovery Time	(I_S = 30 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (Note 3)	t_{rr}	−	36.5	−	ns
		t_a	−	17.7	−	
		t_b	−	18.8	−	
Reverse Recovery Stored Charge		Q_{rr}	−	0.024	−	μC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

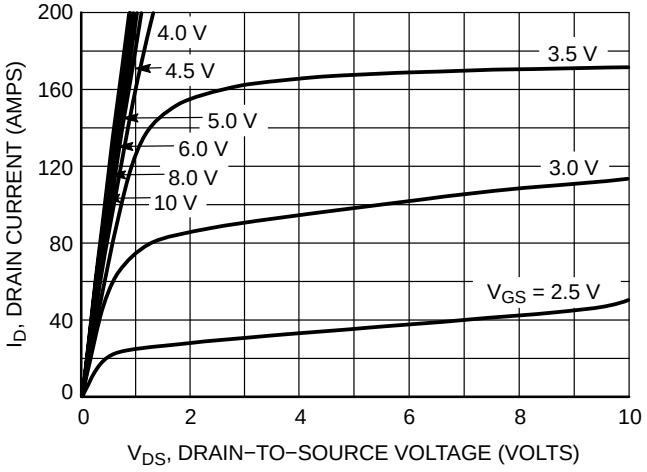


Figure 1. On−Region Characteristics

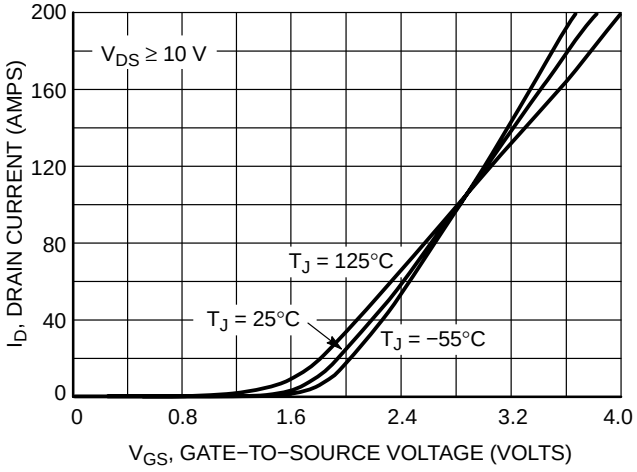


Figure 2. Transfer Characteristics

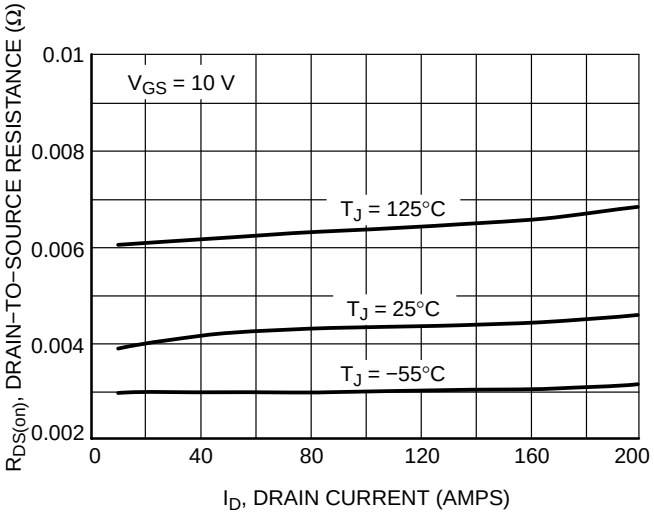


Figure 3. On−Resistance versus Drain Current and Temperature

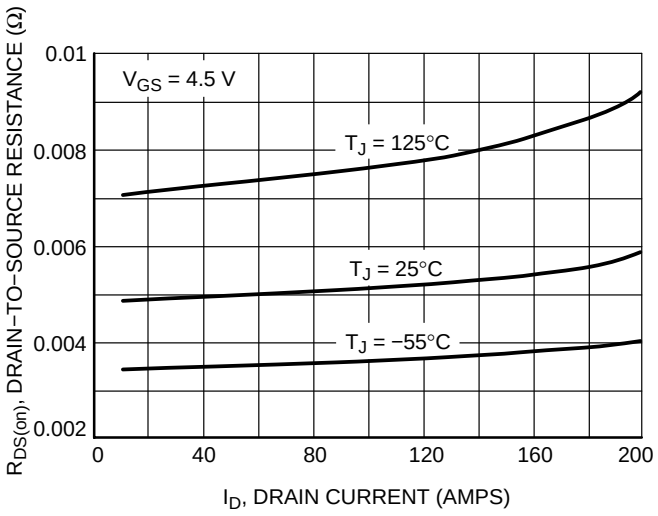


Figure 4. On−Resistance versus Drain Current and Temperature

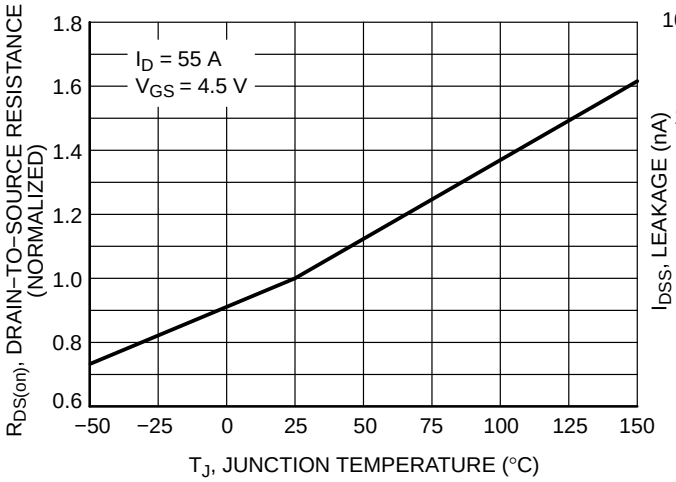


Figure 5. On−Resistance Variation with Temperature

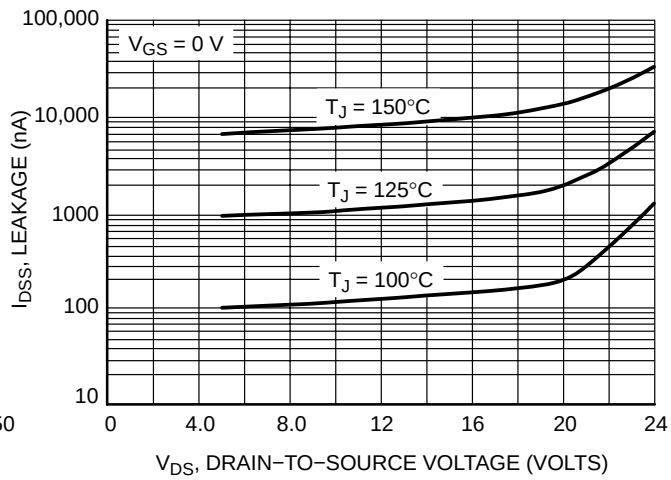


Figure 6. Drain−to−Source Leakage Current versus Voltage

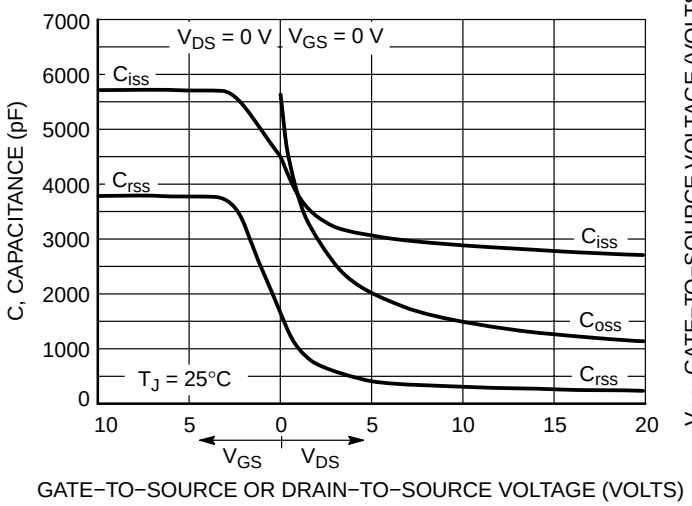


Figure 7. Capacitance Variation

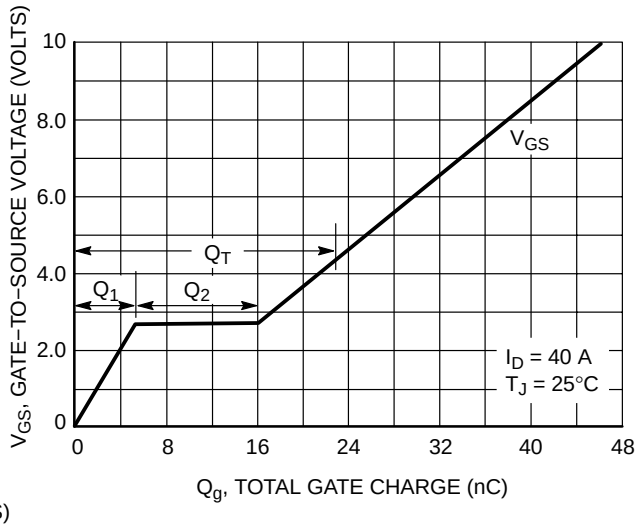


Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

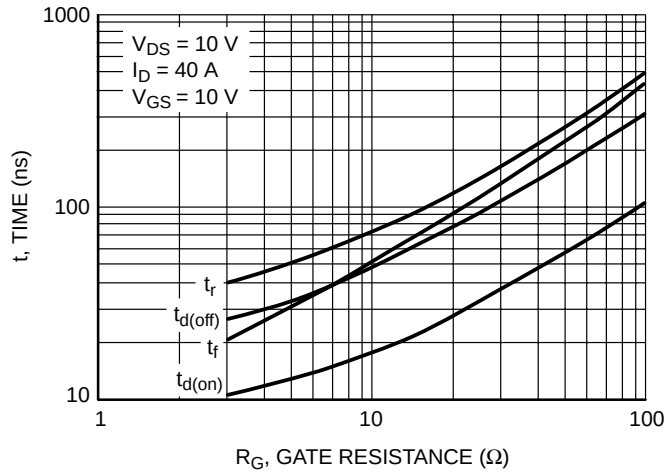


Figure 9. Resistive Switching Time Variation versus Gate Resistance

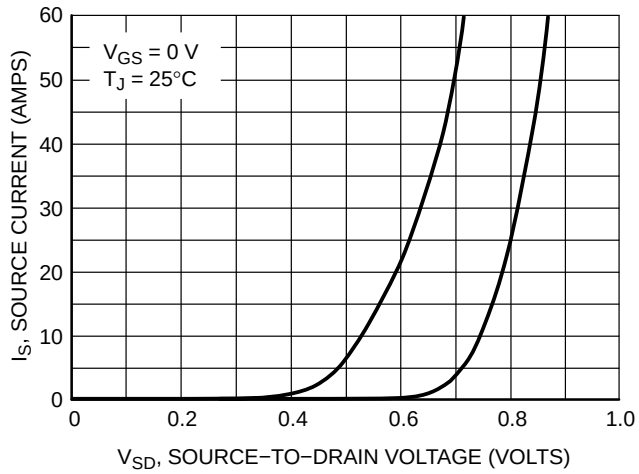


Figure 10. Diode Forward Voltage versus Current

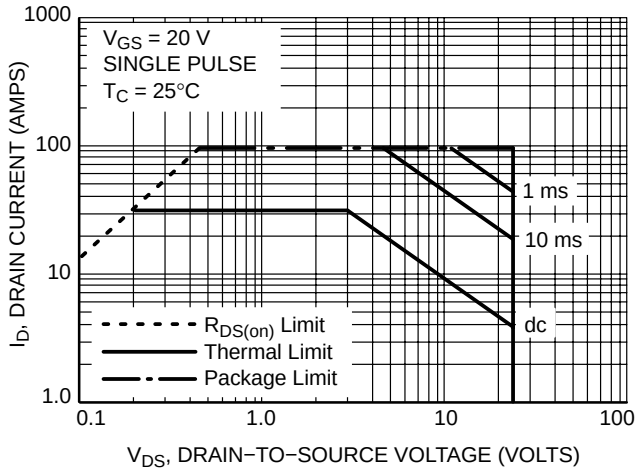


Figure 11. Maximum Rated Forward Biased Safe Operating Area

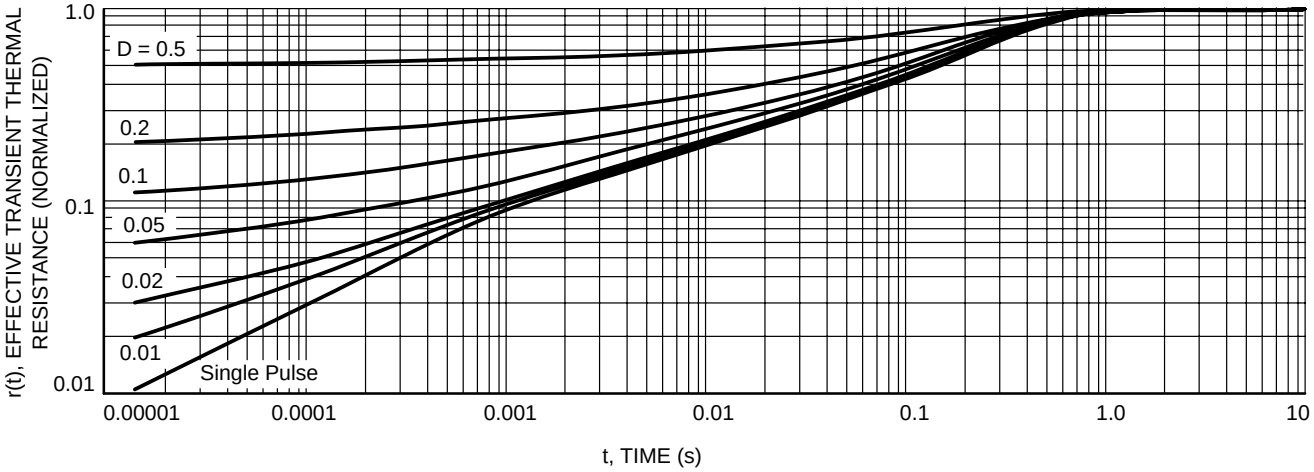
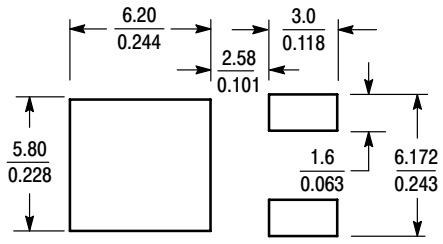


Figure 12. Thermal Response

INFORMATION FOR USING THE DPAK SURFACE MOUNT PACKAGE

RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

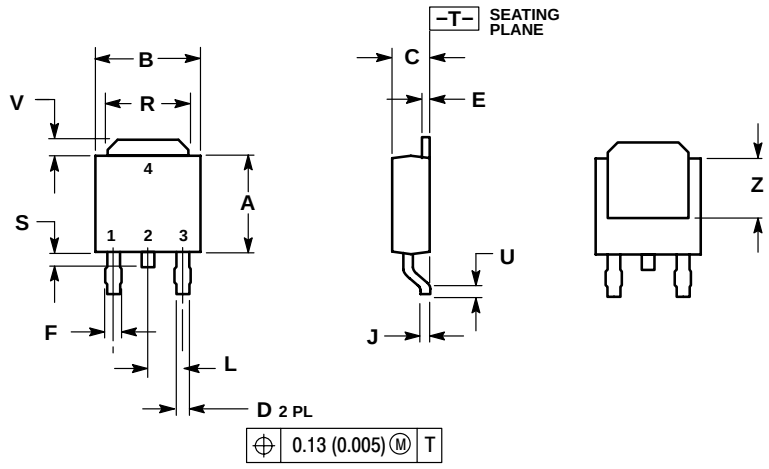
Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

PACKAGE DIMENSIONS

DPAK
CASE 369AA−01
ISSUE O



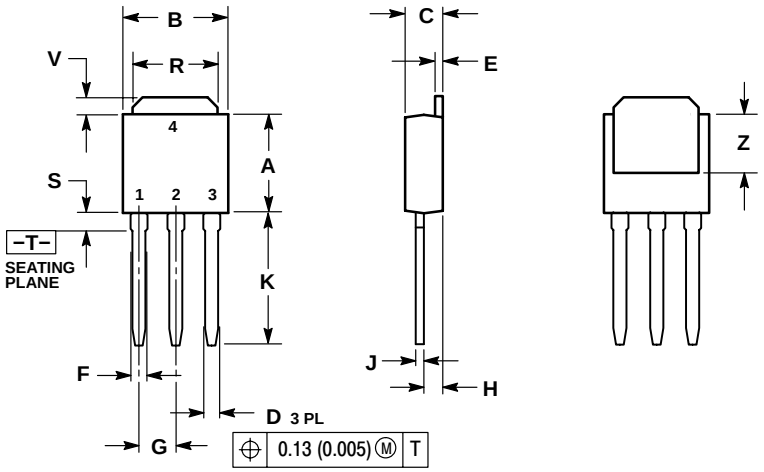
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.025	0.035	0.63	0.88
E	0.018	0.024	0.46	0.61
F	0.033	0.045	0.83	1.14
J	0.018	0.023	0.46	0.58
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

PACKAGE DIMENSIONS

DPAK
CASE 369D−01
ISSUE O



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D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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NTD110N02R/D