NSB1706DMW5T1

Dual Bias Resistor Transistor

NPN Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base−emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. In the NSB1706DMW5T1, two BRT devices are housed in the SC−88A package which is ideal for low power surface mount applications where board space is at a premium.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count

MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted, common for Q_1 and Q_2)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

THERMAL CHARACTERISTICS

Characteristic (One Junction Heated)	Symbol	Max	Unit
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	187 (Note 1) 256 (Note 2) 1.5 (Note 1) 2.0 (Note 2)	mW mW/°C
Thermal Resistance − Junction-to-Ambient	$R_{\theta JA}$	670 (Note 1) 490 (Note 2)	°C/W
Characteristic (Both Junctions Heated)	**Symbol**	**Max**	**Unit**
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	250 (Note 1) 385 (Note 2) 2.0 (Note 1) 3.0 (Note 2)	mW mW/°C
Thermal Resistance − Junction-to-Ambient	$R_{\theta JA}$	493 (Note 1) 325 (Note 2)	°C/W
Thermal Resistance − Junction-to-Lead	$R_{\theta JL}$	188 (Note 1) 208 (Note 2)	°C/W
Junction and Storage Temperature	T_J, T_{stg}	−55 to +150	°C

1. FR−4 @ Minimum Pad.
2. FR−4 @ 1.0 x 1.0 inch Pad.

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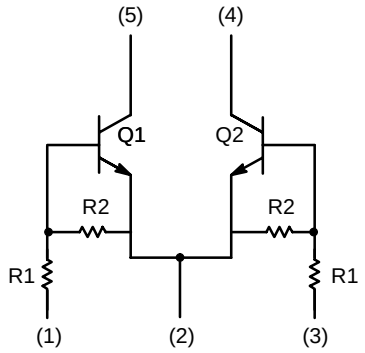
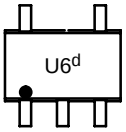


MARKING DIAGRAM



SC−88A
CASE 419A
STYLE 1

U6 = Device Marking
d = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
NSB1706DMW5T1	SC−88A	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted, common for Q_1 and Q_2)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Base Cutoff Current (V_{CB} = 50 V, I_E = 0)	I_{CBO}	−	−	100	nAdc
Collector-Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)	I_{CEO}	−	−	500	nAdc
Emitter-Base Cutoff Current (V_{EB} = 6.0 V, I_C = 0)	I_{EBO}	−	−	0.18	mAdc
Collector-Base Breakdown Voltage (I_C = 10 μA, I_E = 0)	$V_{(BR)CBO}$	50	−	−	Vdc
Collector-Emitter Breakdown Voltage (Note 4) (I_C = 2.0 mA, I_B = 0)	$V_{(BR)CEO}$	50	−	−	Vdc
ON CHARACTERISTICS (Note 4)					
DC Current Gain (V_{CE} = 10 V, I_C = 5.0 mA)	h_{FE}	80	200	−	
Collector-Emitter Saturation Voltage (I_C = 10 mA, I_B = 1 mA)	$V_{CE(sat)}$	−	−	0.25	Vdc
Output Voltage (on) (V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kΩ)	V_{OL}	−	−	0.2	Vdc
Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.25 V, R_L = 1.0 kΩ)	V_{OH}	4.9	−	−	Vdc
Input Resistor	R1	3.3	4.7	6.1	kΩ
Resistor Ratio	R1/R2	0.055	0.1	0.185	

3. New resistor combinations. Updated curves to follow in subsequent data sheets.
4. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%.

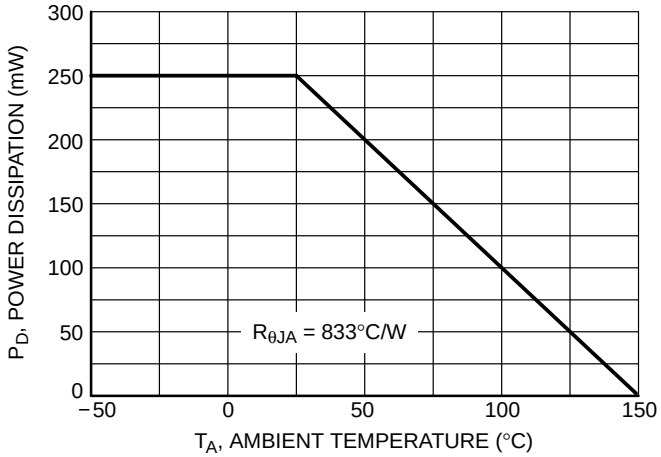
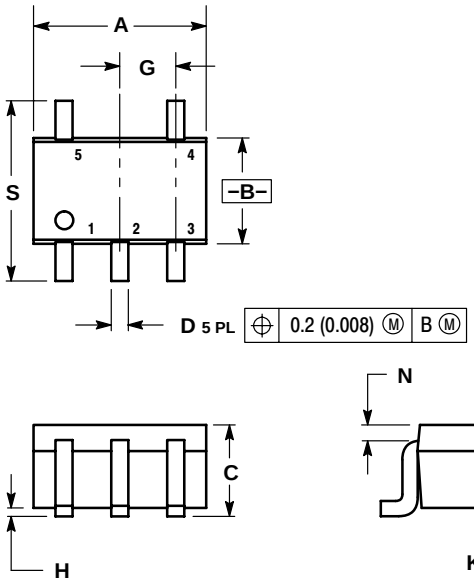


Figure 1. Derating Curve

PACKAGE DIMENSIONS

SC−88A
CASE 419A−02
ISSUE F

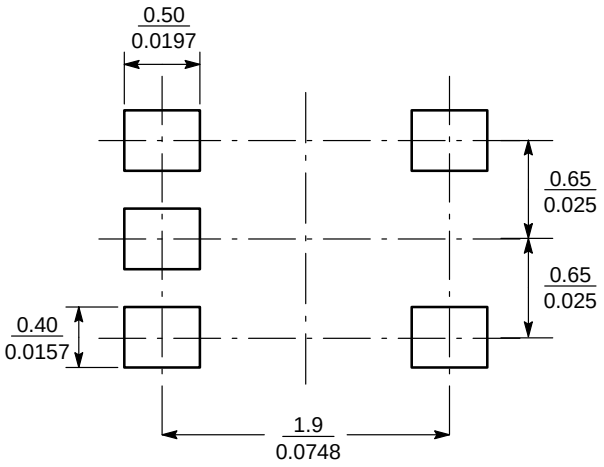


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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