NLAS4717

Product Preview

Low Voltage Dual SPDT Analog Switch

The NLAS4717 is an advanced CMOS analog switch fabricated in Sub−micron silicon gate CMOS technology. The device is a dual Independent Single Pole Double Throw (SPDT) switch featuring two Low R_{ON} of 4.5 Ω at 2.7 V.

The part also features guaranteed Break Before Make switching, assuring the switches never short the driver.

The NLAS4717 is available in a 2.0 x 1.5 mm bumped die array, with a 4 x 3 arrangement of solder bumps. The pitch of the solder bumps is 0.5 mm for easy handling.

Features

- Low R_{ON}, < 4.5 Ω at 2.7 V
- Threshold Adjusted to Function with 1.8 V Control at Supply = 2.7−3.3 V
- Single Supply Operation from 1.8−5.5 V
- Tiny 2.0 x 1.5 mm Bumped Die
- Low Crosstalk, < −80 dB at 10 mHz
- Full 0−V_{CC} Signal Handling Capability
- High Isolation, −55 dB at 10 mHz
- Low Standby Current, < 50 nA
- Low Distortion, < 0.03% THD
- R_{ON} Flatness of 1.2 Ω
- Pin for Pin Replacement for MAX4717

Applications

- Cell Phone
- Speaker Switching
- Power Switching (Up to 100 mA)
- Modems
- Automotive

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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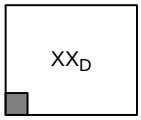
A1

Microbump−10
CASE 489AA

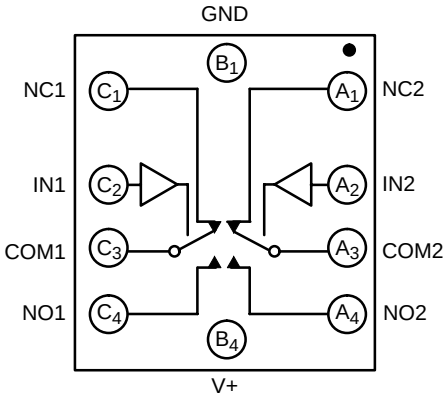
MARKING DIAGRAM



XX = Device Code
D = Date Code

PIN CONNECTIONS AND LOGIC DIAGRAM

(Top View)



FUNCTION TABLE

IN 1, 2	NO 1, 2	NC 1, 2
0	OFF	ON
1	ON	OFF

ORDERING INFORMATION

Device	Package	Shipping
NLAS4717	Microbump−10	3000/Tape & Reel

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V+	Positive DC Supply Voltage	−0.5 to +7.0	V
V_{IS}	Analog Input Voltage (V_{NO}, V_{NC}, or V_{COM}) (Note 1)	$-0.5 \le V_{IS} \le V_{CC} + 0.5$	V
V_{IN}	Digital Select Input Voltage	$-0.5 \le V_I \le +7.0$	V
I_{IK}	DC Current, Into or Out of Any Pin	±50	mA

1. Signal voltage on NC, NO, and COM exceeding VCC or GND are clamped by the internal diodes. Limit forward diode current to maximum current rating.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V+	DC Supply Voltage		1.8	5.5	V
V_{IN}	Digital Select Input Voltage		GND	5.5	V
V_{IS}	Analog Input Voltage (NC, NO, COM)		GND	V_{CC}	V
T_A	Operating Temperature Range		−55	+125	°C
t_r, t_f	Input Rise or Fall Time, SELECT	V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	0 0	100 20	ns/V

DC CHARACTERISTICS − Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} ±10%	Guaranteed Limit			Unit
				−55°C to 25°C	<85°C	<125°C	
V_{IH}	Minimum High−Level Input Voltage, Select Inputs		2.0 2.5 3.0 5.0	1.4 1.4 1.4 2.0	1.4 1.4 1.4 2.0	1.4 1.4 1.4 2.0	V
V_{IL}	Maximum Low−Level Input Voltage, Select Inputs		2.0 2.5 3.0 5.0	0.5 0.5 0.5 0.8	0.5 0.5 0.5 0.8	0.5 0.5 0.5 0.8	V
I_{IN}	Maximum Input Leakage Current, Select Inputs	V_{IN} = 5.5 V or GND	5.5	± 100	± 100	± 120	nA
I_{OFF}	Power Off Leakage Current	V_{IN} = 5.5 V or GND	0	±10	±10	±10	μA
I_{CC}	Maximum Quiescent Supply Current	Select and V_{IS} = V_{CC} or GND	5.5	± 50	± 200	± 200	nA

DC ELECTRICAL CHARACTERISTICS − Analog Section

Symbol	Parameter	Condition	V_{CC} ±10%	Guaranteed Maximum Limit						Unit
				−55°C to 25°C		< 85°C		< 125°C		
				Min	Max	Min	Max	Min	Max	
R_{ON} (NC, NO)	"ON" Resistance (Note 2)	$V_{IN} \geq V_{IH}$ V_{IS} = GND to V_{CC} $I_{IN}I \leq 100$ mA	2.5 3.0 5.0	5.5 4.5 3.0	2.0	6.0 5.0 3.5	2.0	6.5 5.5 4.0	2.0	Ω
R_{FLAT} (NC, NO)	On−Resistance Flatness (Notes 2, 4)	I_{COM} = 100 mA V_{IS} = 0 to V_{CC}	2.5 3.0 5.0	1.2 1.2 1.2		1.5 1.5 1.5	 0.35	1.8 1.8 1.8		Ω
ΔR_{ON}	On−Resistance Match Between Channels (Notes 2 and 3)	V_{IS} = 1.3 V; I_{COM} = 100 mA V_{IS} = 1.5 V; I_{COM} = 100 mA V_{IS} = 2.8 V; I_{COM} = 100 mA	2.5 3.0 5.0		0.18 0.5 0.4 0.3		0.18 0.6 0.5 0.4		0.18 0.7 0.6 0.5	Ω
$I_{NC(OFF)}$ $I_{NO(OFF)}$	NC or NO Off Leakage Current (Figure 10)	$V_{IN} = V_{IL}$ or V_{IH} V_{NO} or V_{NC} = 1.0 V_{COM} = 4.5 V	5.5	−0.5	0.5	−1.0	1.0	−10	10	nA
$I_{COM(ON)}$	COM ON Leakage Current (Figure 10)	$V_{IN} = V_{IL}$ or V_{IH} V_{NO} 1.0 V or 4.5 V with V_{NC} floating or V_{NC} 1.0 V or 4.5 V with V_{NO} floating V_{COM} = 1.0 V or 4.5 V	5.5	−1.0	1.0	−2.0	2.0	−3.0	3	nA

2. Guaranteed by design. Resistance measurements do not include test circuit or package resistance.
3. $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$ between all switches.
4. Flatness is defined as the difference between the maximum and minimum value of on−resistance as measured over the specified analog signal ranges.

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Conditions	V+ ±10% (V)	V_{IS} (V)	Guaranteed Maximum Limit							Unit
					−55°C to 25°C			<85°C		<125°C		
					Min	Typ*	Max	Min	Max	Min	Max	
t_{ON}	Turn−On Time	R_L = 50 Ω, C_L = 35 pF (Figures 2 and 3)	2.5	1.3		100	55	120	65	140	70	ns
			3.0	1.5		80		100		120		
			5.0	2.8		80	30	100	35	120	35	
t_{OFF}	Turn−Off Time	R_L = 50 Ω, C_L = 35 pF (Figures 2 and 3)	2.5	1.3		60	55	70	65	80	70	ns
			3.0	1.5		40		50		60		
			5.0	2.8		40	25	50	30	60	30	
t_{BBM}	Minimum Break−Before−Make Time	V_{IS} = 3.0 R_L = 300 Ω, C_L = 35 pF (Figure 1)	3.0	1.5	1.0	8.0						ns

		V+ = 3.0 V	
C_{NC} Off	NC Off Capacitance, f = 1 MHz	9	pF
C_{NO} Off	NO Off Capacitance, f = 1 MHz	9	
C_{NC} On	NC On Capacitance, f = 1 MHz	15	
C_{NO} On	NO On Capacitance, f = 1 MHz	15	

*Typical Characteristics are at 25°C.

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted) (Note 6)

Symbol	Parameter	Condition	V+ V	Typical 25°C	Unit
BW	Maximum On−Channel −3dB Bandwidth or Minimum Frequency Response	V_{IN} = 0 dBm NC/NO V_{IN} centered between V_{CC} and GND (Figure 4)	3.0	300	MHz
V_{ONL}	Maximum Feedthrough On Loss	V_{IN} = 0 dBm @ 100 kHz to 50 MHz V_{IN} centered between V_{CC} and GND (Figure 4)	3.0	−0.05	dB
V_{ISO}	Off−Channel Isolation	f = 10 mHz; V_{IS} = 1 V RMS; C_L = 5 nF V_{IN} centered between V_{CC} and GND (Figure 4)	3.0	−55	dB
Q	Charge Injection Select Input to Common I/O	V_{IN} = V_{CC} to GND, R_{IS} = 0 Ω, C_L = 1 nF $Q = C_L \cdot \Delta V_{OUT}$ (Figure 5)	3.0 5.0	5.0 10	pC
THD	Total Harmonic Distortion THD + Noise	F_{IS} = 20 Hz to 20 kHz, R_L = Rgen = 600 Ω, C_L = 50 pF V_{IS} = 1 V RMS	3.0	0.03	%
VCT	Channel−to−Channel Crosstalk	f = 10 mHz; V_{IS} = 1 V RMS, C_L = 5 pF, R_L = 50 Ω V_{IN} centered between V_{CC} and GND (Figure 4)	3.0	−80	dB

5. Off−Channel Isolation = 20log10 (Vcom/Vno), Vcom = output, Vno = input to off switch.
6. −40°C specifications are guaranteed by design.

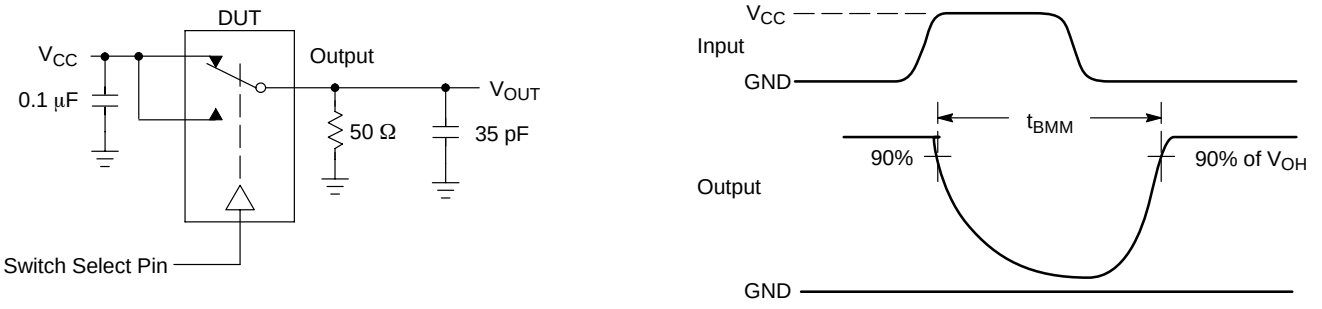


Figure 1. t_{BBM} (Time Break−Before−Make)

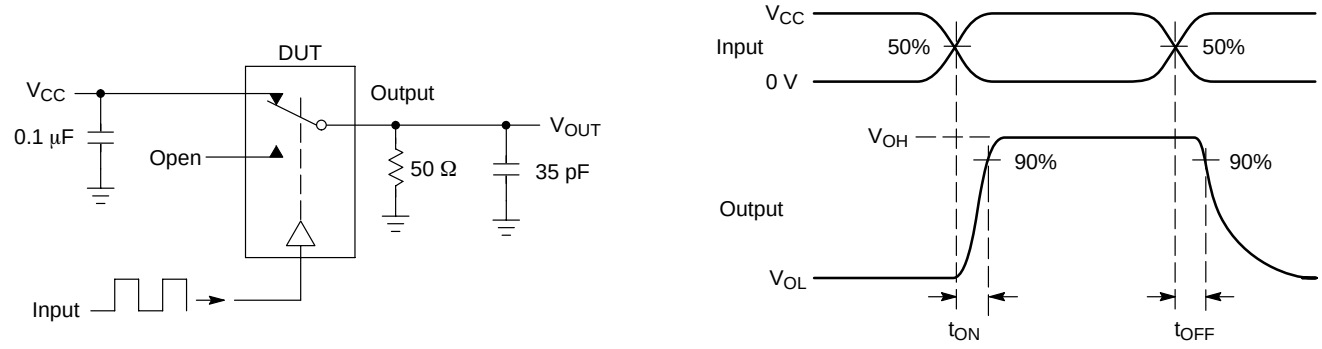


Figure 2. t_{ON}/t_{OFF}

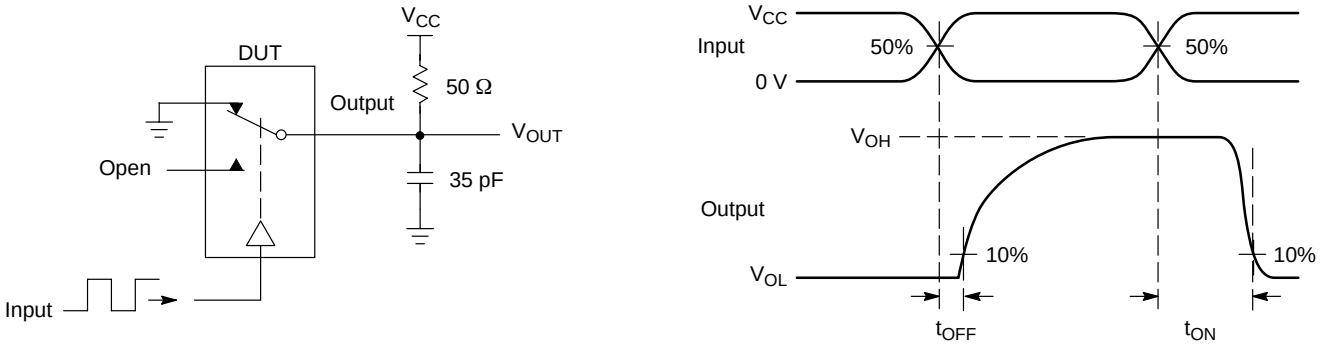
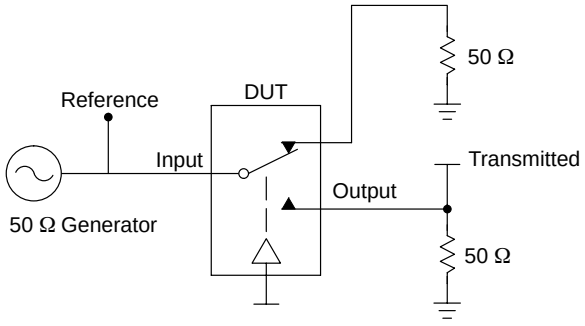


Figure 3. t_{ON}/t_{OFF}



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO}, Bandwidth and V_{ONL} are independent of the input signal direction.

V_{ISO} = Off Channel Isolation = 20 Log $\left(\frac{V_{OUT}}{V_{IN}}\right)$ for V_{IN} at 100 kHz

V_{ONL} = On Channel Loss = 20 Log $\left(\frac{V_{OUT}}{V_{IN}}\right)$ for V_{IN} at 100 kHz to 50 MHz

Bandwidth (BW) = the frequency 3 dB below V_{ONL}
V_{CT} = Use V_{ISO} setup and test to all other switch analog input/outputs terminated with 50 Ω

Figure 4. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/V_{ONL}

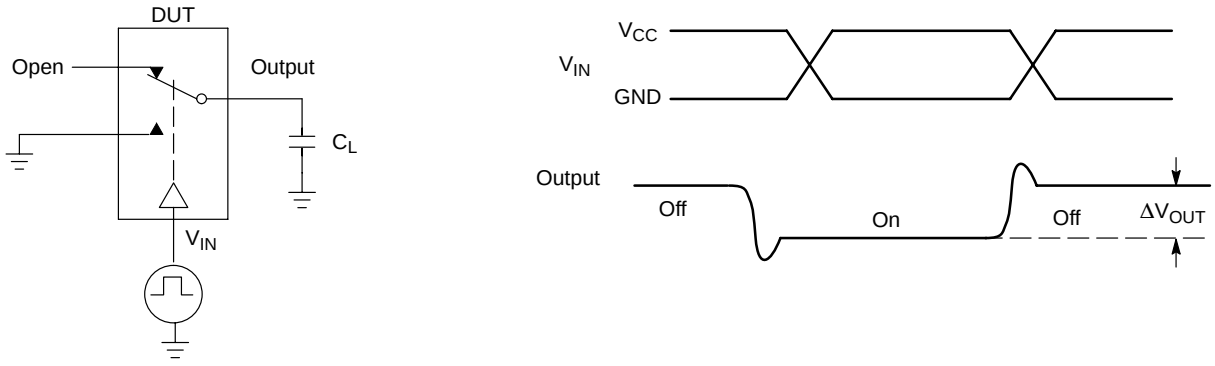


Figure 5. Charge Injection: (Q)

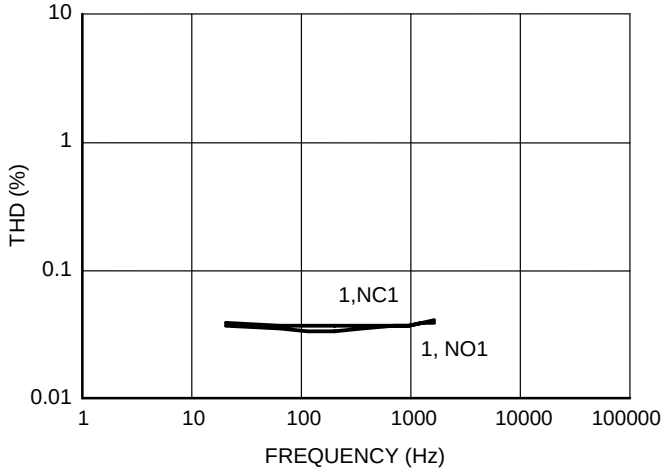


Figure 6. Total Harmonic Distortion Plus Noise versus Frequency

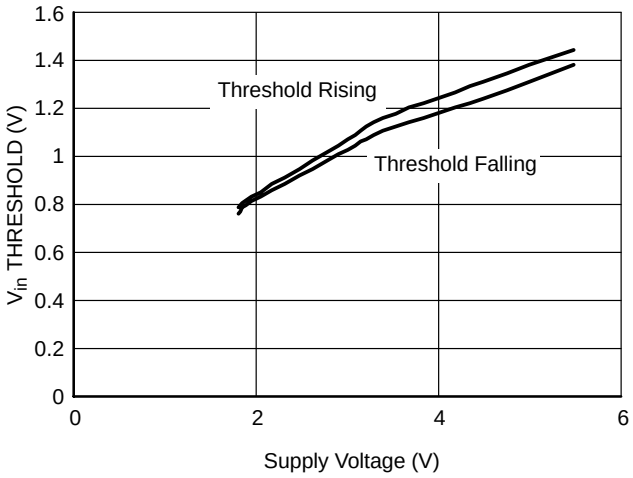


Figure 7. Voltage in Threshold on Logic Pins

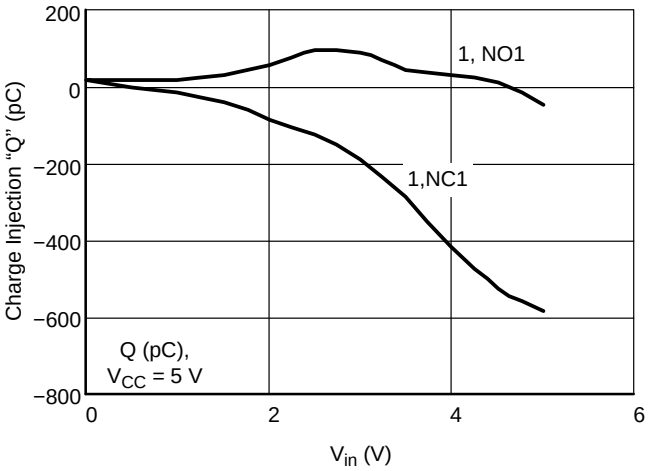


Figure 8. Charge Injection versus V_{is}

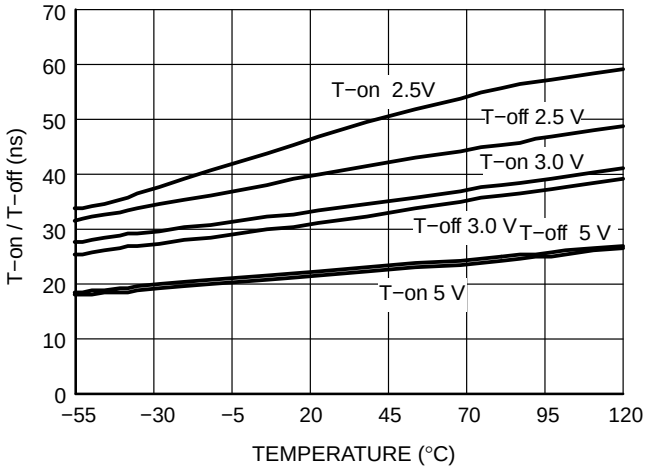


Figure 9. T−on/T−off Time versus Temperature

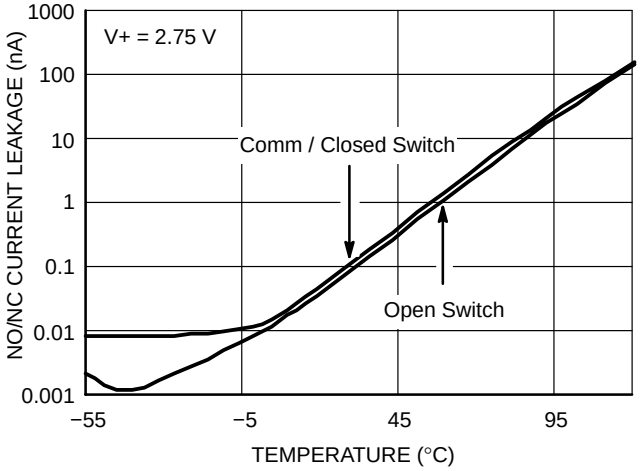


Figure 10. NO/NC Current Leakage Off and On, V_{CC} = 5 V

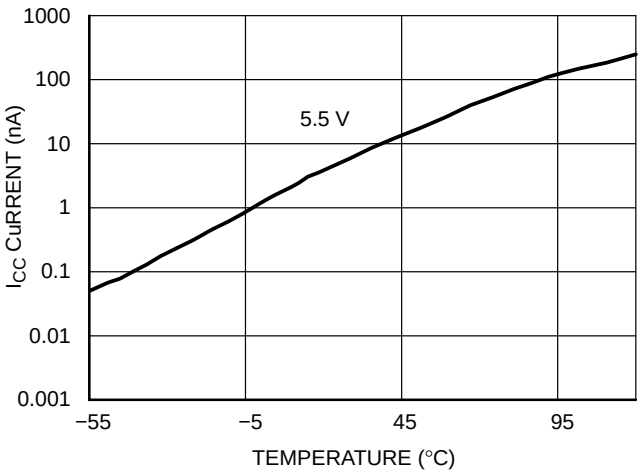


Figure 11. I_{CC} Current Leakage versus Temperature V_{CC} = 5.5 V

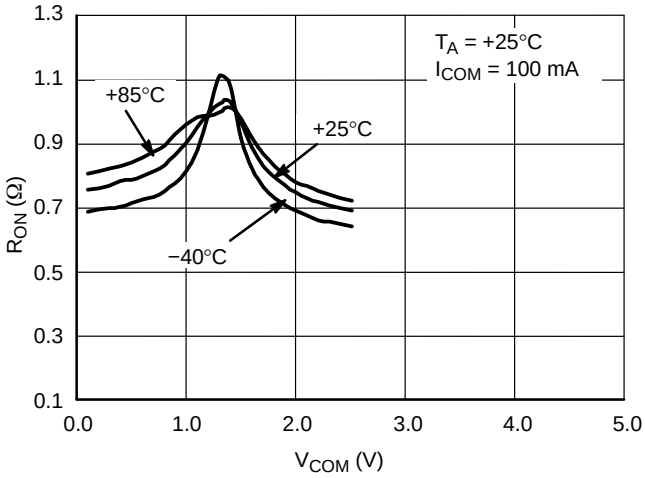


Figure 12. NC/NO On−Resistance versus COM Voltage

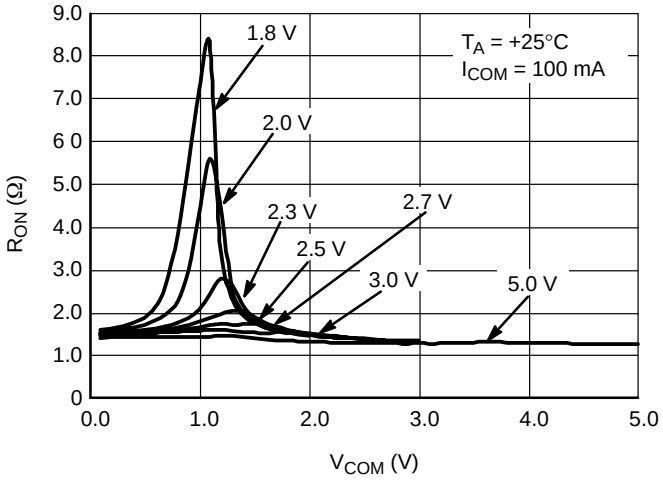


Figure 13. NC/NO On−Resistance versus COM Voltage

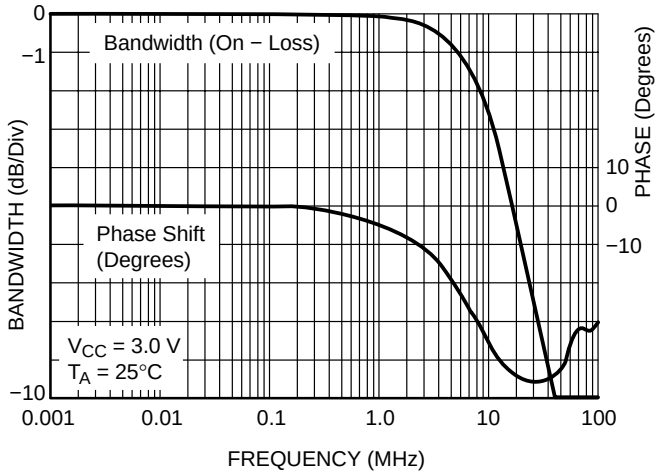


Figure 14. NC/NO Bandwidth and Phase Shift versus Frequency

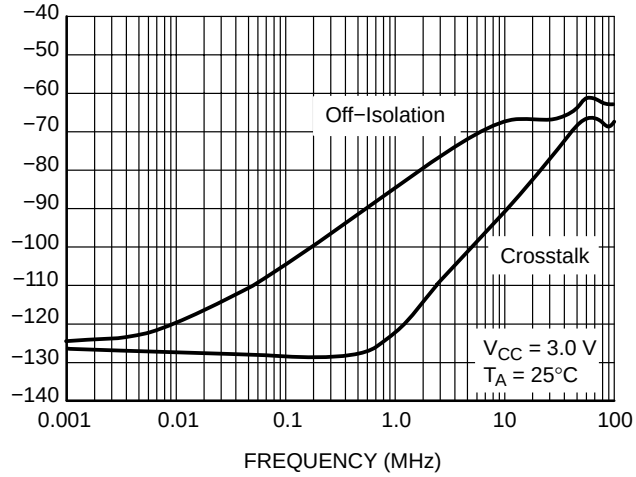


Figure 15. NC/NO Off Isolation and Crosstalk

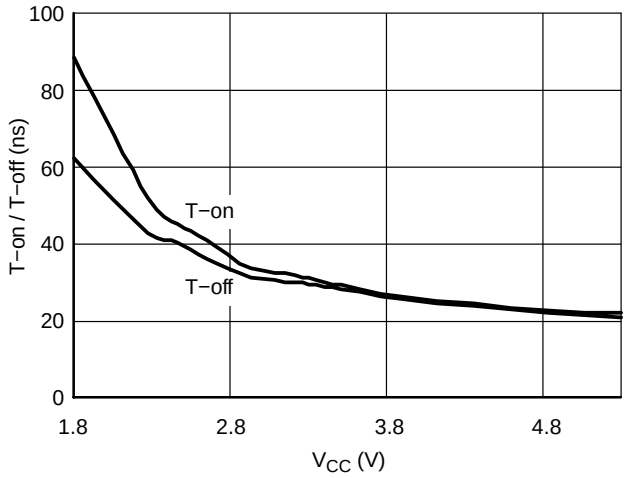


Figure 16. T−on/T−off versus V_{CC}

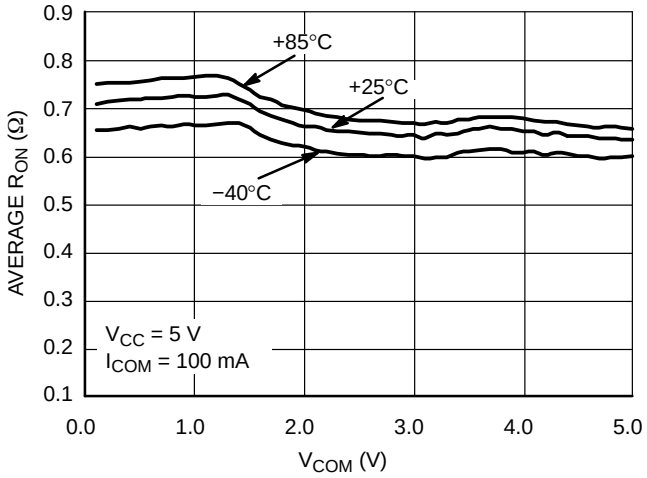


Figure 17. NC/NO On−Resistance versus COM Voltage

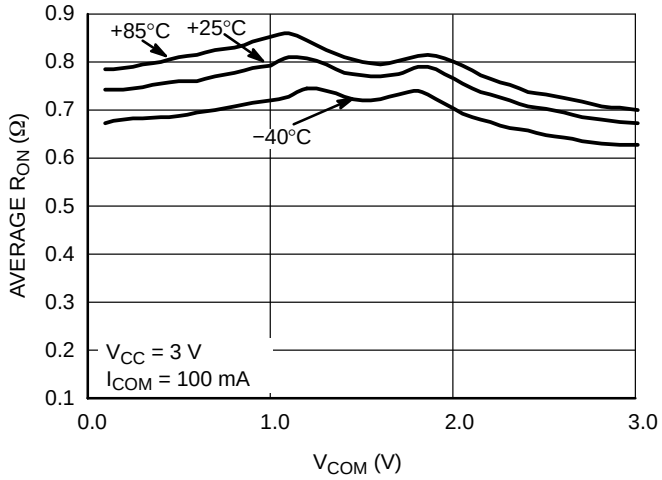
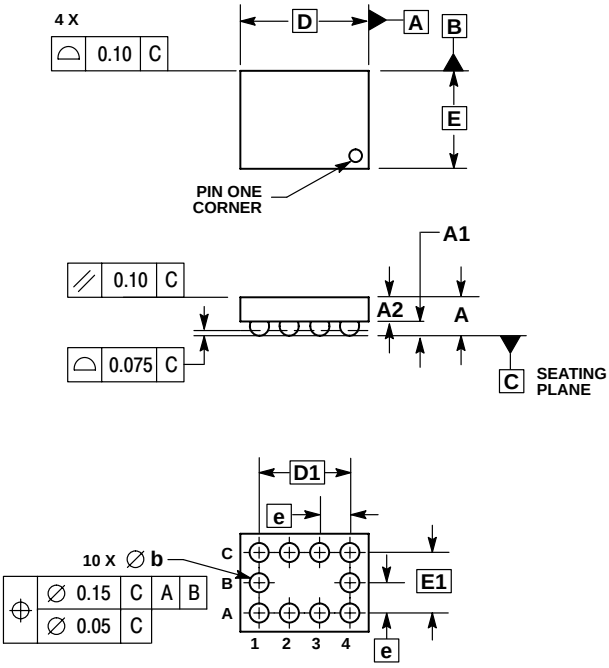


Figure 18. NC/NO On−Resistance versus COM Voltage

PACKAGE DIMENSIONS

Microbump−10
CASE 489AA−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.650
A1	0.210	0.270
A2	0.280	0.380
D	1.965 BSC	
E	1.465 BSC	
b	0.250	0.350
e	0.500 BSC	
D1	1.500 BSC	
E1	1.000 BSC	

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