NL27WZ07

Dual Buffer with Open Drain Outputs

The NL27WZ07 is a high performance dual buffer with open drain outputs operating from a 1.65 to 5.5 V supply.

The internal circuit is composed of multiple stages, including an open drain output which provides the capability to set output switching level. This allows the NL27WZ07 to be used to interface 5 V circuits to circuits of any voltage between V_{CC} and 7 V using an external resistor and power supply.

- Extremely High Speed: t_{PD} 2.3 ns (typical) at V_{CC} = 5 V
- Designed for 1.65 V to 5.5 V V_{CC} Operation, CMOS compatible
- Over Voltage Tolerant Inputs
- LVTTL Compatible − Interface Capability with 5 V TTL Logic with V_{CC} = 3 V
- LVCMOS Compatible
- 24 mA Output Sink Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
- Chip Complexity: FET = 72; Equivalent Gate = 18
- Pb−Free Package May be Available. The G−Suffix Denotes a Pb−Free Lead Finish

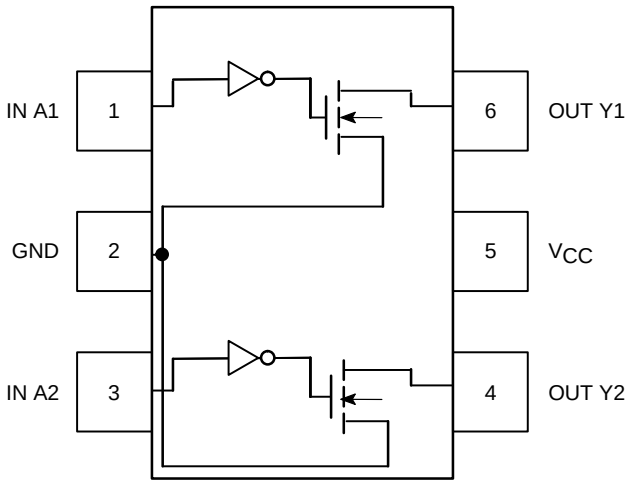

Figure 1. Pinout (Top View)

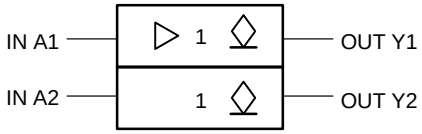

Figure 2. Logic Symbol

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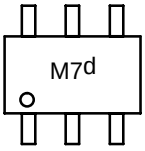
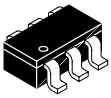
MARKING DIAGRAMS

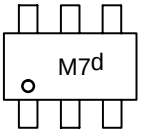
SC−88 (SOT−363)
DF SUFFIX
CASE 419B



Pin 1
d = Date Code



TSOP−6
DT SUFFIX
CASE 318G



Pin 1
d = Date Code

PIN ASSIGNMENT

1	IN A1
2	GND
3	IN A2
4	OUT Y2
5	V_{CC}
6	OUT Y1

FUNCTION TABLE

A Input	Y Output
L	L
H	Z

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MAXIMUM RATINGS (Note 1)

Symbol	Characteristics		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +7.0	V
V_I	DC Input Voltage		$-0.5 \le V_I \le +7.0$	V
V_O	DC Output Voltage	Output in Z or LOW State (Note 2)	$-0.5 \le V_O \le 7.0$	V
I_{IK}	DC Input Diode Current	V_I < GND	−50	mA
I_{OK}	DC Output Diode Current	V_O < GND	−50	mA
I_O	DC Output Sink Current		±50	mA
I_{CC}	DC Supply Current per Supply Pin		±100	mA
I_{GND}	DC Ground Current per Ground Pin		±100	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
P_D	Power Dissipation in Still Air	SC−88, TSOP−6	200	mW
θ_{JA}	Thermal Resistance	SC−88, TSOP−6	333	°C/W
T_L	Lead Temperature, 1 mm from case for 10 s		260	°C
T_J	Junction Temperature under Bias		+150	°C
$I_{Latch-Up}$	Latch−Up Performance	Above V_{CC} and Below GND at 85°C (Note 6)	±500	mA
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Classification	Human Body Model (Note 4) Machine Model (Note 5) Charged Device Model (Note 6)	> 2000 > 200 N/A	

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute−maximum−rated conditions is not implied.
2. I_O absolute maximum rating must be observed.
3. Tested to EIA/JESD22−A114−A, rated to EIA/JESD22−A114−B.
4. Tested to EIA/JESD22−A115−A, rated to EIA/JESD22−A115−A.
5. Tested to JESD22−C101−A
6. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage	Operating Data Retention Only	1.65 1.5	5.5 5.5	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	(Z or LOW State)	0	5.5	V
T_A	Operating Free−Air Temperature		−40	+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate	V_{CC} = 2.5 V ±0.2 V V_{CC} =3.0 V ±0.3 V V_{CC} =5.0 V ±0.5 V	0 0 0	20 10 5	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			−40°C ≤ T_A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High−Level Input Voltage		1.65 to 1.95 2.3 to 5.5	0.75 V_{CC} 0.75 V_{CC}			0.75 V_{CC} 0.75 V_{CC}		V
V_{IL}	Low−Level Input Voltage		1.65 to 1.95 2.3 to 5.5			0.3 V_{CC} 0.3 V_{CC}		0.3 V_{CC} 0.3 V_{CC}	V
I_{LKG}	Z−State Output Leakage Current	V_{IN} = V_{IL} V_{OUT} = V_{CC} or GND	2.3 to 5.5			±5.0		±10.0	μA
V_{OL}	Low−Level Output Voltage V_{IN} = V_{IL}	I_{OL} = 100 μA	1.65 to 5.5		0.0	0.1		0.1	V
		I_{OL} = 4 mA	1.65		0.08	0.24		0.24	
		I_{OL} = 8 mA	2.3		0.20	0.3		0.3	
		I_{OL} = 12 mA	2.7		0.22	0.4		0.4	
		I_{OL} = 16 mA	3.0		0.28	0.4		0.4	
		I_{OL} = 24 mA	3.0		0.38	0.55		0.55	
		I_{OL} = 32 mA	4.5		0.42	0.55		0.55	
I_{IN}	Input Leakage Current	V_{IN} or V_{OUT} = V_{CC} or GND	0 to 5.5			±0.1		±1.0	μA
I_{OFF}	Power Off−Output Leakage Current	V_{OUT} = 5.5 V	0			1		10	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5			1		10	μA

AC ELECTRICAL CHARACTERISTICS t_R = t_F = 2.5 ns; C_L = 50 pF; R_L = 500 Ω

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			−40°C ≤ T_A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PZL}	Propagation Delay (Figure 3 and 4)	R_L = R_1= 5000 Ω, C_L = 15 pF	1.8 ± 0.15	1.8	5.3	11.5	1.8	12.0	ns
		R_L = R_1= 500 Ω, C_L = 50 pF	2.5 ± 0.2	1.2	3.7	5.8	1.2	6.4	
			3.3 ± 0.3	0.8	2.9	4.4	0.8	4.8	
			5.0 ± 0.5	0.5	2.3	3.5	0.5	3.9	
t_{PLZ}	Propagation Delay (Figure 3 and 4)	R_L = R_1= 5000 Ω, C_L = 15 pF	1.8 ± 0.15	1.8	5.3	11.5	1.8	12.0	ns
		R_L = R_1= 500 Ω, C_L = 50 pF	2.5 ± 0.2	1.2	2.8	5.8	1.2	6.4	
			3.3 ± 0.3	0.8	2.1	4.4	0.8	4.8	
			5.0 ± 0.5	0.5	1.4	3.5	0.5	3.9	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	V_{CC} = 5.5 V, V_I = 0 V or V_{CC}	2.5	pF
C_{OUT}	Output Capacitance	V_{CC} = 5.5 V, V_I = 0 V or V_{CC}	4.0	pF
C_{PD}	Power Dissipation Capacitance (Note 7)	10 MHz, V_{CC} = 5.5 V, V_I = 0 V or V_{CC}	4.0	pF

7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

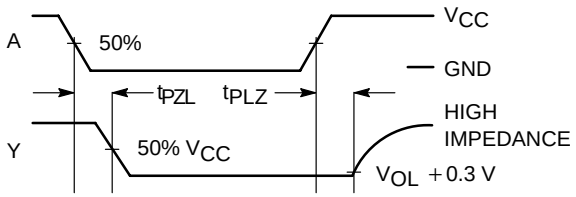
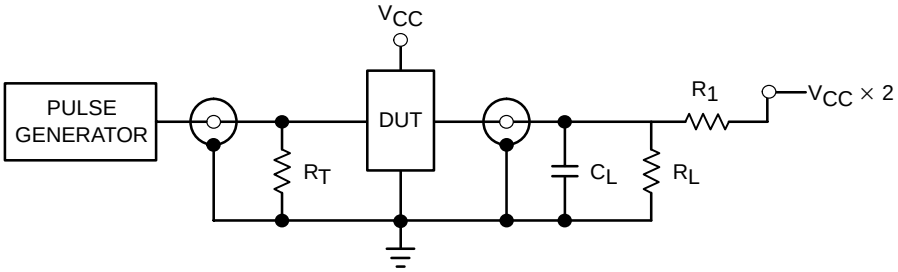


Figure 3. Switching Waveforms



R_T = Z_{OUT} of pulse generator (typically 50 Ω)

Figure 4. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature							Package Type (Name/SOT#/ Common Name)	Tape and Reel Size†
	Logic Circuit Indicator	No. of Gates per Package	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
NL27WZ07DFT2	NL	2	7	WZ	07	DF	T2	SC−88 / SOT−363 / SC−70	178 mm (7”) 3000 Unit
NL27WZ07DTT1	NL	2	7	WZ	07	DT	T1	TSOP−6 / SOT−23 / SC−59	178 mm (7”) 3000 Unit
NL27WZ07DTT1G	NL	2	7	WZ	07	DT	T1	TSOP−6 / SOT−23 / SC−59 (Pb−Free)	178 mm (7”) 3000 Unit

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

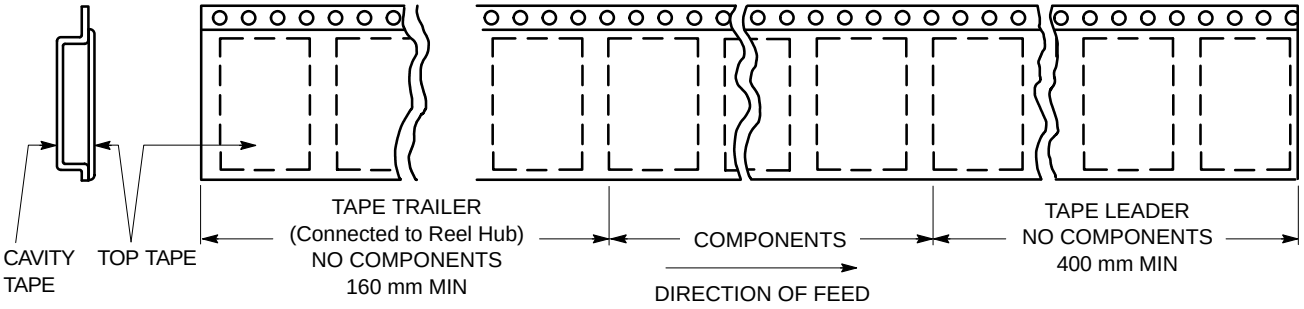


Figure 5. Tape Ends for Finished Goods

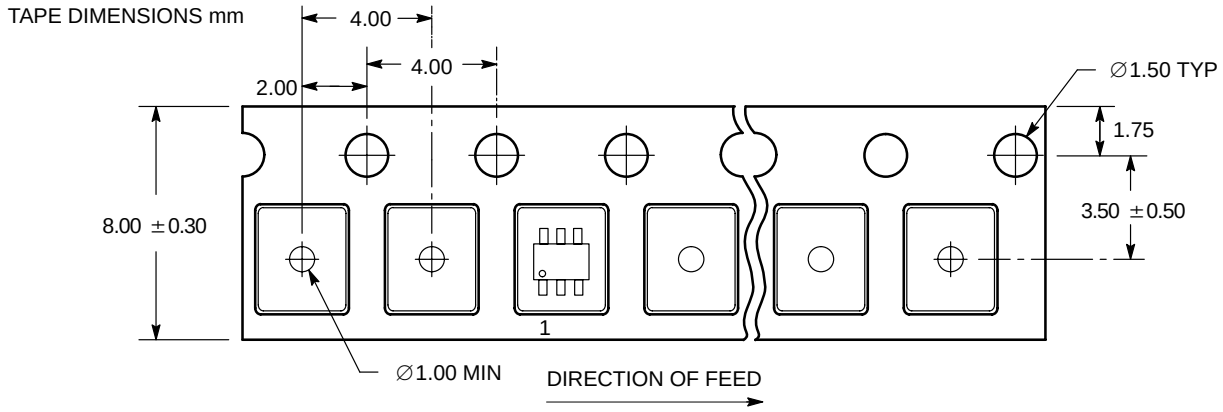


Figure 6. SC70−6/SC−88/SOT−363 DFT2 and SOT23−6/TSOP−6/SC59−6 DTT1 Reel Configuration/Orientation

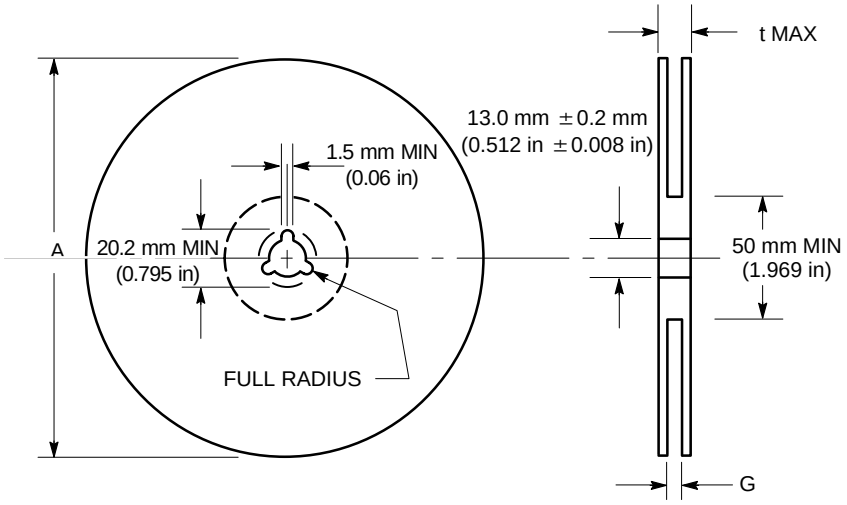


Figure 7. Reel Dimensions

REEL DIMENSIONS

Tape Size	T and R Suffix	A Max	G	t Max
8 mm	T1, T2	178 mm (7 in)	8.4 mm, + 1.5 mm, −0.0 (0.33 in + 0.059 in, −0.00)	14.4 mm (0.56 in)

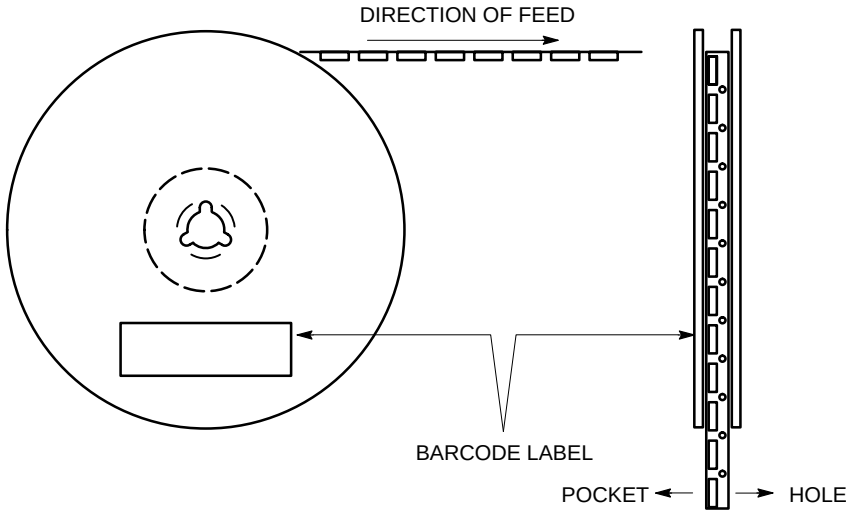
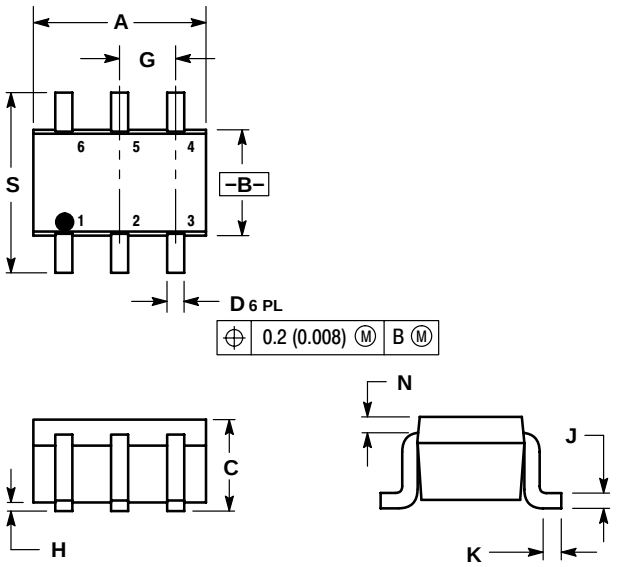


Figure 8. Reel Winding Direction

PACKAGE DIMENSIONS

SC−88 (SOT−363)
DF SUFFIX
CASE 419B−02
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419B−01 OBSOLETE, NEW STANDARD 419B−02.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	−−−	0.004	−−−	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

SOLDERING FOOTPRINT*

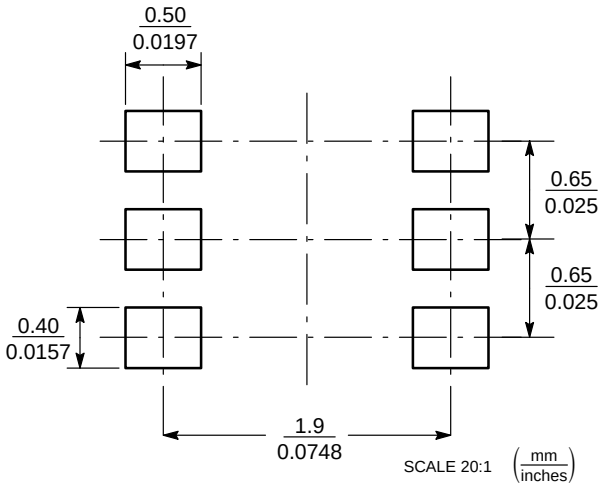
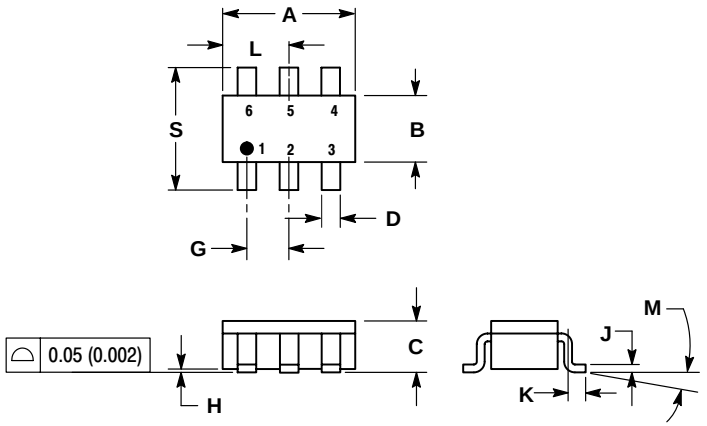


Figure 9. SC−88/SC70−6

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

TSOP−6
DT SUFFIX
CASE 318G−02
ISSUE K



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0	10	0	10
S	2.50	3.00	0.0985	0.1181

SOLDERING FOOTPRINT*

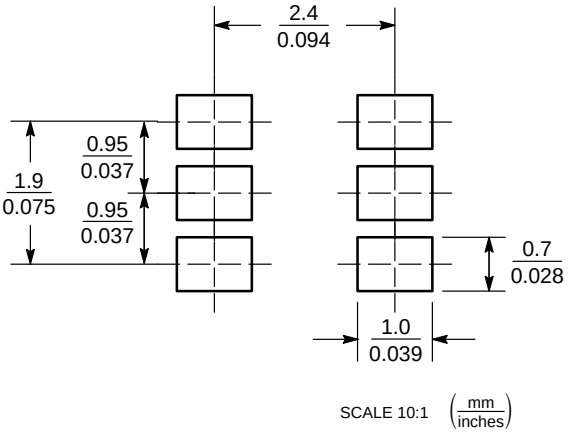


Figure 10. TSOP−6

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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