Non-Inverting 3-State Buffer

The NL17SZ125 is a high performance noninverting buffer operating from a 1.65 V to 5.5 V supply.

- Extremely High Speed: t_{PD} 2.6 ns (typical) at $V_{CC} = 5.0 \text{ V}$
- Designed for 1.65 V to 5.5 V V_{CC} Operation
- Over Voltage Tolerant Inputs and Outputs
- $\bullet~LVTTL$ Compatible Interface Capability With 5.0 V TTL Logic with $V_{CC}=3.0~V$
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
- 3-State OE Input is Active-Low
- Replacement for NC7SZ125
- Chip Complexity = 36 FETs

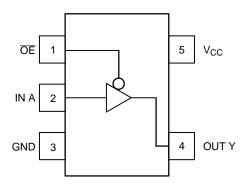


Figure 1. Pinout (Top View)



Figure 2. Logic Symbol

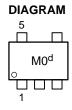


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SC70-5/SC-88A/SOT-353 DF SUFFIX CASE 419A



MARKING

d = Date Code

PIN ASSIGNMENT					
1	ŌĒ				
2	IN A				
3	GND				
4	OUT Y				
5	V_{CC}				

FUNCTION TABLE

OE Input	A Input	Y Output
L	L	L
L	Н	Н
Н	X	Z

X = Don't Care

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

MAXIMUM RATINGS

Symbol	Parame	ter	Value	Unit
V _{CC}	DC Supply Voltage		-0.5 to +7.0	V
V _{IN}	DC Input Voltage		-0.5 to +7.0	V
V _{OUT}	DC Output Voltage		-0.5 to +7.0	V
I _{IK}	DC Input Diode Current		-50	mA
I _{OK}	DC Output Diode Current		-50	mA
I _{OUT}	DC Output Sink Current		±50	mA
I _{CC}	DC Supply Current per Supply Pin		±100	mA
T _{STG}	Storage Temperature Range		-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 S	Seconds	260	°C
TJ	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 1)		350	°C/W
P _D	Power Dissipation in Still Air at 85°C		150	mW
MSL	Moisture Sensitivity		Level 1	
F _R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

- 1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace with no air flow.
- 2. Tested to EIA/JESD22-A114-A.
- 3. Tested to EIA/JESD22-A115-A.
- 4. Tested to JESD22-C101-A.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	1.65	5.5	V
V _{IN}	DC Input Voltage	0	5.5	V
V _{OUT}	DC Output Voltage	0	5.5	V
T _A	Operating Temperature Range	-40	+85	°C
t _r , t _f	Input Rise and Fall Time $V_{CC} = 1.8 \text{ V} \pm 0.15 \\ V_{CC} = 2.5 \text{ V} \pm 0.2 \\ V_{CC} = 3.0 \text{ V} \pm 0.3 \\ V_{CC} = 5.0 \text{ V} \pm 0.5$	V 0 V 0 V 0 V 0	20 20 10 5.0	ns/V

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

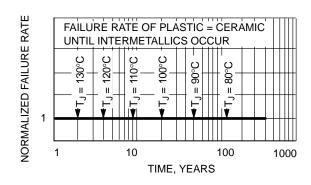


Figure 3. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

		V _{CC}	T,	4 = 25°($-40^{\circ}\text{C} \leq \text{T}_{\text{A}} \leq 85^{\circ}\text{C}$			
Symbol	Parameter	(V)	Min	Тур	Max	Min	Max	Unit	Condition
V _{IH}	High-Level Input Voltage	1.65 to 1.95 2.3 to 5.5	0.75 V _{CC} 0.7 V _{CC}			0.75 V _{CC} 0.7 V _{CC}		V	
V _{IL}	Low-Level Input Voltage	1.65 to 1.95 2.3 to 5.5			0.25 V _{CC} 0.3 V _{CC}		0.25 V _{CC} 0.3 V _{CC}	V	
V _{OH}	High-Level Output Voltage V _{IN} = V _{IH}	1.65 1.8 2.3 3.0 4.5	1.55 1.7 2.2 2.9 4.4	1.65 1.8 2.3 3.0 4.5		1.55 1.7 2.2 2.9 4.4		V	I _{OH} = -100 μA
		1.65 2.3 3.0 3.0 4.5	1.29 1.9 2.4 2.3 3.8	1.52 2.15 2.80 2.68 4.20		1.29 1.9 2.4 2.3 3.8		V	I _{OH} = -4 mA I _{OH} = -8 mA I _{OH} = -16 mA I _{OH} = -24 mA I _{OH} = -32 mA
V _{OL}	Low-Level Output Voltage V _{IN} = V _{IL}	1.65 1.8 2.3 3.0 4.5		0.0 0.0 0.0 0.0 0.0	0.1 0.1 0.1 0.1 0.1		0.1 0.1 0.1 0.1 0.1	V	I _{OL} = 100 μA
		1.65 2.3 3.0 3.0 4.5		0.08 0.10 0.15 0.22 0.22	0.24 0.30 0.40 0.55 0.55		0.24 0.30 0.40 0.55 0.55	V	I _{OL} = 4 mA I _{OL} = 8 mA I _{OL} = 16 mA I _{OL} = 24 mA I _{OL} = 32 mA
I _{IN}	Input Leakage Current	0 to 5.5			±1.0		±1.0	μΑ	$0 \text{ V} \leq \text{V}_{\text{IN}} \leq 5.5 \text{ V}$
I _{OZ}	3-State Output Leakage	1.65 to 5.5			±0.5		±5.0	μΑ	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $0 \text{ V} \leq V_{OUT} \leq 5.5 \text{ V}$
I _{OFF}	Power Off Leakage Current	0.0			1.0		10	μΑ	V _{IN} or V _{OUT} = 5.5 V
I _{CC}	Quiescent Supply Current	1.65 to 5.5			1.0		10	μΑ	V _{IN} = 5.5 V, GND

AC ELECTRICAL CHARACTERISTICS ($t_R = t_F = 3.0 \text{ ns}$)

				V _{CC}	T,	_{\(\)} = 25°	С	-40°C ≤	$T_A \leq 85^{\circ}C$	
Symbol	Parameter	Condi	tion	(V)	Min	Тур	Max	Min	Max	Unit
t _{PLH}	Propagation Delay	$R_L = 1 M\Omega$	$C_{L} = 15 \text{ pF}$	1.8 ± 0.15	2.0	9.0	10	2.0	10.5	ns
t _{PHL}	AN to YN (Figures 4 and 5, Table 1)	$R_L = 1 M\Omega$	$C_{L} = 15 \text{ pF}$	2.5 ± 0.2	1.0		7.5	1.0	8.0	
		R_L = 1 MΩ R_L = 500 Ω	$C_L = 15 pF$ $C_L = 50 pF$	3.3 ± 0.3	0.8 1.2		5.2 5.7	0.8 1.2	5.5 6.0	
		$R_L = 1 \text{ M}\Omega$ $R_L = 500 \Omega$	$C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$	5.0 ± 0.5	0.5 0.8		4.5 5.0	0.5 0.8	4.8 5.3	
t _{PZH}	Output Enable Time	$R_L = 250 \Omega$	$C_{L} = 50 \text{ pF}$	1.8 ± 0.15	2.0	7.6	9.5	2.0	10	ns
t _{PZL}	(Figures 6, 7and 8, Table 1)			2.5 ± 0.2	1.8		8.5	1.8	9.0	
				3.3 ± 0.3	1.2		6.2	1.2	6.5	
				5.0 ± 0.5	0.8		5.5	0.8	5.8	
t _{PHZ}	Output Disable Time	R _L and R ₁ = 500	Ω C _L = 50 pF	1.8 ± 0.15	2.0	8.0	10	2.0	10.5	ns
t _{PLZ}	(Figures 6, 7and 8, Table 1)			2.5 ± 0.2	1.5		8.0	1.5	8.5	
				3.3 ± 0.3	8.0		5.7	0.8	6.0	
				5.0 ± 0.5	0.3		4.7	0.3	5.0	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C _{IN}	Input Capacitance	$V_{CC} = 5.5 \text{ V}, V_I = 0 \text{ V or } V_{CC}$	2.5	pF
C _{OUT}	Output Capacitance	$V_{CC} = 5.5 \text{ V}, V_I = 0 \text{ V or } V_{CC}$	2.5	pF
C _{PD}	Power Dissipation Capacitance (Note 5)	10 MHz, $V_{CC} = 3.3 \text{ V}$, $V_I = 0 \text{ V or } V_{CC}$ 10 MHz, $V_{CC} = 5.5 \text{ V}$, $V_I = 0 \text{ V or } V_{CC}$	9 11	pF

^{5.} C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no–load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

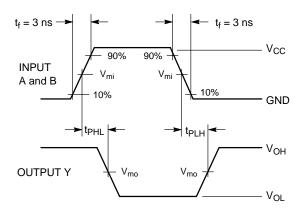
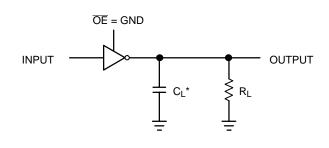


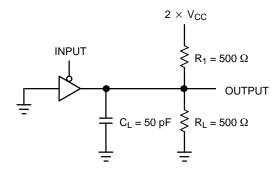
Figure 4. Switching Waveform



*Includes all probe and jig capacitance.

A 1 MHz square input wave is recommended for propagation delay tests.

Figure 5. T_{PLH} or T_{PHL}



A 1 MHz square input wave is recommended for propagation delay tests.

V_{CC} OUTPUT $\frac{1}{2} C_L = 50 \text{ pF}$ $R_L = 250 \Omega$

A 1 MHz square input wave is recommended for propagation delay tests.

Figure 6. T_{PZL} or T_{PL}

Figure 7. T_{PZH} or T_{PHZ}

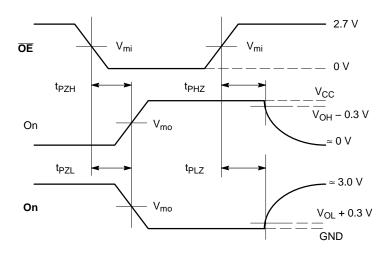


Figure 8. AC Output Enable and Disable Waveform

Table 1. Output Enable and Disable Times

 $t_R = t_F = 2.5 \text{ ns}$, 10% to 90%; f = 1 MHz; $t_W = 500 \text{ ns}$

	V _{CC}					
Symbol	3.3 V \pm 0.3 V	2.7 V	2.5 V \pm 0.2 V			
V _{mi}	1.5 V	1.5 V	V _{CC/} 2			
V_{mo}	1.5 V	1.5 V	V _{CC/} 2			

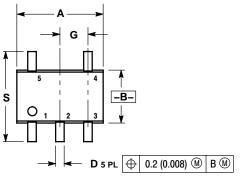
DEVICE ORDERING INFORMATION

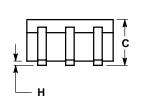
	Device Nomenclature								
Device Order Number	Logic Circuit Indicator	No. of Gates per Package	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape and Reel Suffix	Package Type	Tape and Reel Size
NL17SZ125	NL	1	7	SZ	125	DF	T2	SC70-5/SC-88A/ SOT-353	178 mm (7"), 3000 Units

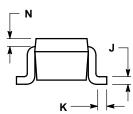
PACKAGE DIMENSIONS

SC70-5/SC-88A/SOT-353 **DF SUFFIX**

5-LEAD PACKAGE CASE 419A-02 ISSUE G



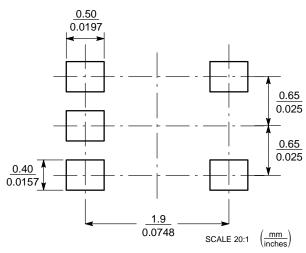




- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
 4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INC	HES	MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.071	0.087	1.80	2.20
В	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026	BSC	0.65	BSC
Н		0.004		0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008	REF	0.20	REF
S	0.079	0.087	2.00	2.20

SOLDERING FOOTPRINT*



*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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