NIF9N05CL

Protected Power MOSFET 2.6 Amps, 52 Volts

N−Channel, Logic Level, Clamped MOSFET w/ ESD Protection in a SOT−223 Package

ON Semiconductor®

http://onsemi.com

V_{DSS} (Clamped)	$R_{DS(ON)}$ TYP	I_D MAX
52 V	107 mΩ	2.6 A

Benefits

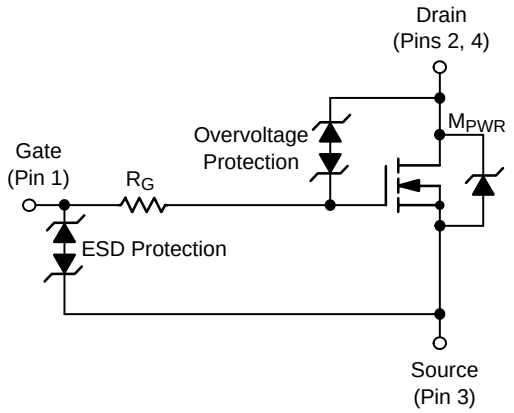
- High Energy Capability for Inductive Loads
- Low Switching Noise Generation

Features

- Diode Clamp Between Gate and Source
- ESD Protection − HBM 5000 V
- Active Over−Voltage Gate to Drain Clamp
- Scalable to Lower or Higher $R_{DS(on)}$
- Internal Series Gate Resistance

Applications

- Automotive and Industrial Markets:
  Solenoid Drivers, Lamp Drivers, Small Motor Drivers



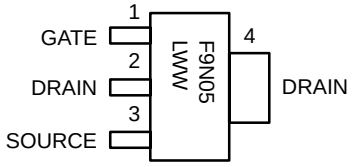
MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage Internally Clamped	V_{DSS}	52−59	V
Gate−to−Source Voltage − Continuous	V_{GS}	±12	V
Drain Current − Continuous @ T_A = 25°C − Single Pulse (tp = 10 μs) (Note 1)	I_D I_{DM}	2.6 10	A
Total Power Dissipation @ T_A = 25°C (Note 1)	P_D	1.69	W
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C
Single Pulse Drain−to−Source Avalanche Energy (V_{DD} = 50 V, $I_{D(pk)}$ = 1.17 A, V_{GS} = 10 V, L = 160 mH, R_G = 25 Ω)	E_{AS}	110	mJ
Thermal Resistance − Junction−to−Ambient (Note 1) − Junction−to−Ambient (Note 2)	 $R_{\theta JA}$ $R_{\theta JA}$	 74 169	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 Sec.	T_L	260	°C

1. When surface mounted to an FR4 board using 1″ pad size, (Cu area 1.127 in^2)
2. When surface mounted to an FR4 board using minimum recommended pad size, (Cu area 0.412 in^2)

SOT−223
CASE 318E
STYLE 3

MARKING DIAGRAM



(Top View)

F9N05 = Specific Device Code
L = Location Code
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NIF9N05CLT1	SOT−223	1000/Tape & Reel
NIF9N05CLT3	SOT−223	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain−to−Source Breakdown Voltage (Note 3) (V_{GS} = 0 V, I_D = 1.0 mA) Temperature Coefficient (Negative)	$V_{(BR)DSS}$	52	55 −9.3	59	V mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 40 V, V_{GS} = 0 V) (V_{DS} = 40 V, V_{GS} = 0 V, T_J = 125°C)	I_{DSS}			10 25	μA
Gate−Body Leakage Current (V_{GS} = ±8 V, V_{DS} = 0 V) (V_{GS} = ±14 V, V_{DS} = 0 V)	I_{GSS}		 ±22	±10	μA
ON CHARACTERISTICS (Note 3)					
Gate Threshold Voltage (Note 3) (V_{DS} = V_{GS}, I_D = 100 μA) Threshold Temperature Coefficient (Negative)	$V_{GS(th)}$	1.3	1.75 −4.1	2.5	V mV/°C
Static Drain−to−Source On−Resistance (Note 3) (V_{GS} = 3.5 V, I_D = 0.6 A) (V_{GS} = 4.0 V, I_D = 1.5 A) (V_{GS} = 10 V, I_D = 2.6 A)	$R_{DS(on)}$		 190 165 107	 380 200 125	mΩ
Forward Transconductance (Note 3) (V_{DS} = 15 V, I_D = 2.6 A)	g_{FS}		3.8		Mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	C_{iss}		155	250	pF
Output Capacitance	C_{oss}		60	100	
Transfer Capacitance	C_{rss}		25	40	
Input Capacitance	C_{iss}		170		pF
Output Capacitance	C_{oss}		70		
Transfer Capacitance	C_{rss}		30		

V_{DS} = 35 V, V_{GS} = 0 V, f = 10 kHz

V_{DS} = 25 V, V_{GS} = 0 V, f = 10 kHz

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (Note 4)						
Turn−On Delay Time	V_{GS} = 4.5 V, V_{DD} = 40 V, I_D = 2.6 A, R_D = 15.4 Ω	$t_{d(on)}$		275	465	ns
Rise Time		t_r		1418	2400	
Turn−Off Delay Time		$t_{d(off)}$		780	1320	
Fall Time		t_f		1120	1900	
Turn−On Delay Time	V_{GS} = 4.5 V, V_{DD} = 40 V, I_D = 1.0 A, R_D = 40 Ω	$t_{d(on)}$		242		ns
Rise Time		t_r		1165		
Turn−Off Delay Time		$t_{d(off)}$		906		
Fall Time		t_f		1273		
Turn−On Delay Time	V_{GS} = 10 V, V_{DD} = 15 V, I_D = 2.6 A, R_D = 5.8 Ω	$t_{d(on)}$		107		ns
Rise Time		t_r		290		
Turn−Off Delay Time		$t_{d(off)}$		1540		
Fall Time		t_f		1000		
Gate Charge	V_{GS} = 4.5 V, V_{DS} = 40 V, I_D = 2.6 A (Note 3)	Q_T		4.5	7.0	nC
		Q_1		0.9		
		Q_2		2.6		
Gate Charge	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 1.5 A (Note 3)	Q_T		3.9		nC
		Q_1		1.0		
		Q_2		1.7		
SOURCE−DRAIN DIODE CHARACTERISTICS						
Forward On−Voltage	I_S = 2.6 A, V_{GS} = 0 V (Note 3) I_S = 2.6 A, V_{GS} = 0 V, T_J = 125°C	V_{SD}		0.81 0.66	1.5	V
Reverse Recovery Time	I_S = 1.5 A, V_{GS} = 0 V, dI_S/dt = 100 A/μs (Note 3)	t_{rr}		730		ns
		t_a		200		
		t_b		530		
Reverse Recovery Stored Charge		Q_{RR}		6.3		μC
ESD CHARACTERISTICS						
Electro−Static Discharge Capability	Human Body Model (HBM)	ESD	5000			V
	Machine Model (MM)		500			

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

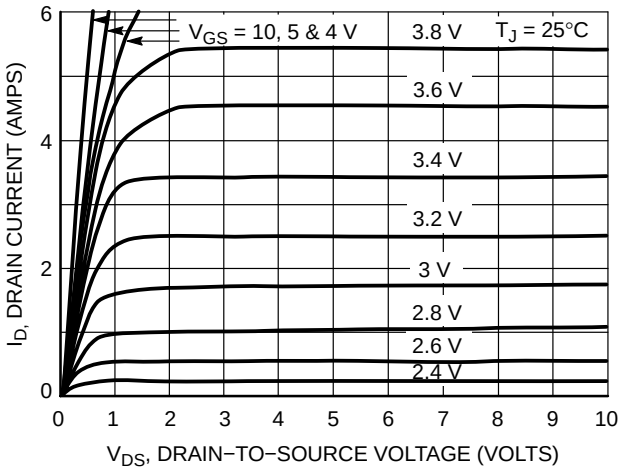


Figure 1. On−Region Characteristics

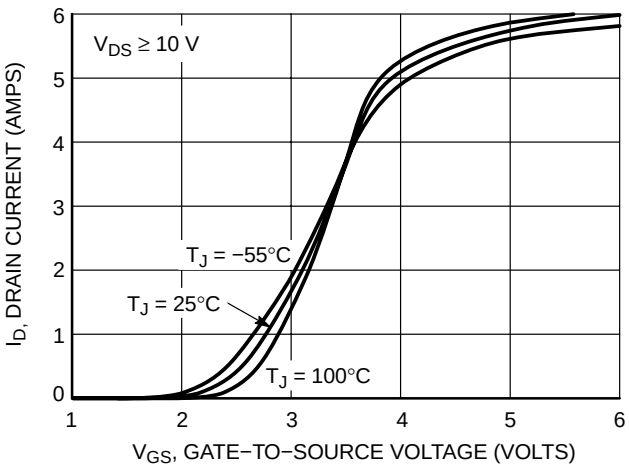


Figure 2. Transfer Characteristics

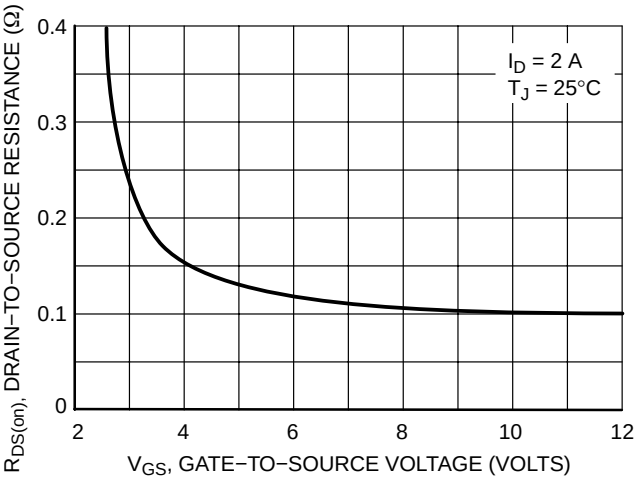


Figure 3. On−Resistance vs. Gate−to−Source Voltage

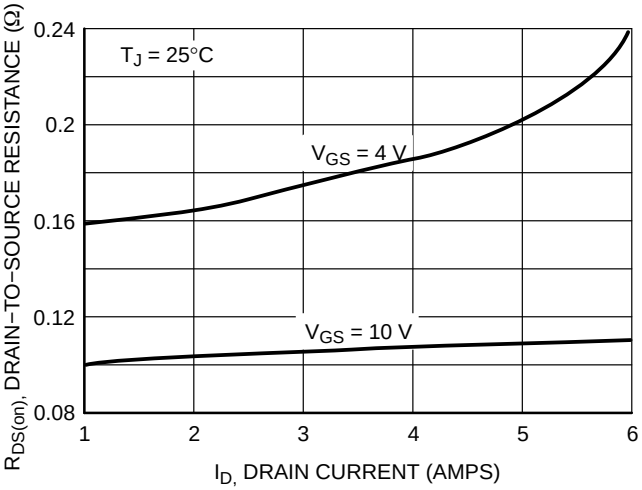


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

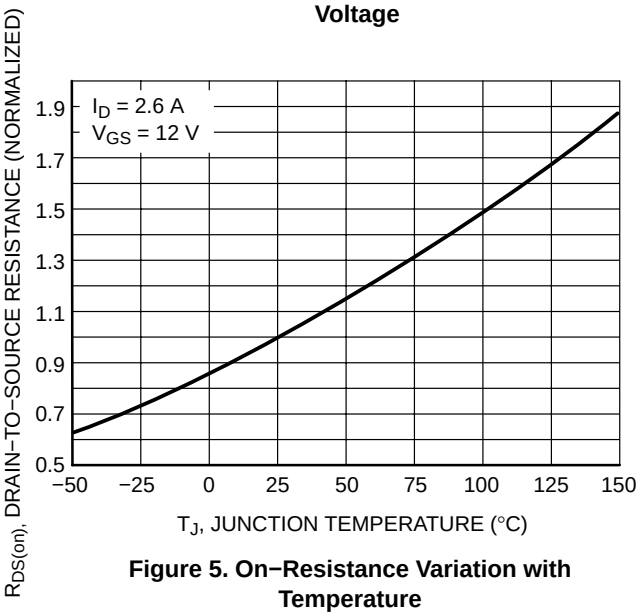


Figure 5. On−Resistance Variation with Temperature

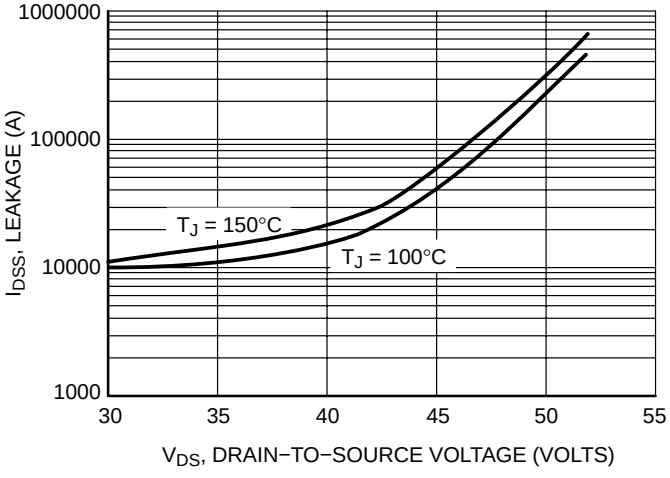


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

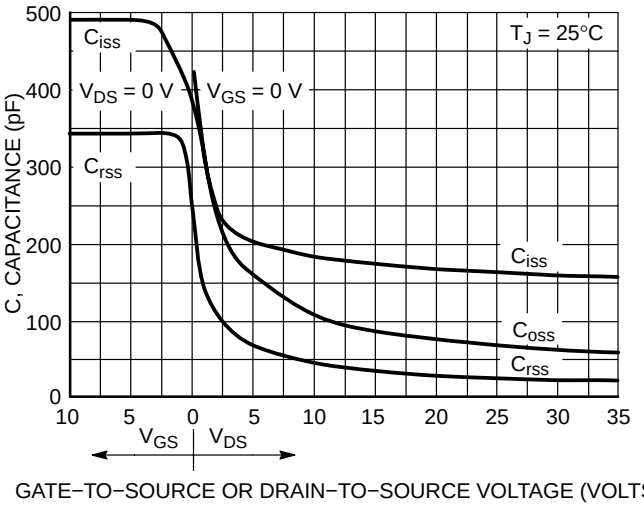


Figure 7. Capacitance Variation

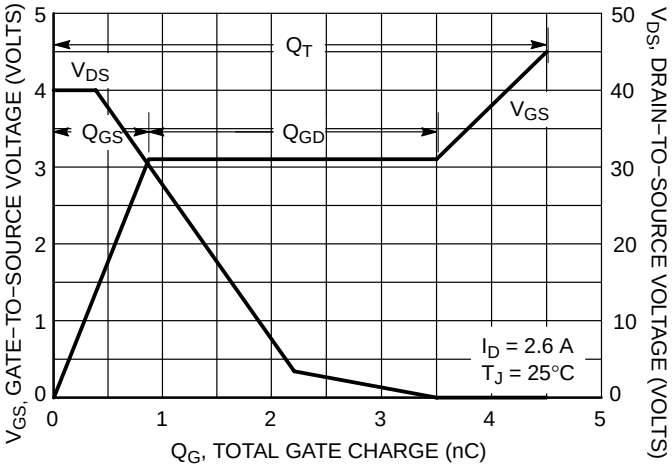


Figure 8. Gate−to−Source Voltage vs. Total Gate Charge

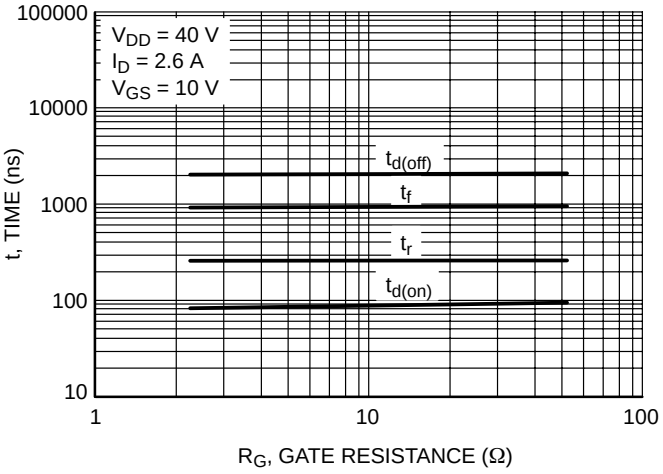


Figure 9. Resistance Switching Time Variation vs. Gate Resistance

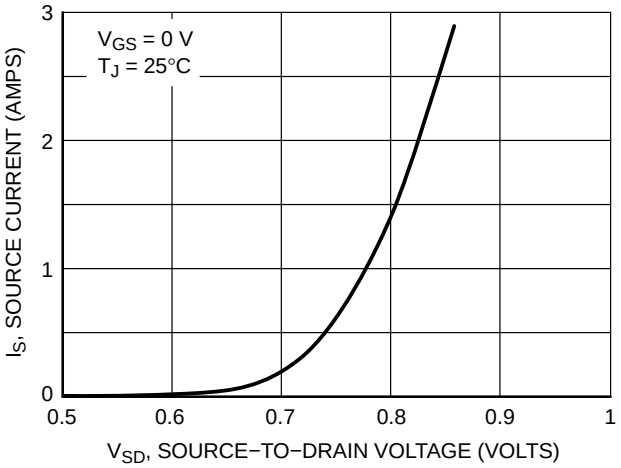
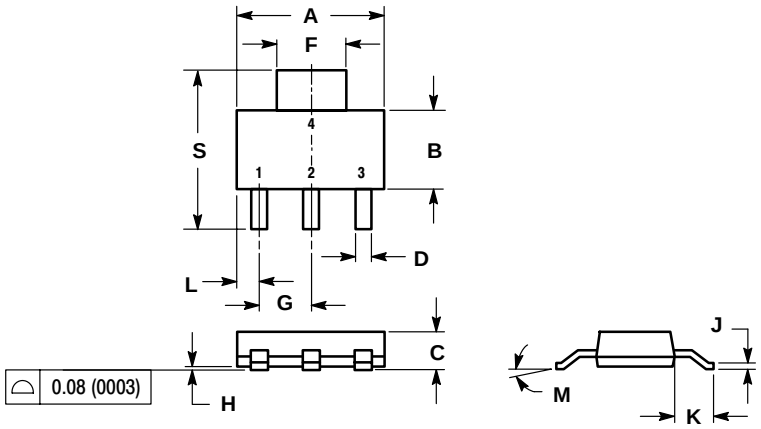


Figure 10. Diode Forward Voltage vs. Current

PACKAGE DIMENSIONS

SOT−223
CASE 318E−04
ISSUE K



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.249	0.263	6.30	6.70
B	0.130	0.145	3.30	3.70
C	0.060	0.068	1.50	1.75
D	0.024	0.035	0.60	0.89
F	0.115	0.126	2.90	3.20
G	0.087	0.094	2.20	2.40
H	0.0008	0.0040	0.020	0.100
J	0.009	0.014	0.24	0.35
K	0.060	0.078	1.50	2.00
L	0.033	0.041	0.85	1.05
M	0 °	10 °	0 °	10 °
S	0.264	0.287	6.70	7.30

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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