

NGB18N40CLBT4

Ignition IGBT 18 Amps, 400 Volts

N-Channel D²PAK

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features monolithic circuitry integrating ESD and Over-Voltage clamped protection for use in inductive coil drivers applications. Primary uses include Ignition, Direct Fuel Injection, or wherever high voltage and high current switching is required.

- Ideal for Coil-on-Plug Applications
- Gate-Emitter ESD Protection
- Temperature Compensated Gate-Collector Voltage Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- New Design Increases Unclamped Inductive Switching (UIS) Energy Per Area
- Low Threshold Voltage to Interface Power Loads to Logic or Microprocessor Devices
- Low Saturation Voltage
- High Pulsed Current Capability
- Optional Gate Resistor (R_G) and Gate-Emitter Resistor (R_{GE})
- Emitter Ballasting for Short-Circuit Capability

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CES}	430	V_{DC}
Collector-Gate Voltage	V_{CER}	430	V_{DC}
Gate-Emitter Voltage	V_{GE}	18	V_{DC}
Collector Current-Continuous @ $T_C = 25^\circ\text{C}$ - Pulsed	I_C	18 50	A_{DC} A_{AC}
ESD (Human Body Model) $R = 1500\ \Omega$, $C = 100\ \text{pF}$	ESD	8.0	kV
ESD (Machine Model) $R = 0\ \Omega$, $C = 200\ \text{pF}$	ESD	800	V
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	115 0.77	Watts $\text{W}/^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to +175	$^\circ\text{C}$



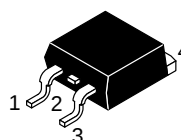
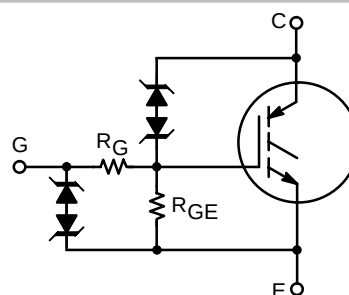
ON Semiconductor®

<http://onsemi.com>

18 AMPS

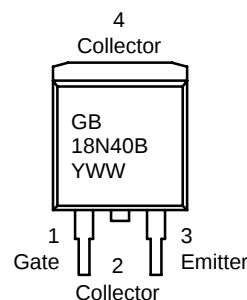
400 VOLTS

$$V_{CE(on)} \leq 2.0\ \text{V @}$$
$$I_C = 10\ \text{A}, V_{GE} \geq 4.5\ \text{V}$$



D²PAK
CASE 418B
STYLE 4

MARKING DIAGRAM



GB18N40B = NGB18N40CLB
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
NGB18N40CLBT4	D ² PAK	800/Tape & Reel

NGB18N40CLBT4

UNCLAMPED COLLECTOR-TO-EMITTER AVALANCHE CHARACTERISTICS (-55° ≤ T_J ≤ 175°C)

Characteristic	Symbol	Value	Unit
Single Pulse Collector-to-Emitter Avalanche Energy V _{CC} = 50 V, V _{GE} = 5.0 V, Pk I _L = 21.1 A, L = 1.8 mH, Starting T _J = 25°C V _{CC} = 50 V, V _{GE} = 5.0 V, Pk I _L = 18.3 A, L = 1.8 mH, Starting T _J = 125°C	E _{AS}	400 300	mJ
Reverse Avalanche Energy V _{CC} = 100 V, V _{GE} = 20 V, Pk I _L = 25.8 A, L = 6.0 mH, Starting T _J = 25°C	E _{AS(R)}	2000	mJ

MAXIMUM SHORT-CIRCUIT TIMES (-55°C ≤ T_J ≤ 150°C)

Short Circuit Withstand Time 1 (See Figure 17, 3 Pulses with 10 ms Period)	t _{sc1}	750	μs
Short Circuit Withstand Time 2 (See Figure 18, 3 Pulses with 10 ms Period)	t _{sc2}	5.0	ms

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case	R _{θJC}	1.3	°C/W
Thermal Resistance, Junction to Ambient D ² PAK (Note 1)	R _{θJA}	50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T _L	275	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
----------------	--------	-----------------	-------------	-----	-----	-----	------

OFF CHARACTERISTICS

Collector-Emitter Clamp Voltage	BV _{CES}	I _C = 2.0 mA	T _J = -40°C to 150°C	380	395	420	V _{DC}
		I _C = 10 mA	T _J = -40°C to 150°C	390	405	430	
Zero Gate Voltage Collector Current	I _{CES}	V _{CE} = 350 V, V _{GE} = 0 V	T _J = 25°C	-	2.0	20	μA _{DC}
			T _J = 150°C	-	10	40*	
			T _J = -40°C	-	1.0	10	
Reverse Collector-Emitter Leakage Current	I _{ECS}	V _{CE} = -24 V	T _J = 25°C	-	0.7	2.0	mA
			T _J = 150°C	-	12	25*	
			T _J = -40°C	-	0.1	1.0	
Reverse Collector-Emitter Clamp Voltage	BV _{CES(R)}	I _C = -75 mA	T _J = 25°C	27	33	37	V _{DC}
			T _J = 150°C	30	36	40	
			T _J = -40°C	25	32	35	
Gate-Emitter Clamp Voltage	BV _{GES}	I _G = 5.0 mA	T _J = -40°C to 150°C	11	13	15	V _{DC}
Gate-Emitter Leakage Current	I _{GES}	V _{GE} = 10 V	T _J = -40°C to 150°C	384	640	1000	μA _{DC}
Gate Resistor (Optional)	R _G	-	T _J = -40°C to 150°C	-	70	-	Ω
Gate Emitter Resistor	R _{GE}	-	T _J = -40°C to 150°C	10	16	26	kΩ

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	V _{GE(th)}	I _C = 1.0 mA, V _{GE} = V _{CE}	T _J = 25°C	1.1	1.4	1.9	V _{DC}
			T _J = 150°C	0.75	1.0	1.4	
			T _J = -40°C	1.2	1.6	2.1*	
Threshold Temperature Coefficient (Negative)	-	-	-	-	3.4	-	mV/°C

1. When surface mounted to an FR4 board using the minimum recommended pad size.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

*Maximum Value of Characteristic across Temperature Range.

NGB18N40CLBT4

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
----------------	--------	-----------------	-------------	-----	-----	-----	------

ON CHARACTERISTICS (continued) (Note 3)

Collector-to-Emitter On-Voltage	$V_{CE(on)}$	$I_C = 6.0 \text{ A}, V_{GE} = 4.0 \text{ V}$	$T_J = 25^\circ\text{C}$	1.0	1.4	1.6	V_{DC}
			$T_J = 150^\circ\text{C}$	0.9	1.3	1.6	
			$T_J = -40^\circ\text{C}$	1.1	1.45	1.7*	
		$I_C = 8.0 \text{ A}, V_{GE} = 4.0 \text{ V}$	$T_J = 25^\circ\text{C}$	1.3	1.6	1.9*	
			$T_J = 150^\circ\text{C}$	1.2	1.55	1.8	
			$T_J = -40^\circ\text{C}$	1.4	1.6	1.9*	
		$I_C = 10 \text{ A}, V_{GE} = 4.0 \text{ V}$	$T_J = 25^\circ\text{C}$	1.4	1.8	2.05	
			$T_J = 150^\circ\text{C}$	1.5	1.8	2.0	
			$T_J = -40^\circ\text{C}$	1.4	1.8	2.1*	
		$I_C = 15 \text{ A}, V_{GE} = 4.0 \text{ V}$	$T_J = 25^\circ\text{C}$	1.8	2.2	2.5	
			$T_J = 150^\circ\text{C}$	2.0	2.4	2.6*	
			$T_J = -40^\circ\text{C}$	1.7	2.1	2.5	
		$I_C = 10 \text{ A}, V_{GE} = 4.5 \text{ V}$	$T_J = 25^\circ\text{C}$	1.3	1.8	2.0*	
			$T_J = 150^\circ\text{C}$	1.3	1.75	2.0*	
			$T_J = -40^\circ\text{C}$	1.4	1.8	2.0*	
Forward Transconductance	g_{fs}	$V_{CE} = 5.0 \text{ V}, I_C = 6.0 \text{ A}$	$T_J = -40^\circ\text{C to } 150^\circ\text{C}$	8.0	14	25	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	C_{ISS}	$V_{CC} = 25 \text{ V}, V_{GE} = 0 \text{ V}$ $f = 1.0 \text{ MHz}$	$T_J = -40^\circ\text{C to } 150^\circ\text{C}$	400	800	1000	pF
Output Capacitance	C_{OSS}			50	75	100	
Transfer Capacitance	C_{RSS}			4.0	7.0	10	

SWITCHING CHARACTERISTICS

Turn-Off Delay Time (Resistive)	$t_{d(off)}$	$V_{CC} = 300 \text{ V}, I_C = 6.5 \text{ A}$ $R_G = 1.0 \text{ k}\Omega, R_L = 46 \Omega$	$T_J = 25^\circ\text{C}$	-	4.0	10	μSec
Fall Time (Resistive)	t_f	$V_{CC} = 300 \text{ V}, I_C = 6.5 \text{ A}$ $R_G = 1.0 \text{ k}\Omega, R_L = 46 \Omega$	$T_J = 25^\circ\text{C}$	-	9.0	15	
Turn-On Delay Time	$t_{d(on)}$	$V_{CC} = 10 \text{ V}, I_C = 6.5 \text{ A}$ $R_G = 1.0 \text{ k}\Omega, R_L = 1.5 \Omega$	$T_J = 25^\circ\text{C}$	-	0.7	4.0	μSec
Rise Time	t_r	$V_{CC} = 10 \text{ V}, I_C = 6.5 \text{ A}$ $R_G = 1.0 \text{ k}\Omega, R_L = 1.5 \Omega$	$T_J = 25^\circ\text{C}$	-	4.5	7.0	

3. Pulse Test: Pulse Width $\leq 300 \mu\text{S}$, Duty Cycle $\leq 2\%$.

*Maximum Value of Characteristic across Temperature Range.

NGB18N40CLBT4

TYPICAL ELECTRICAL CHARACTERISTICS (unless otherwise noted)

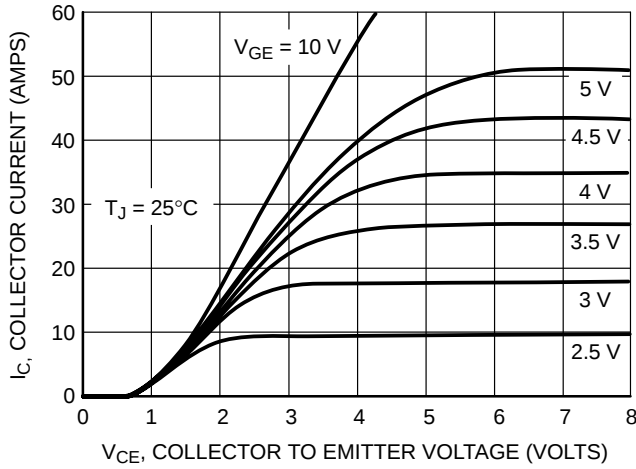


Figure 1. Output Characteristics

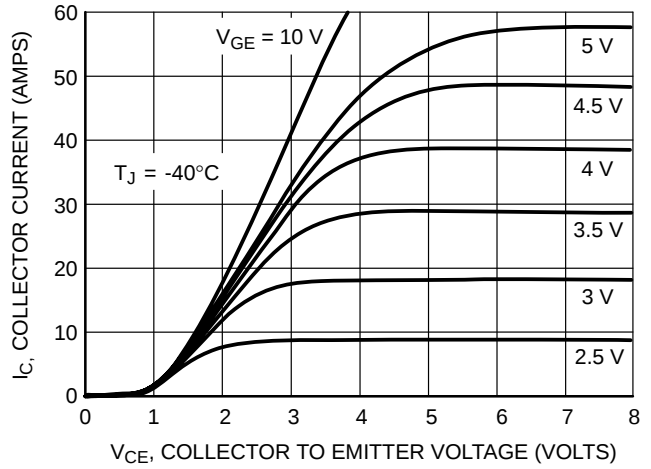


Figure 2. Output Characteristics

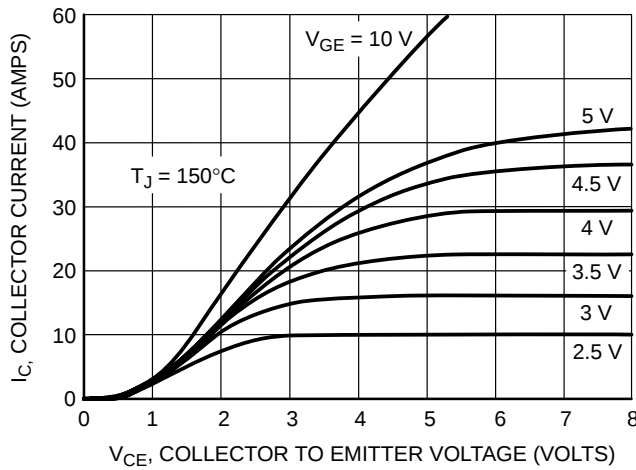


Figure 3. Output Characteristics

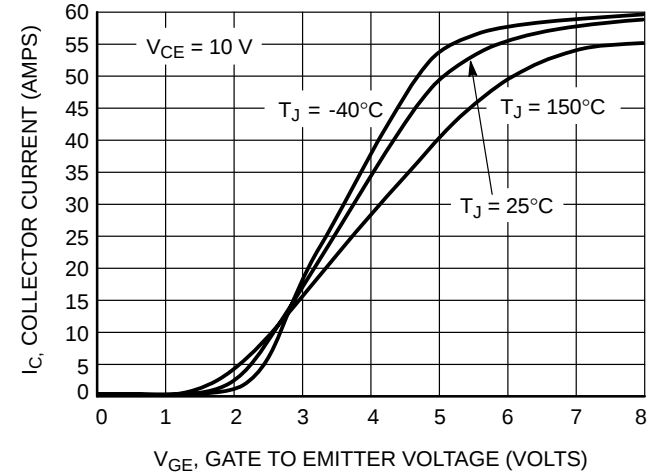


Figure 4. Transfer Characteristics

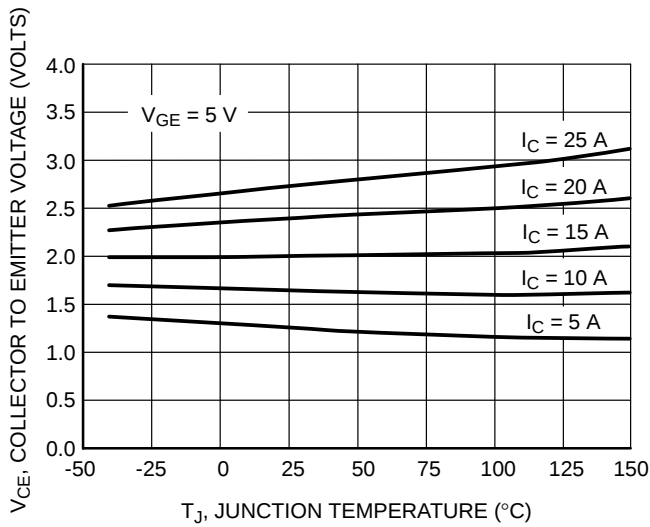


Figure 5. Collector-to-Emitter Saturation Voltage versus Junction Temperature

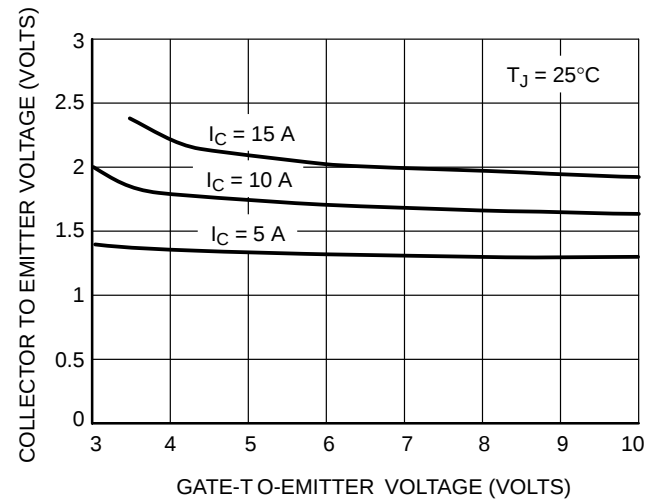


Figure 6. Collector-to-Emitter Voltage versus Gate-to-Emitter Voltage

NGB18N40CLBT4

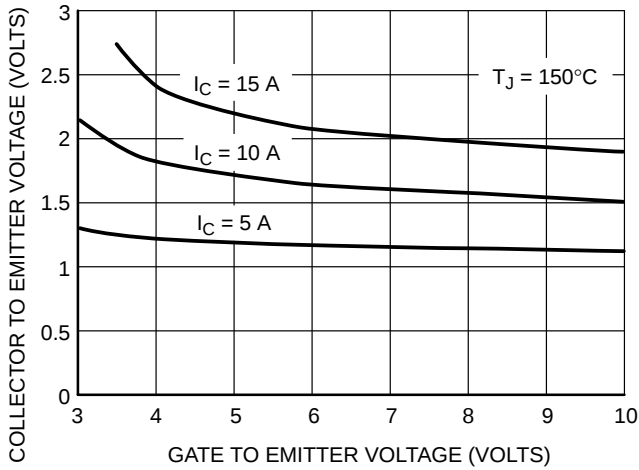


Figure 7. Collector-to-Emitter Voltage versus Gate-to-Emitter Voltage

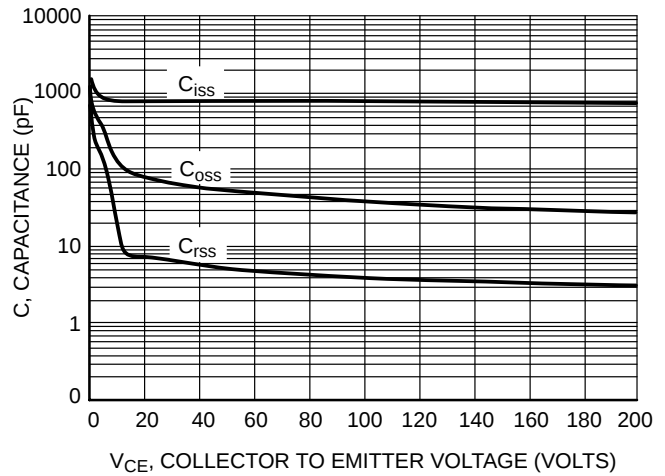


Figure 8. Capacitance Variation

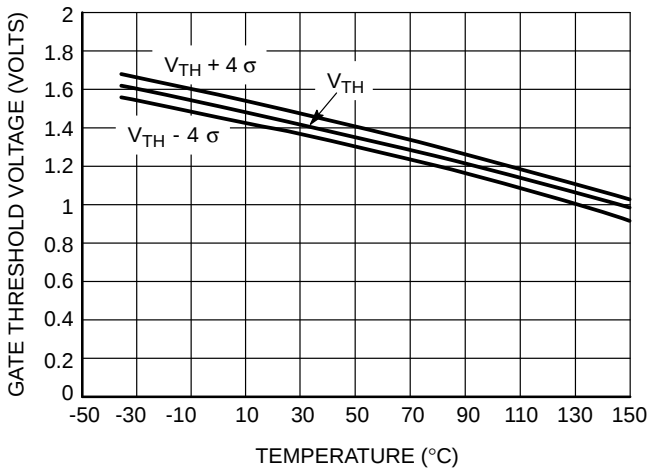


Figure 9. Gate Threshold Voltage versus Temperature

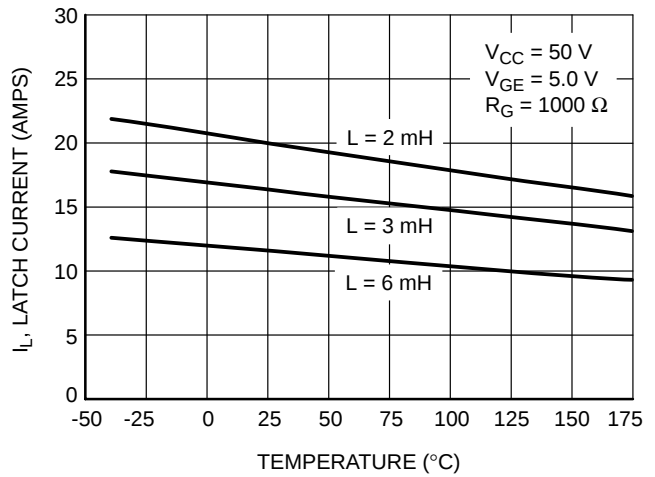


Figure 10. Minimum Open Secondary Latch Current versus Temperature

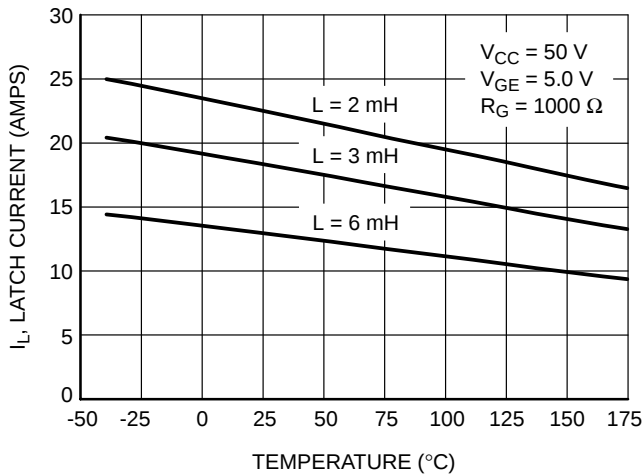


Figure 11. Typical Open Secondary Latch Current versus Temperature

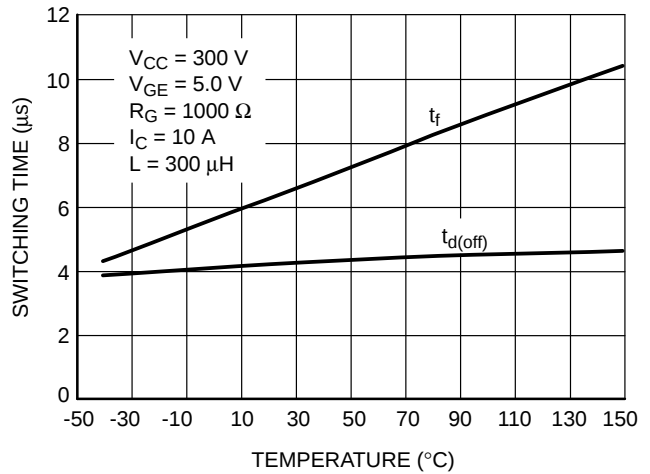


Figure 12. Inductive Switching Fall Time versus Temperature

NGB18N40CLBT4

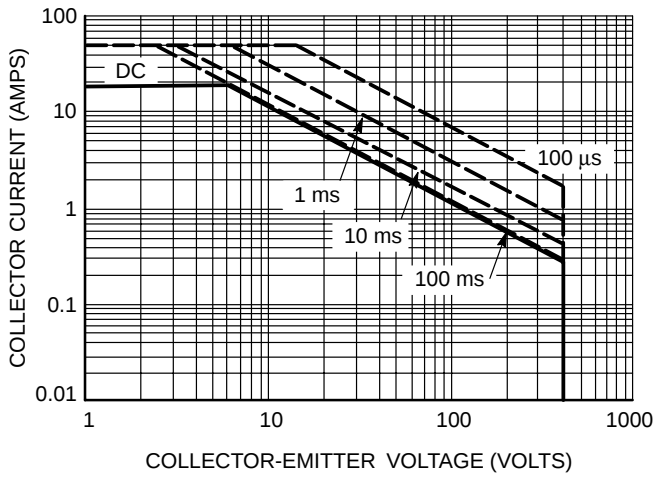


Figure 13. Single Pulse Safe Operating Area
(Mounted on an Infinite Heatsink at $T_A = 25^\circ\text{C}$)

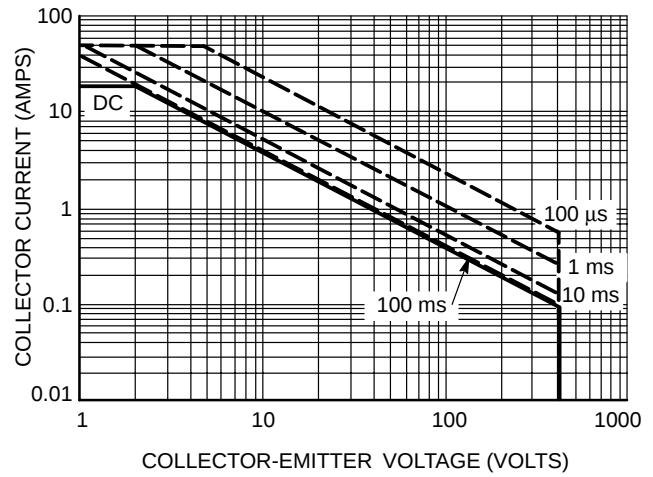


Figure 14. Single Pulse Safe Operating Area
(Mounted on an Infinite Heatsink at $T_A = 125^\circ\text{C}$)

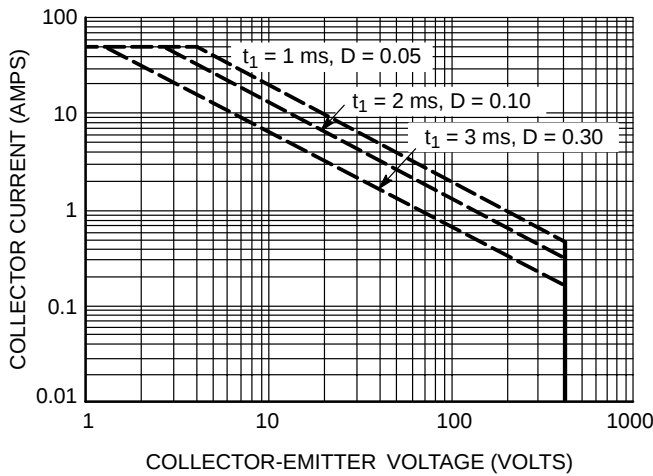


Figure 15. Pulse Train Safe Operating Area
(Mounted on an Infinite Heatsink at $T_C = 25^\circ\text{C}$)

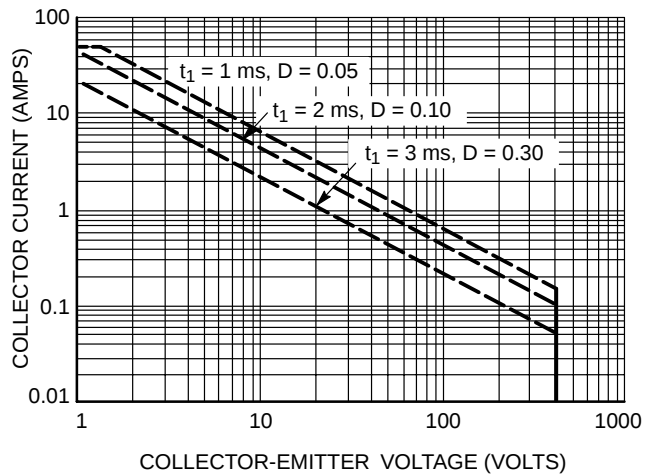


Figure 16. Pulse Train Safe Operating Area
(Mounted on an Infinite Heatsink at $T_C = 125^\circ\text{C}$)

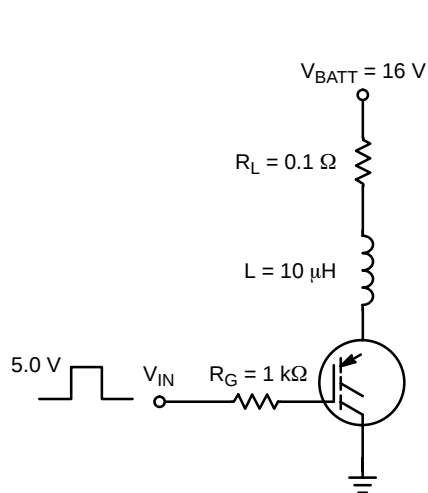


Figure 17. Circuit Configuration for
Short Circuit Test #1

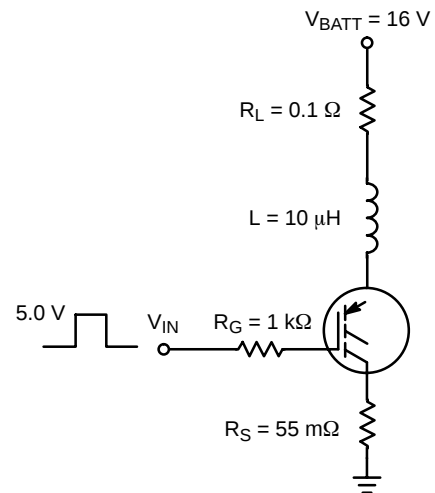


Figure 18. Circuit Configuration for
Short Circuit Test #2

NGB18N40CLBT4

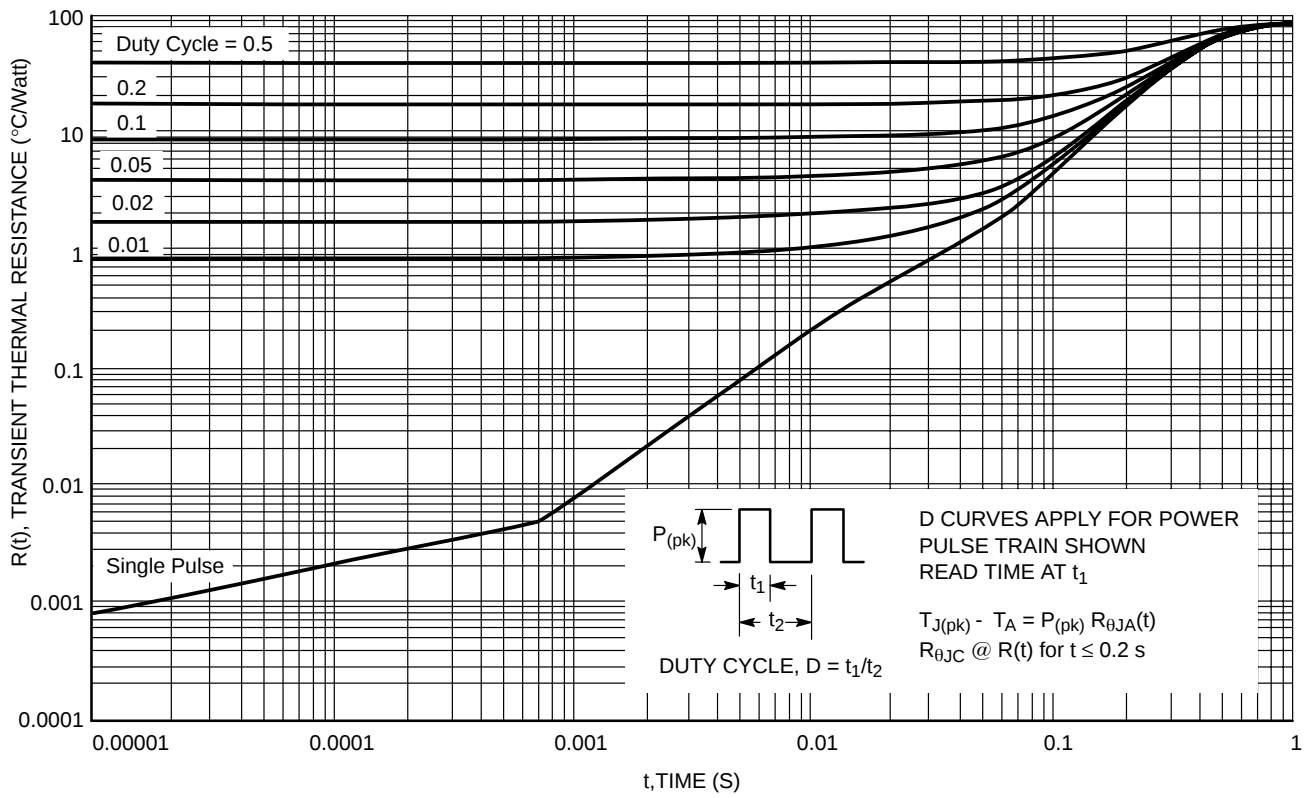
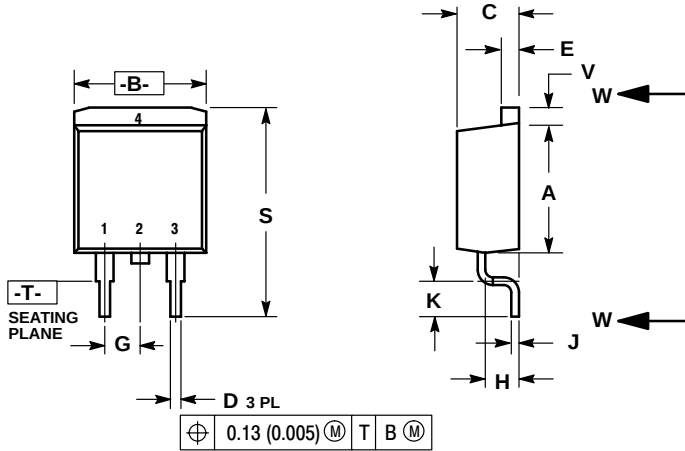


Figure 19. Transient Thermal Resistance
(Non-normalized Junction-to-Ambient mounted on minimum pad area)

NGB18N40CLBT4

PACKAGE DIMENSIONS

D²PAK
CASE 418B-04
ISSUE H



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197 REF		5.00 REF	
P	0.079 REF		2.00 REF	
R	0.039 REF		0.99 REF	
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 4:

- PIN 1: GATE
2: COLLECTOR
3: EMITTER
4: COLLECTOR

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.