

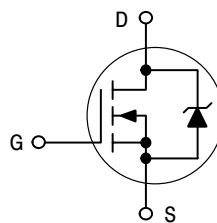
TMOS E-FET™

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate

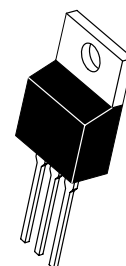
This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage-blocking capability without degrading performance over time. In addition, this advanced TMOS E-FET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain-to-source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters, PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature



MTP8N50E

TMOS POWER FET
8.0 AMPERES
500 VOLTS
 $R_{DS(on)} = 0.8 \text{ OHM}$



CASE 221A-09, Style 5
TO-220AB

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	500	Vdc
Drain-to-Gate Voltage ($R_{GS} = 1.0 \text{ M}\Omega$)	V_{DGR}	500	Vdc
Gate-to-Source Voltage – Continuous	V_{GS}	± 20	Vdc
– Non-repetitive ($t_p \leq 10 \text{ ms}$)	V_{GSM}	± 40	Vpk
Drain Current — Continuous @ $T_C = 25^\circ\text{C}$	I_D	8.0	Adc
— Continuous @ $T_C = 100^\circ\text{C}$	I_D	5.0	
— Single Pulse ($t_p \leq 10 \mu\text{s}$)	I_{DM}	32	Apk
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	125	Watts
Derate above 25°C		1.0	W/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – STARTING $T_J = 25^\circ\text{C}$ ($V_{DD} = 25 \text{ Vdc}$, $V_{GS} = 10 \text{ Vdc}$, PEAK $I_L = 8.0 \text{ Apk}$, $L = 16 \text{ mH}$, $R_G = 25 \Omega$)	E_{AS}	510	mJ
Thermal Resistance			
– Junction-to-Case	$R_{\theta JC}$	1.0	$^\circ\text{C/W}$
– Junction-to-Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 5 sec.	T_L	260	$^\circ\text{C}$

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ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage ($V_{GS} = 0\text{ Vdc}$, $I_D = 250\text{ }\mu\text{Adc}$) Temperature Coefficient (Positive)	$V_{(BR)DSS}$	500 —	— 500	— —	Vdc mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current ($V_{DS} = 500\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$) ($V_{DS} = 400\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$, $T_J = 125^\circ\text{C}$)	I_{DSS}	— —	— —	250 1000	μAdc
Gate-Body Leakage Current ($V_{GS} = \pm 20\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	100	nAdc

ON CHARACTERISTICS (1)

Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{Adc}$) Threshold Temperature Coefficient (Negative)	$V_{GS(th)}$	2.0 —	2.8 6.3	4.0 —	Vdc mV/ $^\circ\text{C}$
Static Drain-to-Source On-Resistance ($V_{GS} = 10\text{ Vdc}$, $I_D = 4.0\text{ Adc}$)	$R_{DS(on)}$	—	0.6	0.8	Ohms
Drain-to-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$) ($I_D = 8.0\text{ Adc}$) ($I_D = 4.0\text{ Adc}$, $T_J = 125^\circ\text{C}$)	$V_{DS(on)}$	— —	5.0 —	7.2 6.4	Vdc
Forward Transconductance ($V_{DS} = 15\text{ Vdc}$, $I_D = 4.0\text{ Adc}$)	g_{FS}	4.0	—	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = 25\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$, $f = 1.0\text{ MHz}$)	C_{iss}	—	1450	1680	pF
Output Capacitance		C_{oss}	—	190	246	
Transfer Capacitance		C_{rss}	—	45.4	144	

SWITCHING CHARACTERISTICS (2)

Turn-On Delay Time	$(R_{go} + C17n = 9.1\text{ }\Omega)$	$t_{d(on)}$	—	15	50	ns
Rise Time		t_r	—	33	72	
Turn-Off Delay Time		$t_{d(off)}$	—	40	150	
Fall Time		t_f	—	32	60	
Gate Charge (see Figure 8)	$(V_{DS} = 400\text{ Vdc}$, $I_D = 8.0\text{ Adc}$, $V_{GS} = 10\text{ Vdc}$)	Q_T	—	40	64	nC
		Q_1	—	8.0	—	
		Q_2	—	17	—	
		Q_3	—	17.3	—	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage ($I_S = 8.0\text{ Adc}$, $V_{GS} = 0\text{ Vdc}$) ($I_S = 8.0\text{ Adc}$, $V_{GS} = 0\text{ Vdc}$, $T_J = 125^\circ\text{C}$)	V_{SD}	—	1.2	2.0	Vdc
		—	1.1	—	
Reverse Recovery Time	$(I_S = 8.0\text{ Adc}$, $V_{GS} = 0\text{ Vdc}$, $dI_S/dt = 100\text{ A}/\mu\text{s}$)	t_{rr}	—	320	ns
		t_a	—	179	
		t_b	—	141	
Reverse Recovery Stored Charge	Q_{RR}	—	3.0	—	μC

INTERNAL PACKAGE INDUCTANCE

Internal Drain Inductance (Measured from the drain lead 0.25" from package to center of die)	L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	L_S	—	7.5	—	

(1) Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

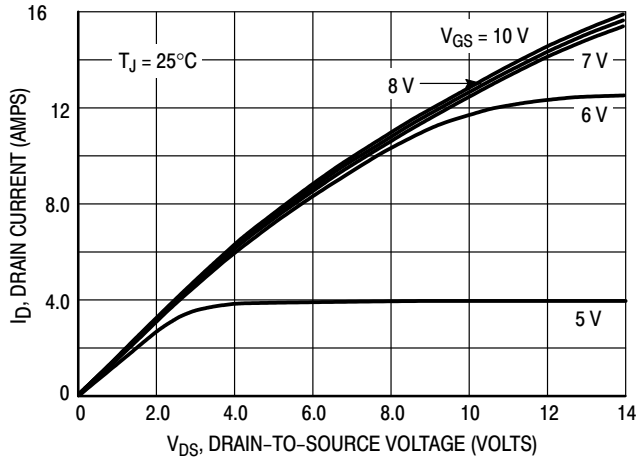


Figure 1. On-Region Characteristics

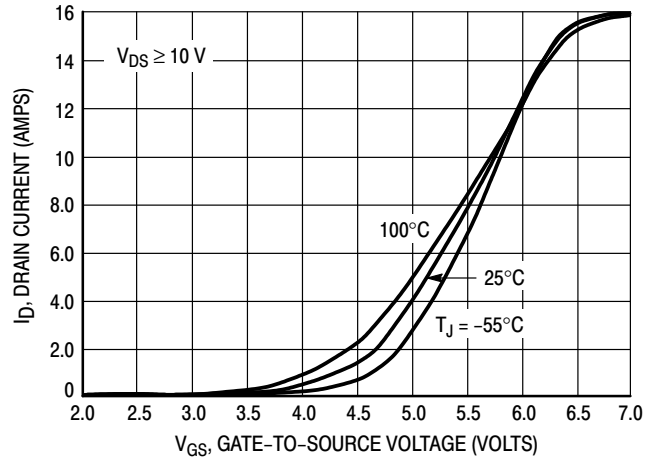


Figure 2. Transfer Characteristics

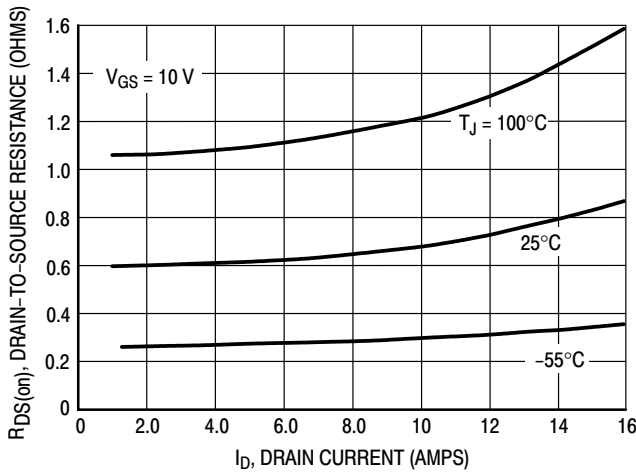


Figure 3. On-Resistance versus Drain Current and Temperature

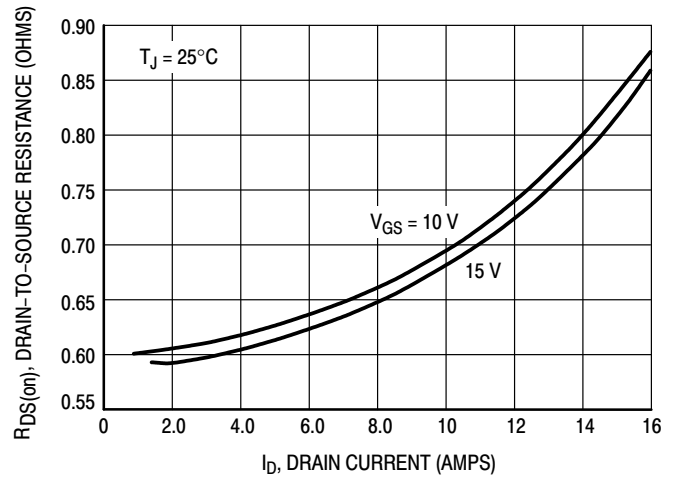


Figure 4. On-Resistance versus Drain Current and Gate Voltage

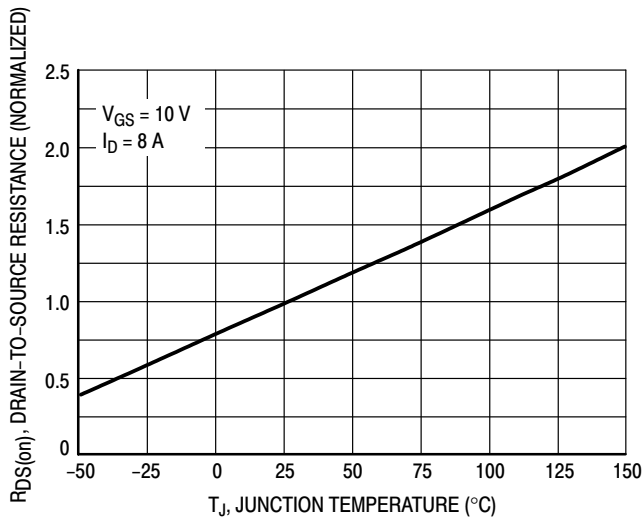


Figure 5. On-Resistance Variation with Temperature

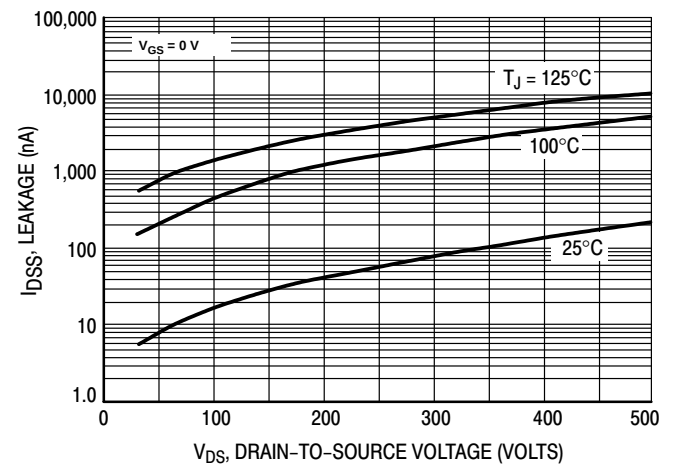


Figure 6. Drain-to-Source Leakage Current versus Voltage

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TYPICAL ELECTRICAL CHARACTERISTICS

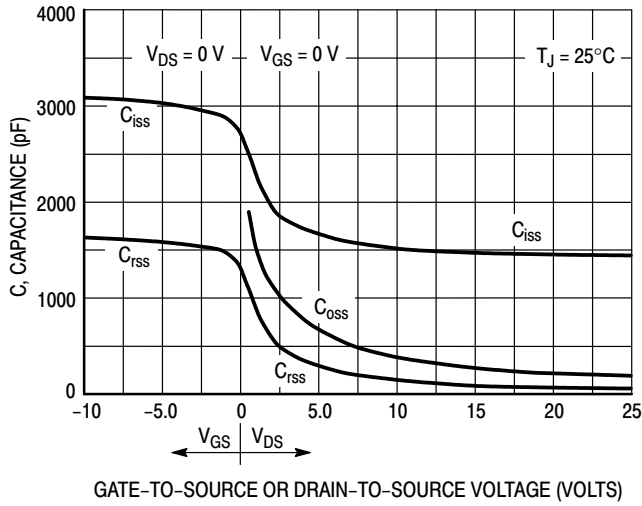


Figure 7. Capacitance Variation

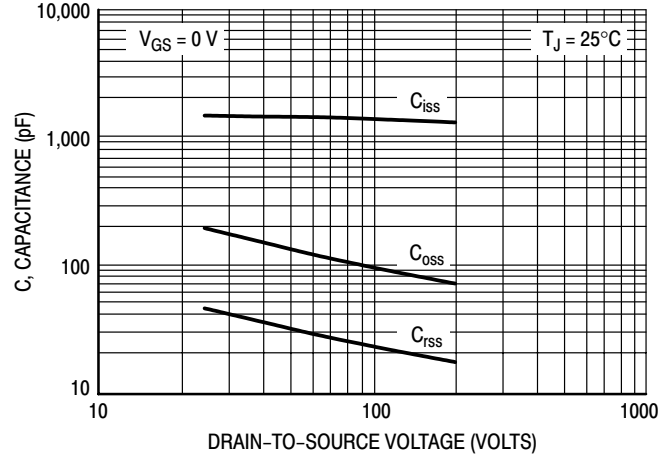


Figure 8. High Voltage Capacitance Variation

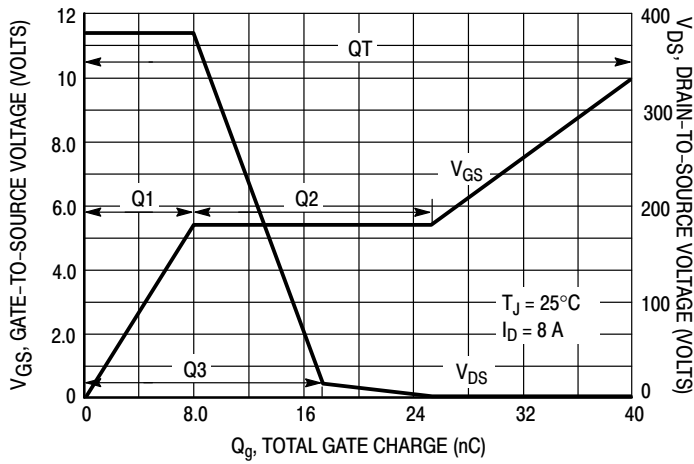


Figure 9. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

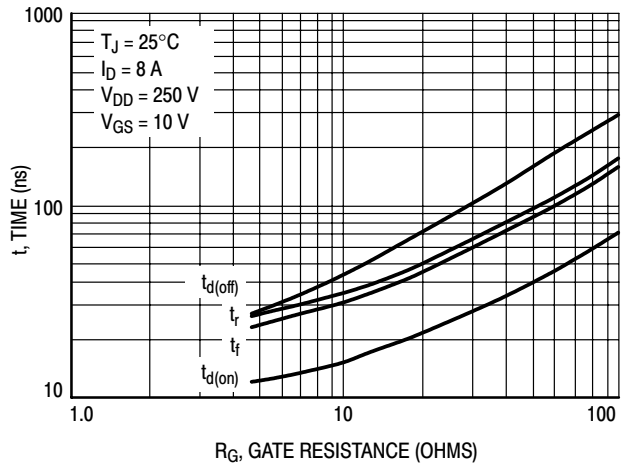


Figure 10. Resistive Switching Time Variation versus Gate Resistance

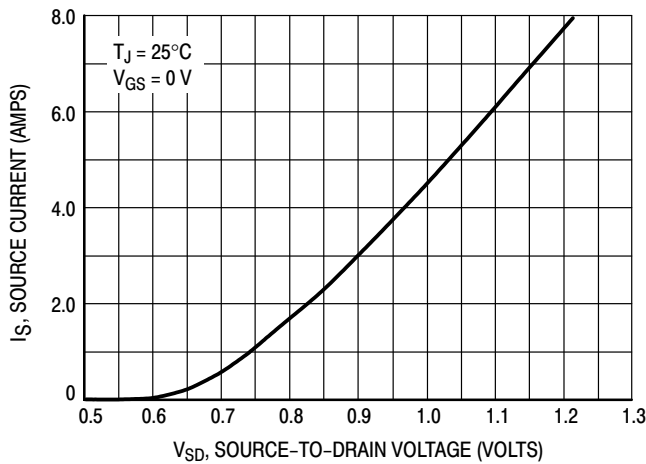


Figure 11. Diode Forward Voltage versus Current

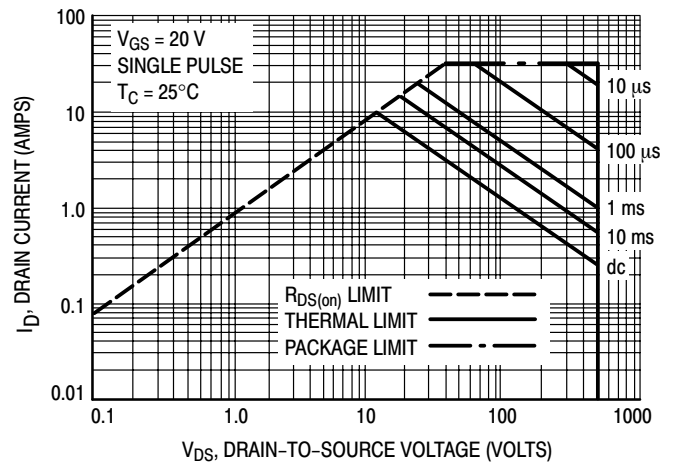


Figure 12. Maximum Rated Forward Biased Safe Operating Area

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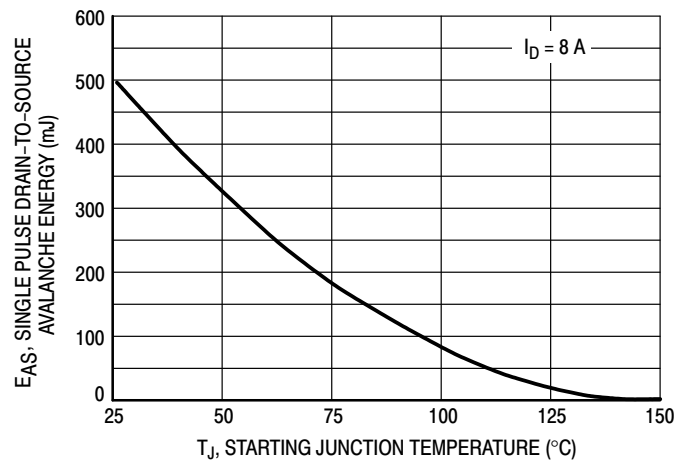


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

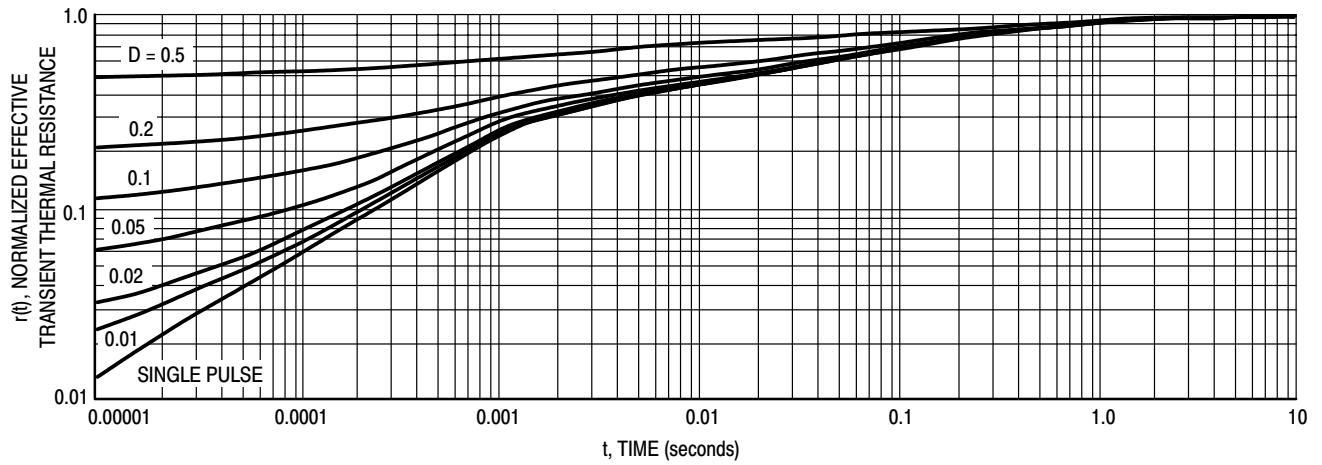
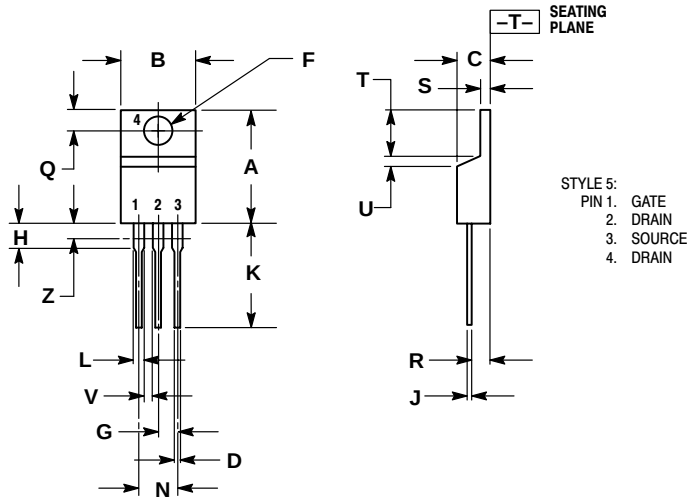


Figure 14. Thermal Response

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PACKAGE DIMENSIONS CASE 221A-09 ISSUE AA



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

Notes

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