

# MTD6N15

## Power Field Effect Transistor DPAK for Surface Mount

### N-Channel Enhancement-Mode Silicon Gate

This TMOS Power FET is designed for high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low  $R_{DS(on)}$  — 0.3  $\Omega$  Max
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement —  $V_{GS(th)} = 4.0$  V Max
- Surface Mount Package on 16 mm Tape

#### MAXIMUM RATINGS

| Rating                                                                                             | Symbol                | Value                | Unit                         |
|----------------------------------------------------------------------------------------------------|-----------------------|----------------------|------------------------------|
| Drain-Source Voltage                                                                               | $V_{DS}$              | 150                  | Vdc                          |
| Drain-Gate Voltage ( $R_{GS} = 1.0$ M $\Omega$ )                                                   | $V_{DGR}$             | 150                  | Vdc                          |
| Gate-Source Voltage — Continuous<br>— Non-Repetitive<br>( $t_p \leq 50$ $\mu$ s)                   | $V_{GS}$<br>$V_{GSM}$ | $\pm 20$<br>$\pm 40$ | Vdc<br>Vpk                   |
| Drain Current — Continuous<br>— Pulsed                                                             | $I_D$<br>$I_{DM}$     | 6.0<br>20            | Adc                          |
| Total Power Dissipation @ $T_C = 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$              | $P_D$                 | 20<br>0.16           | Watts<br>W/ $^\circ\text{C}$ |
| Total Power Dissipation @ $T_A = 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$ (Note 1)     | $P_D$                 | 1.25<br>0.01         | Watts<br>W/ $^\circ\text{C}$ |
| Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (1)<br>Derate above $25^\circ\text{C}$ (Note 2) | $P_D$                 | 1.75<br>0.014        | Watts<br>W/ $^\circ\text{C}$ |
| Operating and Storage Junction Temperature Range                                                   | $T_J, T_{stg}$        | -65 to +150          | $^\circ\text{C}$             |

#### THERMAL CHARACTERISTICS

| Characteristic                                                                                               | Symbol                                                | Value               | Unit               |
|--------------------------------------------------------------------------------------------------------------|-------------------------------------------------------|---------------------|--------------------|
| Thermal Resistance<br>— Junction to Case<br>— Junction to Ambient (Note 1)<br>— Junction to Ambient (Note 2) | $R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | 6.25<br>100<br>71.4 | $^\circ\text{C/W}$ |

1. When surface mounted to an FR4 board using the minimum recommended pad size.
2. When surface mounted to an FR4 board using 0.5 sq. in. drain pad size.

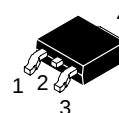
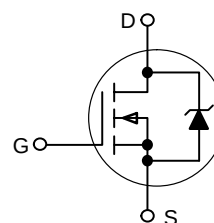


ON Semiconductor®

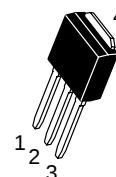
<http://onsemi.com>

| $V_{(BR)DSS}$ | $R_{DS(on)}$ MAX | $I_D$ MAX |
|---------------|------------------|-----------|
| 150 V         | 0.3 $\Omega$     | 6.0 A     |

#### N-CHANNEL

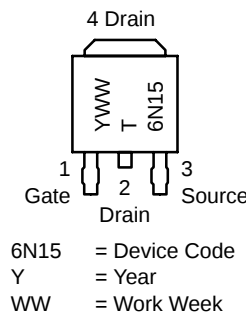


CASE 369C  
DPAK  
(Surface Mount)  
STYLE 2



CASE 369D  
DPAK  
(Straight Lead)  
STYLE 2

#### MARKING DIAGRAM & PIN ASSIGNMENTS



#### ORDERING INFORMATION

| Device    | Package               | Shipping†        |
|-----------|-----------------------|------------------|
| MTD6N15   | DPAK                  | 75 Units/Rail    |
| MTD6N15-1 | DPAK<br>Straight Lead | 75 Units/Rail    |
| MTD6N15T4 | DPAK                  | 2500 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# MTD6N15

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic                                                                                                                 | Symbol        | Min    | Max       | Unit            |
|--------------------------------------------------------------------------------------------------------------------------------|---------------|--------|-----------|-----------------|
| <b>OFF CHARACTERISTICS</b>                                                                                                     |               |        |           |                 |
| Drain-Source Breakdown Voltage<br>( $V_{GS} = 0\text{ Vdc}$ , $I_D = 0.25\text{ mAdc}$ )                                       | $V_{(BR)DSS}$ | 150    | —         | Vdc             |
| Zero Gate Voltage Drain Current<br>( $V_{DS} = \text{Rated } V_{DSS}$ , $V_{GS} = 0\text{ Vdc}$ )<br>$T_J = 125^\circ\text{C}$ | $I_{DSS}$     | —<br>— | 10<br>100 | $\mu\text{Adc}$ |
| Gate-Body Leakage Current, Forward ( $V_{GSF} = 20\text{ Vdc}$ , $V_{DS} = 0$ )                                                | $I_{GSSF}$    | —      | 100       | nAdc            |
| Gate-Body Leakage Current, Reverse ( $V_{GSR} = 20\text{ Vdc}$ , $V_{DS} = 0$ )                                                | $I_{GSSR}$    | —      | 100       | nAdc            |

## ON CHARACTERISTICS (Note 3)

|                                                                                                                                              |              |            |            |      |
|----------------------------------------------------------------------------------------------------------------------------------------------|--------------|------------|------------|------|
| Gate Threshold Voltage ( $V_{DS} = V_{GS}$ , $I_D = 1.0\text{ mAdc}$ )<br>$T_J = 100^\circ\text{C}$                                          | $V_{GS(th)}$ | 2.0<br>1.5 | 4.5<br>4.0 | Vdc  |
| Static Drain-Source On-Resistance ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 3.0\text{ Adc}$ )                                                      | $R_{DS(on)}$ | —          | 0.3        | Ohm  |
| Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ )<br>( $I_D = 6.0\text{ Adc}$ )<br>( $I_D = 3.0\text{ Adc}$ , $T_J = 100^\circ\text{C}$ ) | $V_{DS(on)}$ | —<br>—     | 1.8<br>1.5 | Vdc  |
| Forward Transconductance ( $V_{DS} = 15\text{ Vdc}$ , $I_D = 3.0\text{ Adc}$ )                                                               | $g_{FS}$     | 2.5        | —          | mhos |

## DYNAMIC CHARACTERISTICS

|                              |                                                                                                   |           |   |      |    |
|------------------------------|---------------------------------------------------------------------------------------------------|-----------|---|------|----|
| Input Capacitance            | ( $V_{DS} = 25\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ ,<br>$f = 1.0\text{ MHz}$ )<br>See Figure 11 | $C_{iss}$ | — | 1200 | pF |
| Output Capacitance           |                                                                                                   | $C_{oss}$ | — | 500  |    |
| Reverse Transfer Capacitance |                                                                                                   | $C_{rss}$ | — | 120  |    |

## SWITCHING CHARACTERISTICS\* ( $T_J = 100^\circ\text{C}$ )

|                     |                                                                                                                     |              |           |     |    |
|---------------------|---------------------------------------------------------------------------------------------------------------------|--------------|-----------|-----|----|
| Turn-On Delay Time  | ( $V_{DD} = 25\text{ Vdc}$ , $I_D = 3.0\text{ Adc}$ ,<br>$R_G = 50\ \Omega$ )<br>See Figures 13 and 14              | $t_{d(on)}$  | —         | 50  | ns |
| Rise Time           |                                                                                                                     | $t_r$        | —         | 180 |    |
| Turn-Off Delay Time |                                                                                                                     | $t_{d(off)}$ | —         | 200 |    |
| Fall Time           |                                                                                                                     | $t_f$        | —         | 100 |    |
| Total Gate Charge   | ( $V_{DS} = 0.8\text{ Rated } V_{DSS}$ ,<br>$I_D = \text{Rated } I_D$ , $V_{GS} = 10\text{ Vdc}$ )<br>See Figure 12 | $Q_g$        | 15 (Typ)  | 30  | nC |
| Gate-Source Charge  |                                                                                                                     | $Q_{gs}$     | 8.0 (Typ) | —   |    |
| Gate-Drain Charge   |                                                                                                                     | $Q_{gd}$     | 7.0 (Typ) | —   |    |

## SOURCE-DrAIN DIODE CHARACTERISTICS\*

|                       |                                                                                             |          |                             |     |     |
|-----------------------|---------------------------------------------------------------------------------------------|----------|-----------------------------|-----|-----|
| Forward On-Voltage    | ( $I_S = 6.0\text{ Adc}$ , $di/dt = 25\text{ A}/\mu\text{s}$ ,<br>$V_{GS} = 0\text{ Vdc}$ ) | $V_{SD}$ | 1.3 (Typ)                   | 2.0 | Vdc |
| Forward Turn-On Time  |                                                                                             | $t_{on}$ | Limited by stray inductance |     |     |
| Reverse Recovery Time |                                                                                             | $t_{rr}$ | 325 (Typ)                   | —   | ns  |

3. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

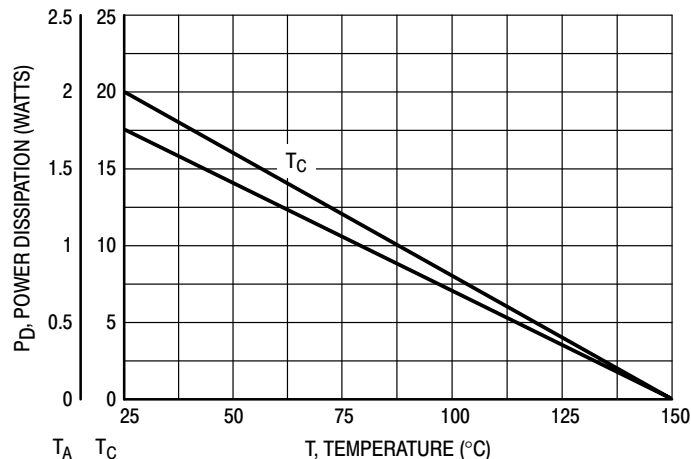


Figure 1. Power Derating

TYPICAL ELECTRICAL CHARACTERISTICS

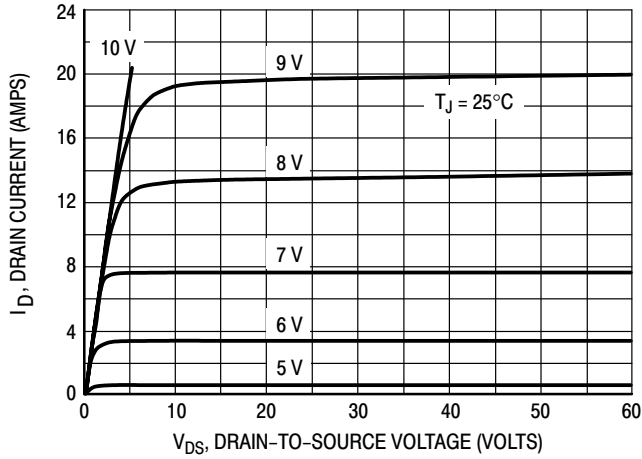


Figure 2. On-Region Characteristics

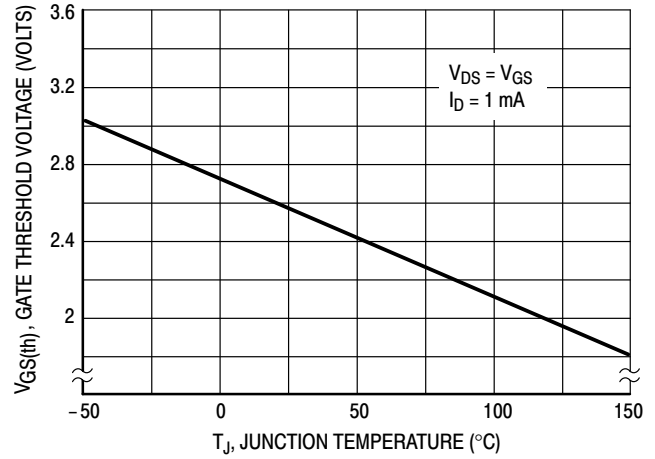


Figure 3. Gate-Threshold Voltage Variation With Temperature

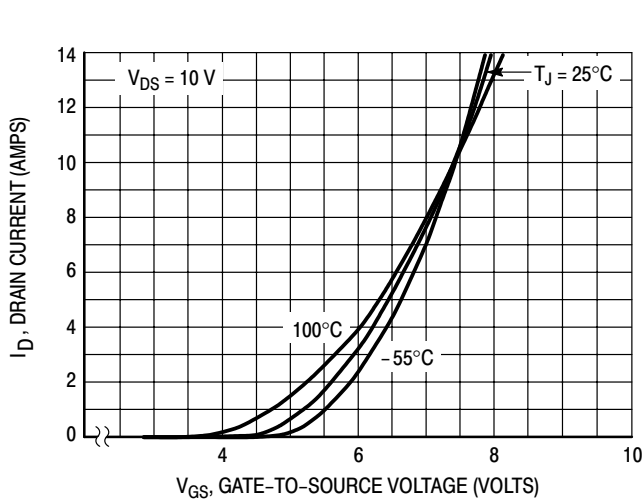


Figure 4. Transfer Characteristics

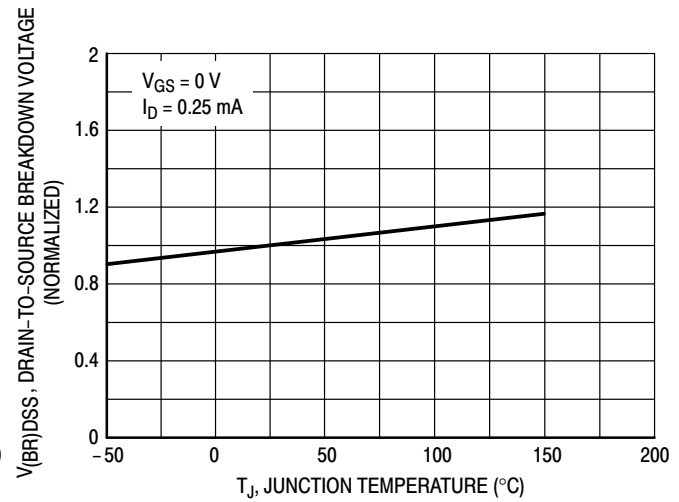


Figure 5. Breakdown Voltage Variation With Temperature

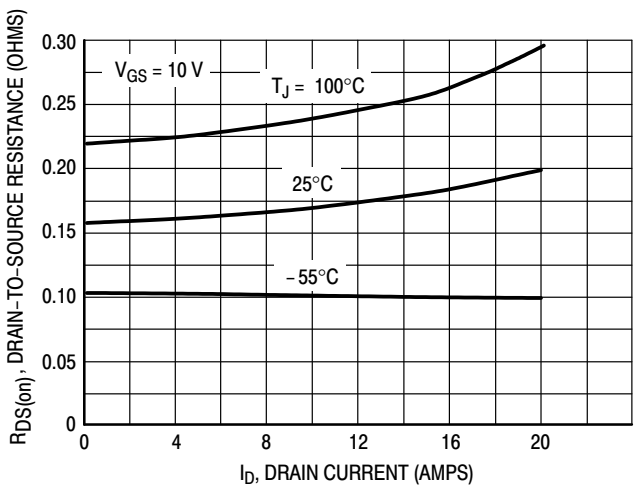


Figure 6. On-Resistance versus Drain Current

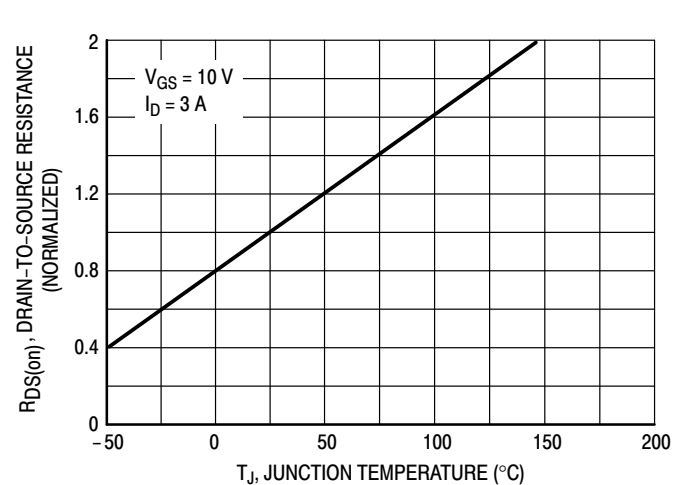


Figure 7. On-Resistance Variation With Temperature

# SAFE OPERATING AREA

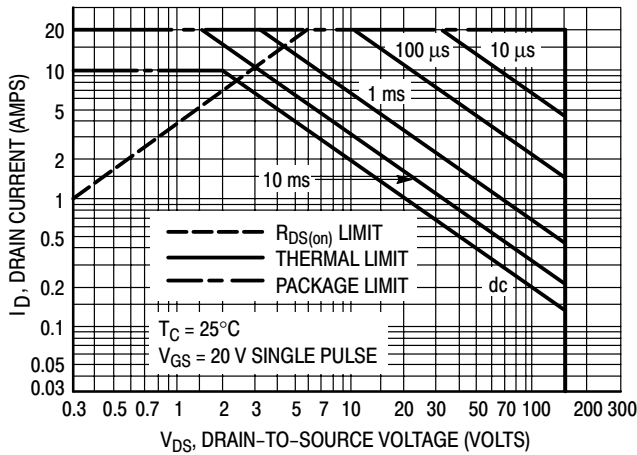


Figure 8. Maximum Rated Forward Biased Safe Operating Area

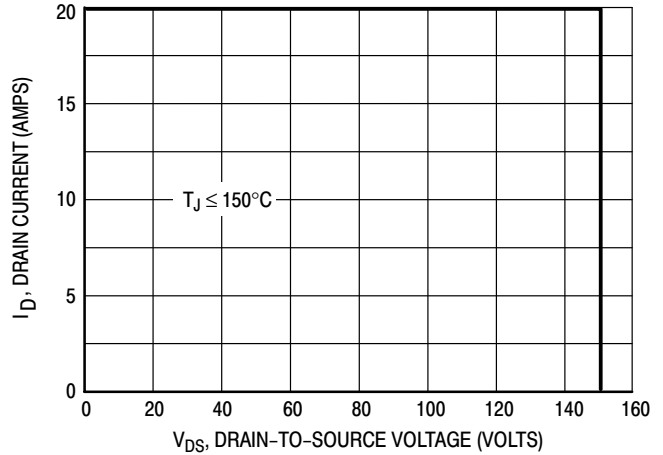


Figure 9. Maximum Rated Switching Safe Operating Area

## FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

## SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current,  $I_{DM}$  and the breakdown voltage,  $V_{(BR)DSS}$ . The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

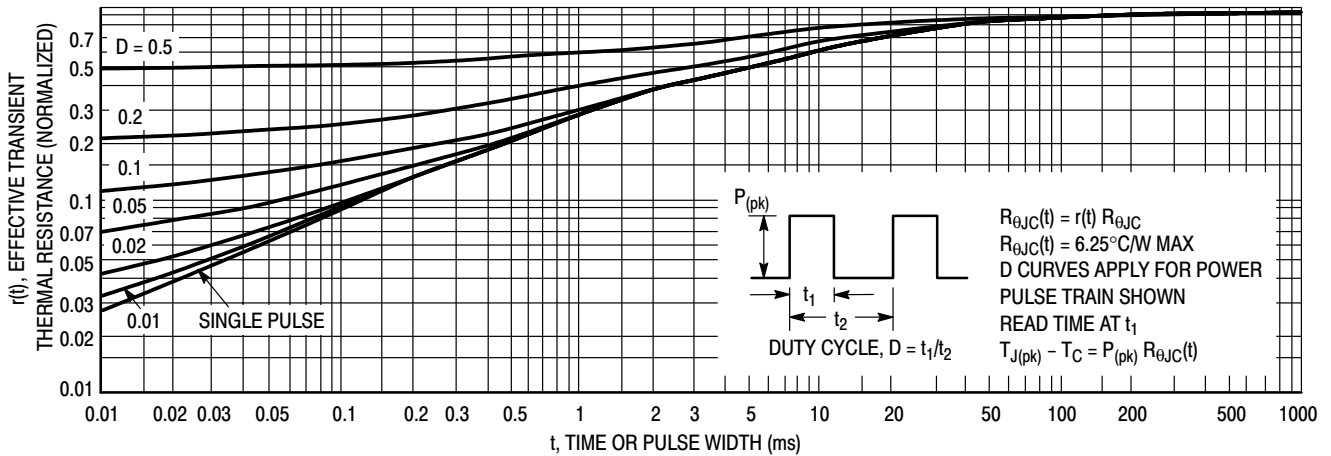


Figure 10. Thermal Response

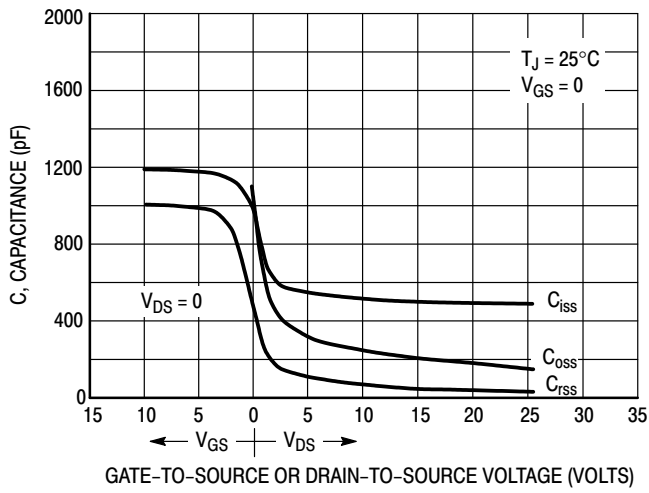


Figure 11. Capacitance Variation

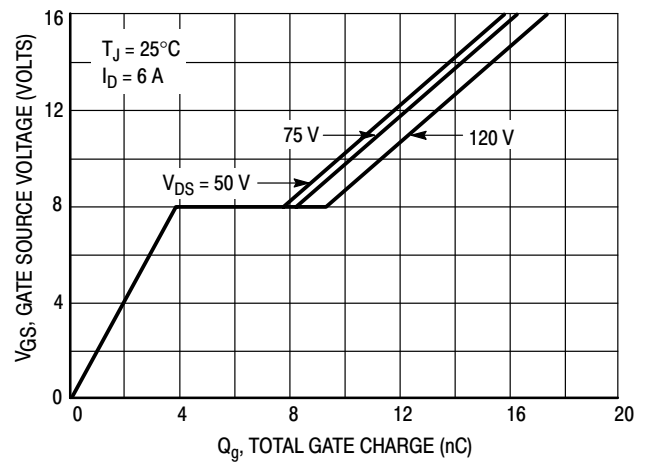


Figure 12. Gate Charge versus Gate-To-Source Voltage

## RESISTIVE SWITCHING

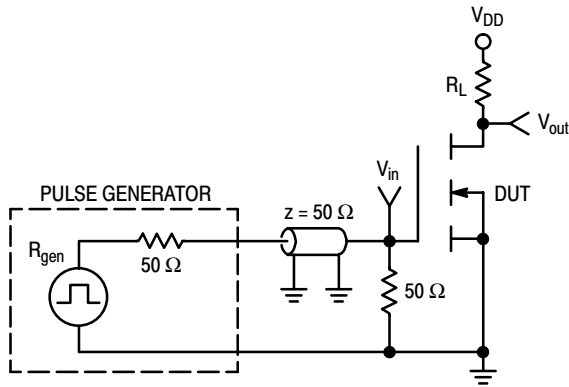


Figure 13. Switching Test Circuit

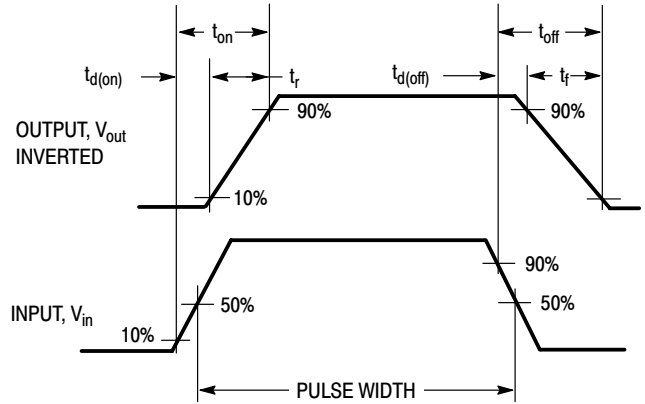
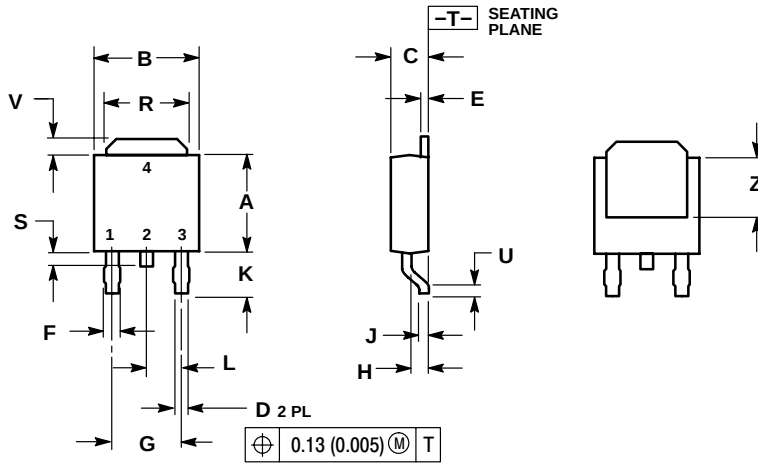


Figure 14. Switching Waveforms

# MTD6N15

## PACKAGE DIMENSIONS

DPAK  
CASE 369C-01  
ISSUE O

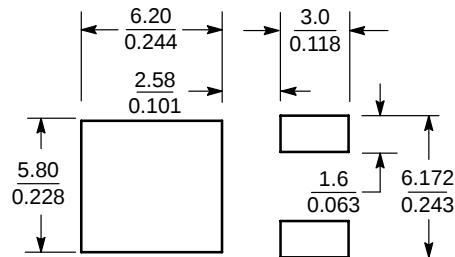


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.

| DIM | INCHES    |       | MILLIMETERS |      |
|-----|-----------|-------|-------------|------|
|     | MIN       | MAX   | MIN         | MAX  |
| A   | 0.235     | 0.245 | 5.97        | 6.22 |
| B   | 0.250     | 0.265 | 6.35        | 6.73 |
| C   | 0.086     | 0.094 | 2.19        | 2.38 |
| D   | 0.027     | 0.035 | 0.69        | 0.88 |
| E   | 0.018     | 0.023 | 0.46        | 0.58 |
| F   | 0.037     | 0.045 | 0.94        | 1.14 |
| G   | 0.180 BSC |       | 4.58 BSC    |      |
| H   | 0.034     | 0.040 | 0.87        | 1.01 |
| J   | 0.018     | 0.023 | 0.46        | 0.58 |
| K   | 0.102     | 0.114 | 2.60        | 2.89 |
| L   | 0.090 BSC |       | 2.29 BSC    |      |
| R   | 0.180     | 0.215 | 4.57        | 5.45 |
| S   | 0.025     | 0.040 | 0.63        | 1.01 |
| U   | 0.020     | ---   | 0.51        | ---  |
| V   | 0.035     | 0.050 | 0.89        | 1.27 |
| Z   | 0.155     | ---   | 3.93        | ---  |

- STYLE 2:
- PIN 1. GATE
  - DRAIN
  - SOURCE
  - DRAIN

## SOLDERING FOOTPRINT\*



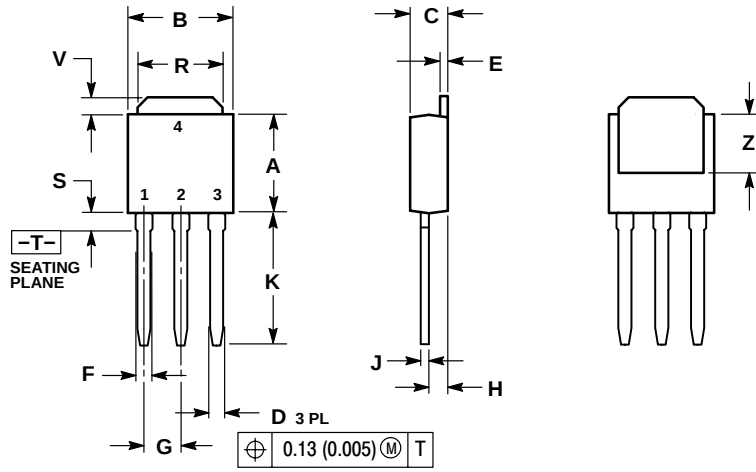
SCALE 3:1  $\left( \frac{\text{mm}}{\text{inches}} \right)$

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MTD6N15

## PACKAGE DIMENSIONS

DPAK  
CASE 369D-01  
ISSUE O



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| DIM | INCHES    |       | MILLIMETERS |      |
|-----|-----------|-------|-------------|------|
|     | MIN       | MAX   | MIN         | MAX  |
| A   | 0.235     | 0.245 | 5.97        | 6.35 |
| B   | 0.250     | 0.265 | 6.35        | 6.73 |
| C   | 0.086     | 0.094 | 2.19        | 2.38 |
| D   | 0.027     | 0.035 | 0.69        | 0.88 |
| E   | 0.018     | 0.023 | 0.46        | 0.58 |
| F   | 0.037     | 0.045 | 0.94        | 1.14 |
| G   | 0.090 BSC |       | 2.29 BSC    |      |
| H   | 0.034     | 0.040 | 0.87        | 1.01 |
| J   | 0.018     | 0.023 | 0.46        | 0.58 |
| K   | 0.350     | 0.380 | 8.89        | 9.65 |
| R   | 0.180     | 0.215 | 4.45        | 5.45 |
| S   | 0.025     | 0.040 | 0.63        | 1.01 |
| V   | 0.035     | 0.050 | 0.89        | 1.27 |
| Z   | 0.155     | ---   | 3.93        | ---  |

### STYLE 2:

- PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA

**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada

**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada

**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada

**Japan:** ON Semiconductor, Japan Customer Focus Center  
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051  
**Phone:** 81-3-5773-3850

**ON Semiconductor Website:** <http://onsemi.com>

**Order Literature:** <http://www.onsemi.com/litorder>

For additional information, please contact your  
local Sales Representative.