MMBT2907ALT1

General Purpose Transistors

PNP Silicon

Feature

- Pb−Free Package May be Available. The G−Suffix Denotes a Pb−Free Lead Finish

MAXIMUM RATINGS

Rating	Symbol	2907A	Unit
Collector−Emitter Voltage	V_{CEO}	−60	Vdc
Collector−Base Voltage	V_{CBO}	−60	Vdc
Emitter−Base Voltage	V_{EBO}	−5.0	Vdc
Collector Current − Continuous	I_C	−600	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR−5 Board (Note 1) T_A = 25°C Derate above 25°C	P_D	 225 1.8	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	556	°C/W
Total Device Dissipation Alumina Substrate, (Note 2) T_A = 25°C Derate above 25°C	P_D	300 2.4	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	417	°C/W
Junction and Storage Temperature	T_J, T_{stg}	−55 to +150	°C

1. FR−5 = 1.0 × 0.75 × 0.062 in.
2. Alumina = 0.4 × 0.3 × 0.024 in. 99.5% alumina.

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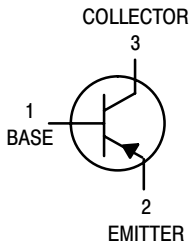
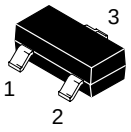
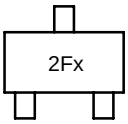




SOT−23 (TO−236AB)
CASE 318
STYLE 6

DEVICE MARKING



x = Monthly Date Code

ORDERING INFORMATION

Device	Package	Shipping†
MMBT2907ALT1	SOT−23	3000 Units/Reel
MMBT2907ALT3G	SOT−23	3000 Units/Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Breakdown Voltage (Note 3) (I_C = −10 mAdc, I_B = 0)	$V_{(BR)CEO}$	−60	−	Vdc
Collector−Base Breakdown Voltage (I_C = −10 μAdc, I_E = 0)	$V_{(BR)CBO}$	−60	−	Vdc
Emitter−Base Breakdown Voltage (I_E = −10 μAdc, I_C = 0)	$V_{(BR)EBO}$	−5.0	−	Vdc
Collector Cutoff Current (V_{CE} = −30 Vdc, $V_{BE(off)}$ = −0.5 Vdc)	I_{CEX}	−	−50	nAdc
Collector Cutoff Current (V_{CB} = −50 Vdc, I_E = 0) (V_{CB} = −50 Vdc, I_E = 0, T_A = 125°C)	I_{CBO}	− −	−0.010 −10	μAdc
Base Current (V_{CE} = −30 Vdc, $V_{EB(off)}$ = −0.5 Vdc)	I_B	−	−50	nAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = −0.1 mAdc, V_{CE} = −10 Vdc) (I_C = −1.0 mAdc, V_{CE} = −10 Vdc) (I_C = −10 mAdc, V_{CE} = −10 Vdc) (I_C = −150 mAdc, V_{CE} = −10 Vdc) (I_C = −500 mAdc, V_{CE} = −10 Vdc) (Note 3)	h_{FE}	 75 100 100 100 50	 − − − 300 −	−
Collector−Emitter Saturation Voltage (Note 3) (I_C = −150 mAdc, I_B = −15 mAdc) (Note 3) (I_C = −500 mAdc, I_B = −50 mAdc)	$V_{CE(sat)}$	 − −	 −0.4 −1.6	Vdc
Base−Emitter Saturation Voltage (Note 3) (I_C = −150 mAdc, I_B = −15 mAdc) (I_C = −500 mAdc, I_B = −50 mAdc)	$V_{BE(sat)}$	 − −	 −1.3 −2.6	Vdc
SMALL−SIGNAL CHARACTERISTICS				
Current−Gain − Bandwidth Product (Notes 3, 4) (I_C = −50 mAdc, V_{CE} = −20 Vdc, f = 100 MHz)	f_T	200	−	MHz
Output Capacitance (V_{CB} = −10 Vdc, I_E = 0, f = 1.0 MHz)	C_{obo}	−	8.0	pF
Input Capacitance (V_{EB} = −2.0 Vdc, I_C = 0, f = 1.0 MHz)	C_{ibo}	−	30	
SWITCHING CHARACTERISTICS				
Turn−On Time	(V_{CC} = −30 Vdc, I_C = −150 mAdc, I_{B1} = −15 mAdc)	t_{on}	−	45	ns
Delay Time		t_d	−	10	
Rise Time		t_r	−	40	
Turn−Off Time	(V_{CC} = −6.0 Vdc, I_C = −150 mAdc, I_{B1} = I_{B2} = −15 mAdc)	t_{off}	−	100	
Storage Time		t_s	−	80	
Fall Time		t_f	−	30	

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
4. f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

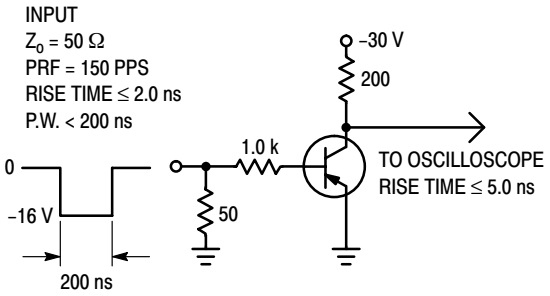


Figure 1. Delay and Rise Time Test Circuit

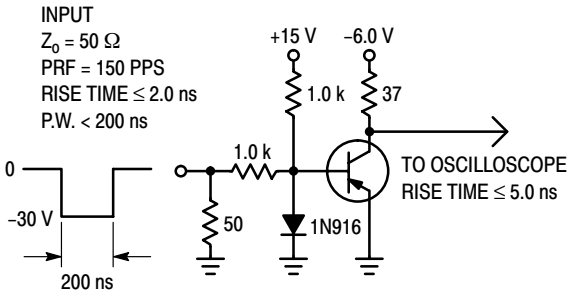


Figure 2. Storage and Fall Time Test Circuit

TYPICAL CHARACTERISTICS

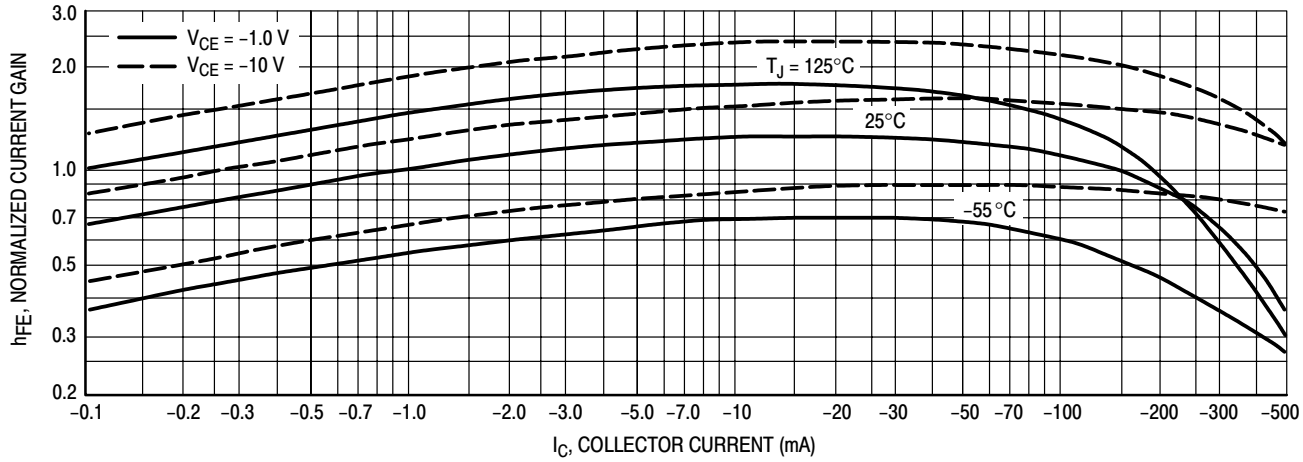


Figure 3. DC Current Gain

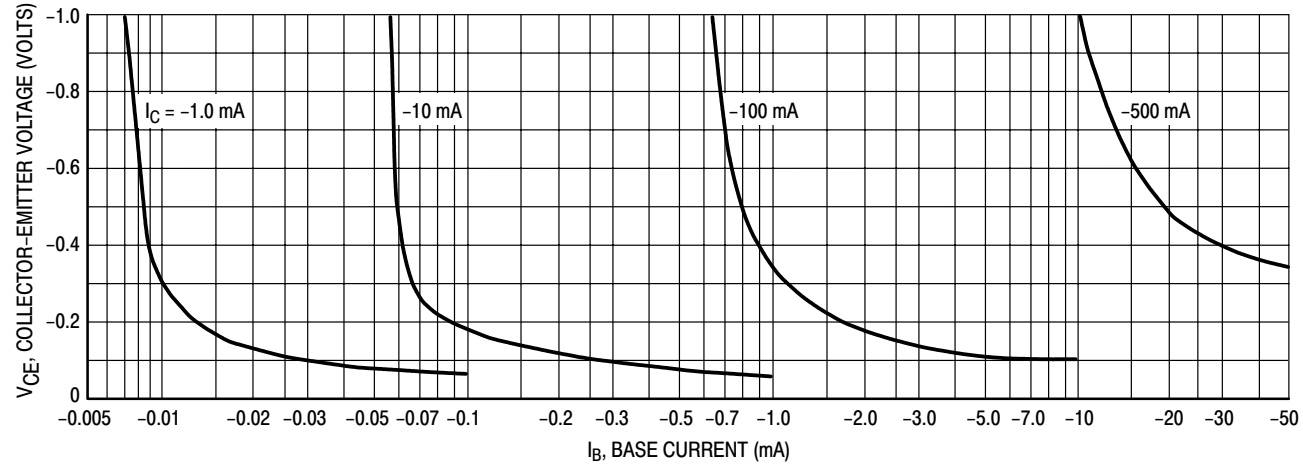


Figure 4. Collector Saturation Region

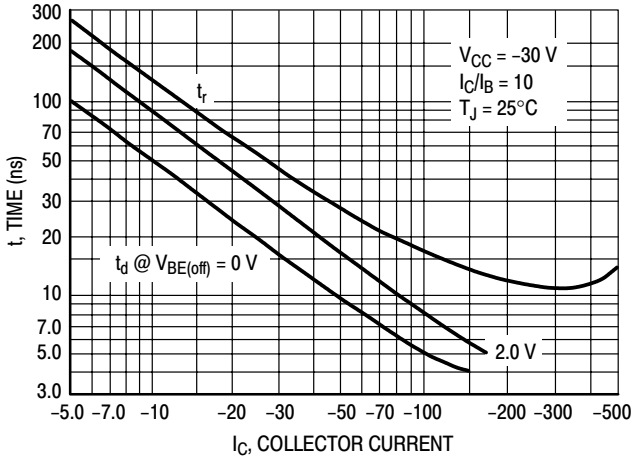


Figure 5. Turn−On Time

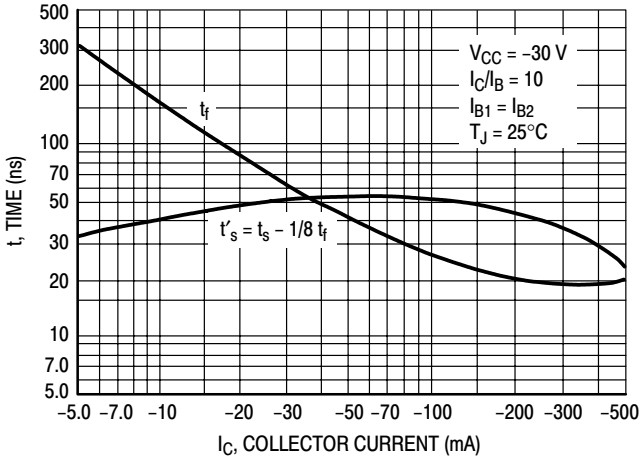


Figure 6. Turn−Off Time

TYPICAL SMALL−SIGNAL Characteristics

NOISE FIGURE

V_{CE} = 10 Vdc, T_A = 25°C

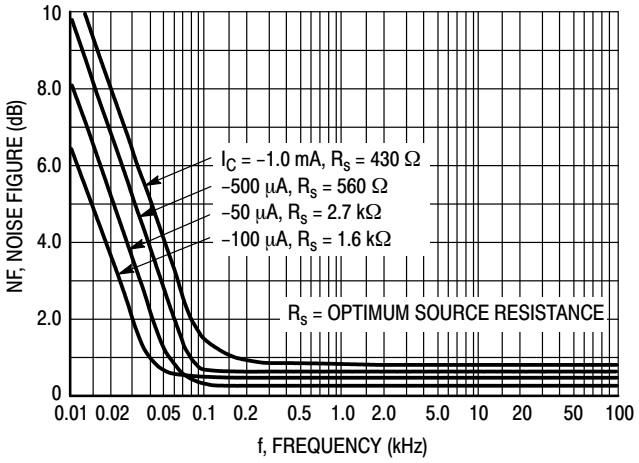


Figure 7. Frequency Effects

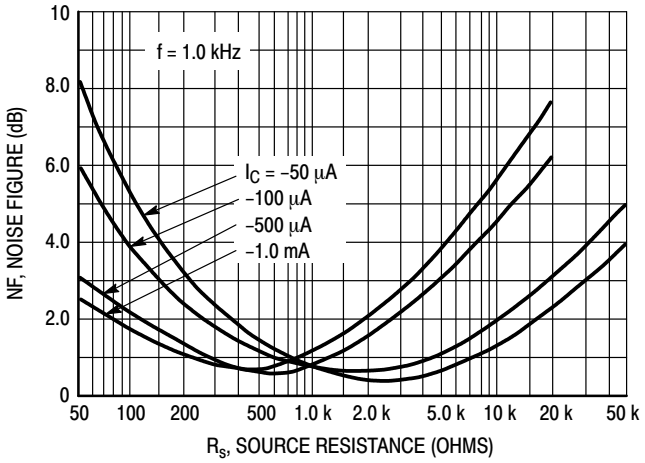


Figure 8. Source Resistance Effects

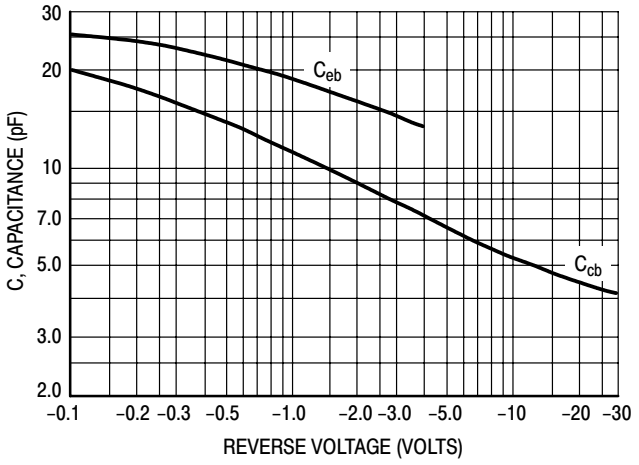


Figure 9. Capacitances

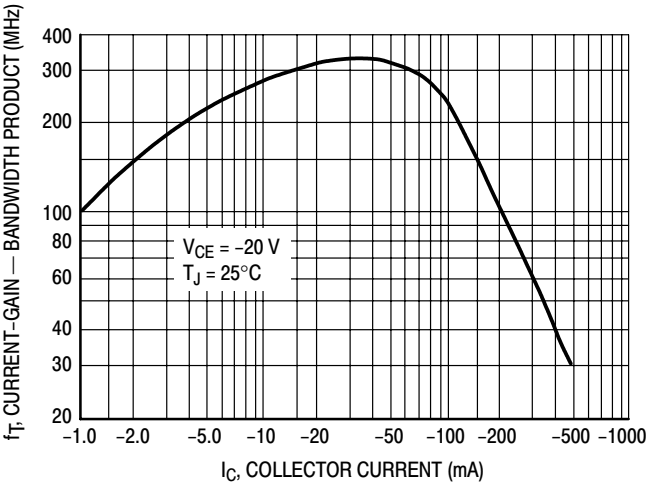


Figure 10. Current−Gain − Bandwidth Product

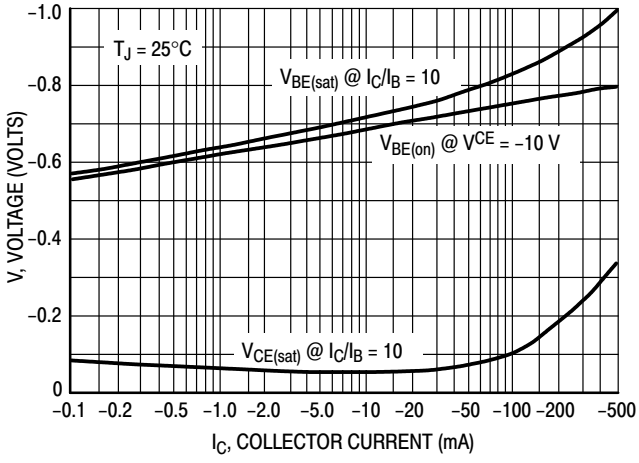


Figure 11. “On” Voltage

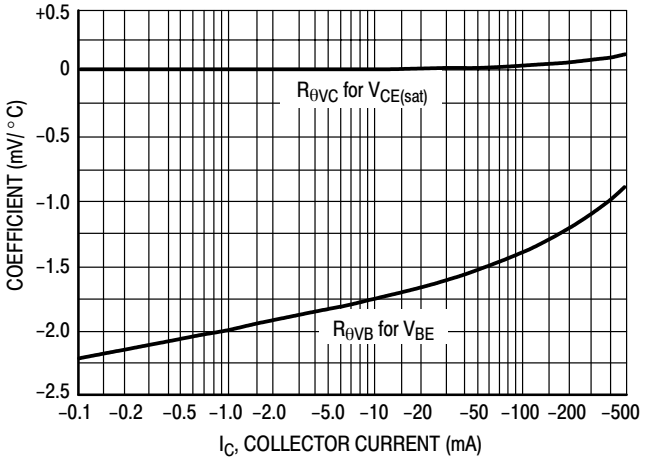
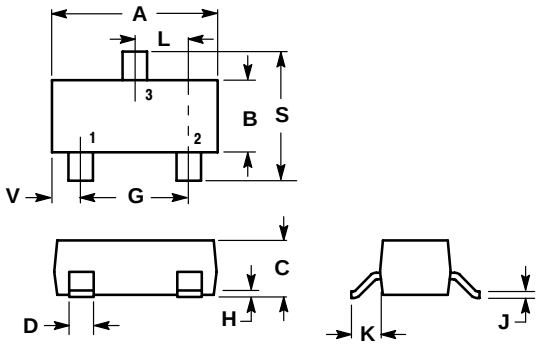


Figure 12. Temperature Coefficients

PACKAGE DIMENSIONS

SOT−23 (TO−236AB)
CASE 318−08
ISSUE AH



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318−03 AND −07 OBSOLETE, NEW STANDARD 318−08.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

SOLDERING FOOTPRINT*

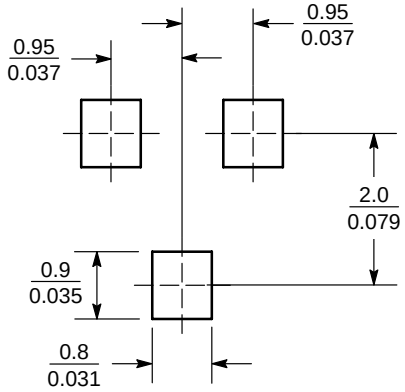


Figure 13. SOT−23

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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