

Silicon Power Transistors

The MJL21195 and MJL21196 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

- Total Harmonic Distortion Characterized
- High DC Current Gain – $h_{FE} = 25 \text{ Min @ } I_C = 8 \text{ Adc}$
- Excellent Gain Linearity
- High SOA: 2.50 A, 80 V, 1 Second

MAXIMUM RATINGS

Rating	Symbo l	Value	Unit
Collector–Emitter Voltage	V_{CEO}	250	Vdc
Collector–Base Voltage	V_{CBO}	400	Vdc
Emitter–Base Voltage	V_{EBO}	5	Vdc
Collector–Emitter Voltage – 1.5 V	V_{CEX}	400	Vdc
Collector Current — Continuous Peak (1)	I_C	16 30	Adc
Base Current – Continuous	I_B	5	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate Above 25°C	P_D	200 1.43	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	$^\circ\text{C}$

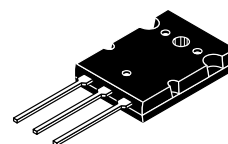
THERMAL CHARACTERISTICS

Characteristic	Sym- bol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	$^\circ\text{C/W}$

PNP
MJL21195*
NPN
MJL21196*

*ON Semiconductor Preferred Device

**16 AMPERE
COMPLEMENTARY
SILICON POWER
TRANSISTORS
250 VOLTS
200 WATTS**



**CASE 340G-02
TO-3PBL**

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

MJL21195 MJL21196

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
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OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (I _C = 100 mAdc, I _B = 0)	V _{CEO(sus)}	250	—	—	Vdc
Collector Cutoff Current (V _{CE} = 200 Vdc, I _B = 0)	I _{CEO}	—	—	100	μAdc

(1) Pulse Test: Pulse Width = 5.0 μs, Duty Cycle ≤10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
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OFF CHARACTERISTICS

Emitter Cutoff Current (V _{CE} = 5 Vdc, I _C = 0)	I _{EBO}	—	—	100	μAdc
Collector Cutoff Current (V _{CE} = 250 Vdc, V _{BE(off)} = 1.5 Vdc)	I _{CEX}	—	—	100	μAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased (V _{CE} = 50 Vdc, t = 1 s (non-repetitive) (V _{CE} = 80 Vdc, t = 1 s (non-repetitive)	I _{S/b}	4.0 2.25	— —	— —	Adc
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ON CHARACTERISTICS

DC Current Gain (I _C = 8 Adc, V _{CE} = 5 Vdc) (I _C = 16 Adc, I _B = 5 Adc)	h _{FE}	25 8	— —	100 —	
Base–Emitter On Voltage (I _C = 8 Adc, V _{CE} = 5 Vdc)	V _{BE(on)}	—	—	2.2	Vdc
Collector–Emitter Saturation Voltage (I _C = 8 Adc, I _B = 0.8 Adc) (I _C = 16 Adc, I _B = 3.2 Adc)	V _{CE(sat)}	— —	— —	1.4 4	Vdc

DYNAMIC CHARACTERISTICS

Total Harmonic Distortion at the Output V _{RMS} = 28.3 V, f = 1 kHz, P _{LOAD} = 100 W _{RMS} (Matched pair h _{FE} = 50 @ 5 A/5 V) h _{FE} unmatched h _{FE} matched	T _{HD}	— —	0.8 0.08	— —	%
Current Gain Bandwidth Product (I _C = 1 Adc, V _{CE} = 10 Vdc, f _{test} = 1 MHz)	f _T	4	—	—	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f _{test} = 1 MHz)	C _{ob}	—	—	500	pF

(2) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤2%

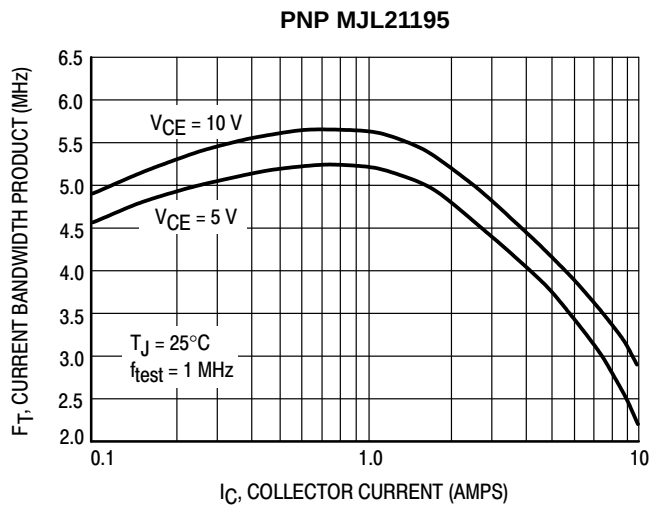


Figure 1. Typical Current Gain Bandwidth Product

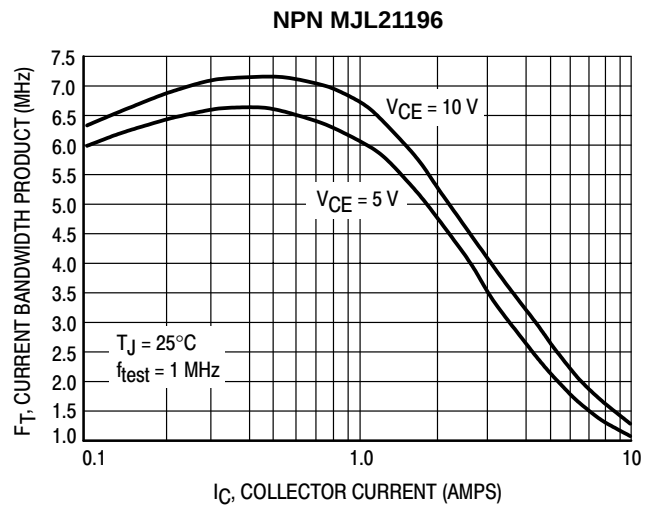


Figure 2. Typical Current Gain Bandwidth Product

TYPICAL CHARACTERISTICS

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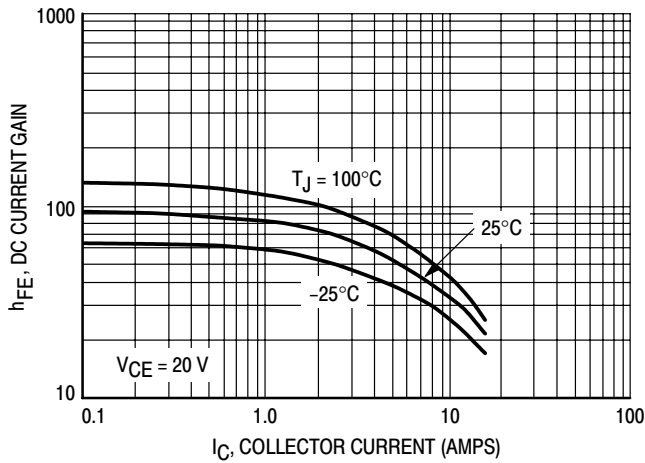


Figure 3. DC Current Gain, $V_{CE} = 20\text{ V}$

NPN MJL21196

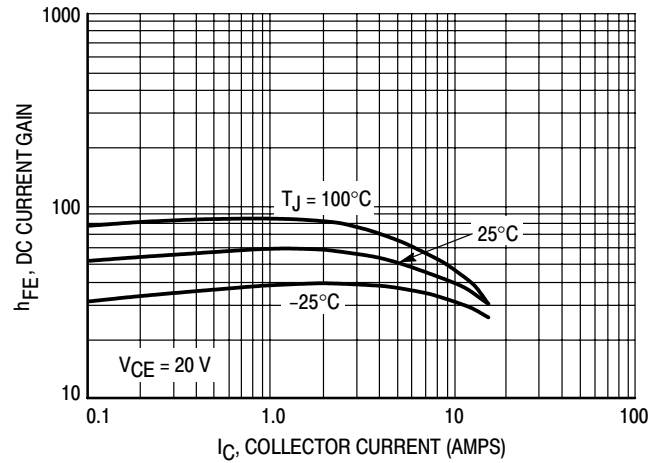


Figure 4. DC Current Gain, $V_{CE} = 20\text{ V}$

PNP MJL21195

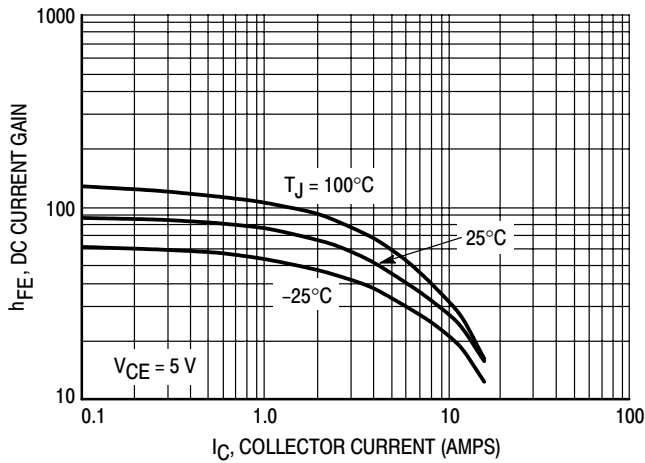


Figure 5. DC Current Gain, $V_{CE} = 5\text{ V}$

NPN MJL21196

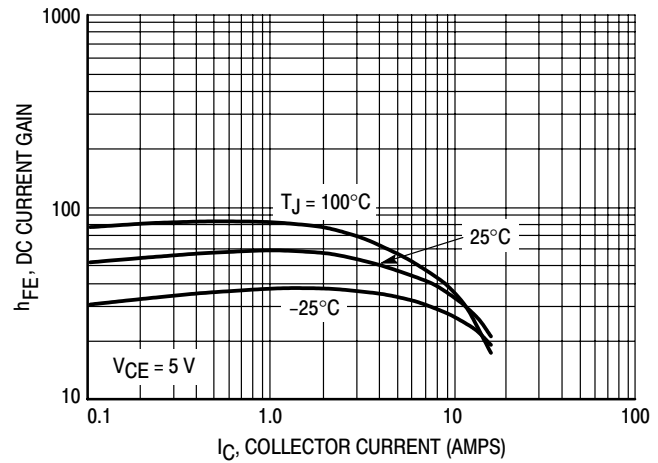


Figure 6. DC Current Gain, $V_{CE} = 5\text{ V}$

PNP MJL21195

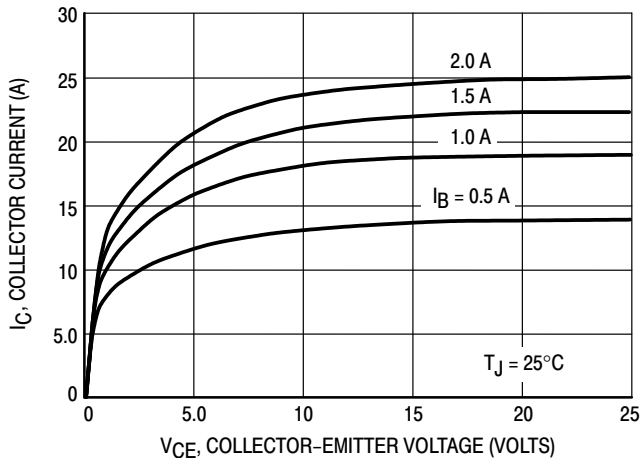


Figure 7. Typical Output Characteristics

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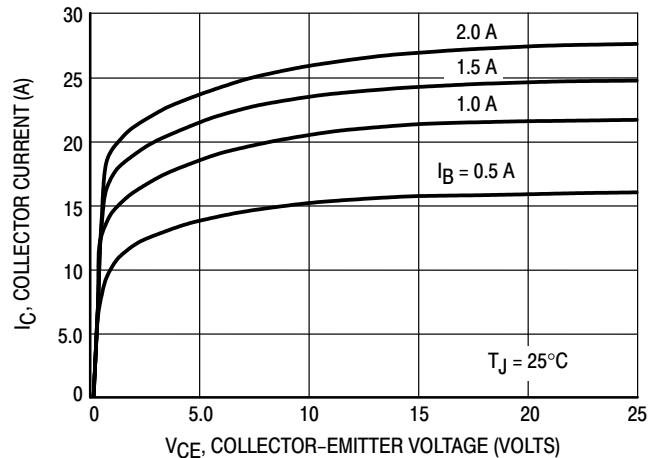


Figure 8. Typical Output Characteristics

TYPICAL CHARACTERISTICS

PNP MJL21195

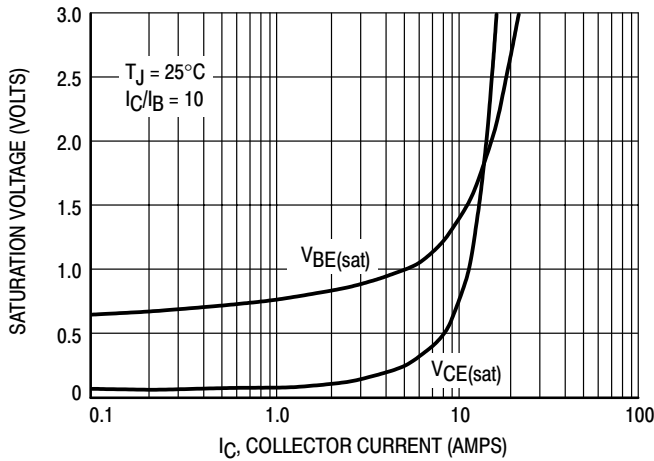


Figure 9. Typical Saturation Voltages

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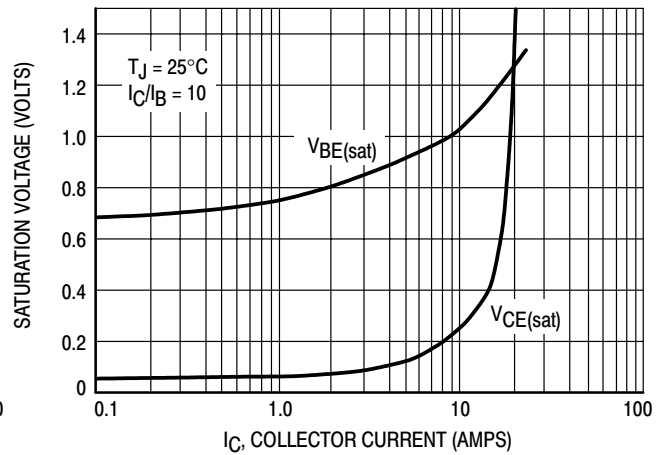


Figure 10. Typical Saturation Voltages

PNP MJL21195

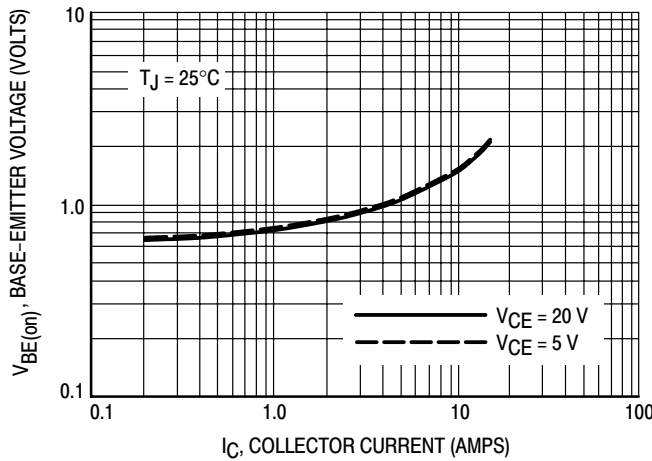


Figure 11. Typical Base-Emitter Voltage

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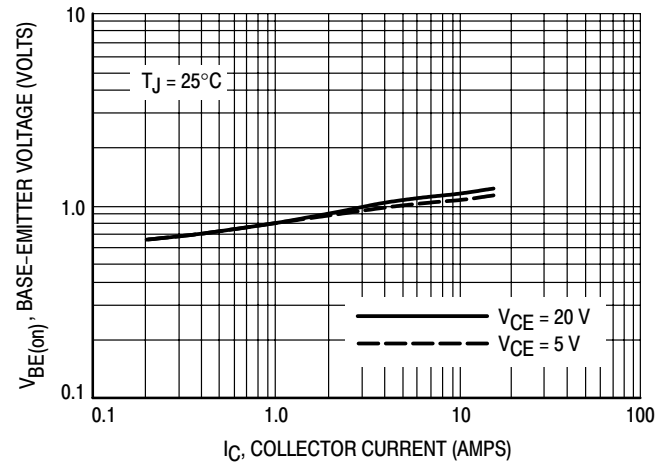


Figure 12. Typical Base-Emitter Voltage

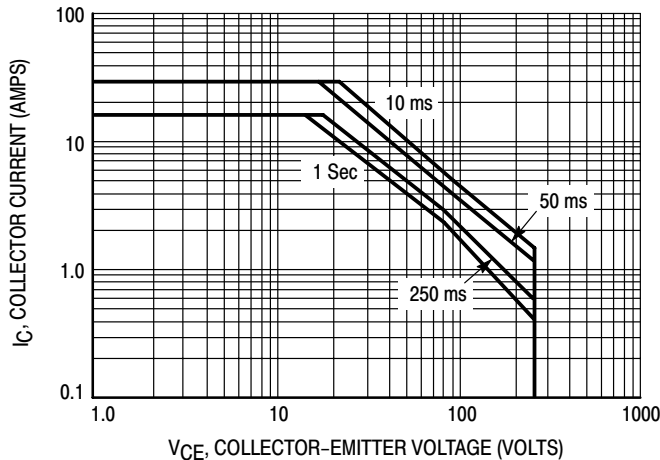


Figure 13. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

MJL21195 MJL21196

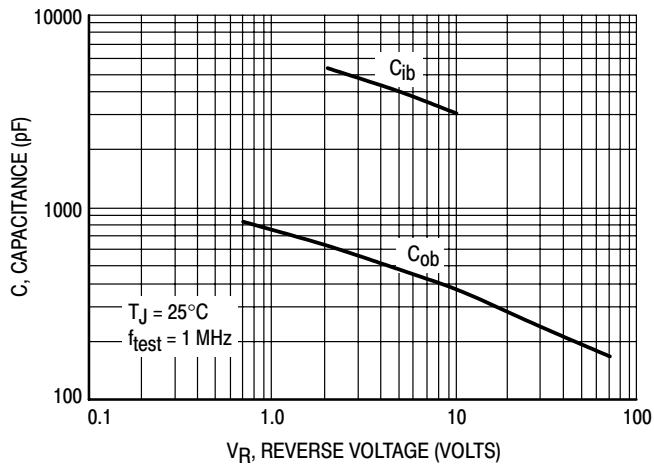


Figure 14. MJL21195 Typical Capacitance

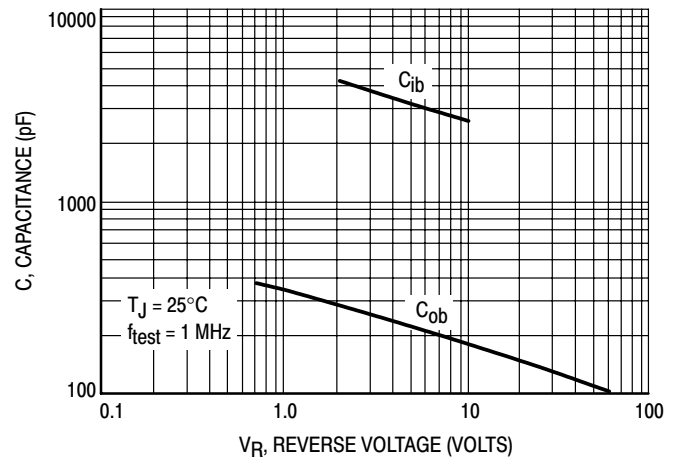


Figure 15. MJL21196 Typical Capacitance

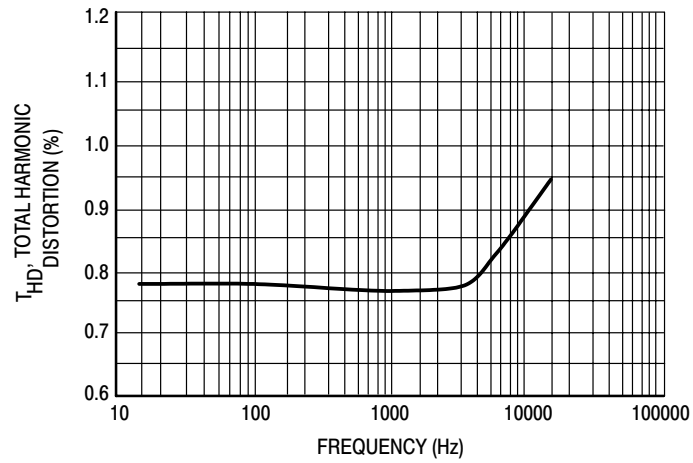


Figure 16. Typical Total Harmonic Distortion

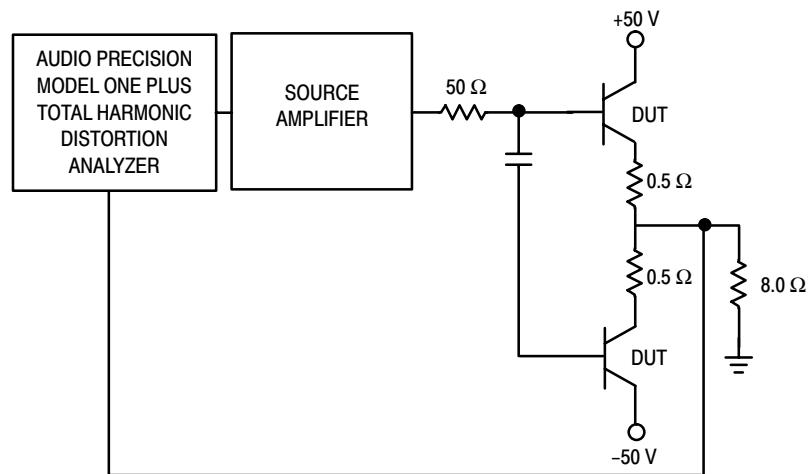
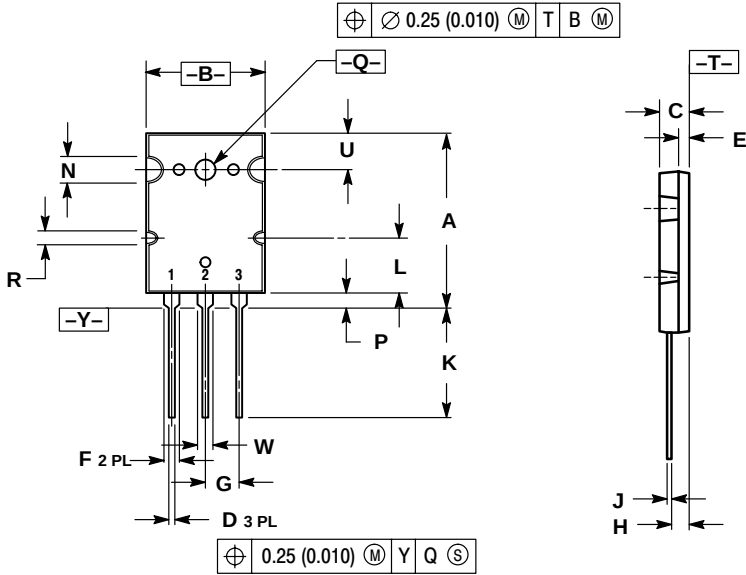


Figure 17. Total Harmonic Distortion Test Circuit

MJL21195 MJL21196

PACKAGE DIMENSIONS

TO-3PBL (TO-264)
CASE 340G-02
ISSUE H



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	28.0	29.0	1.102	1.142
B	19.3	20.3	0.760	0.800
C	4.7	5.3	0.185	0.209
D	0.93	1.48	0.037	0.058
E	1.9	2.1	0.075	0.083
F	2.2	2.4	0.087	0.102
G	5.45 BSC		0.215 BSC	
H	2.6	3.0	0.102	0.118
J	0.43	0.78	0.017	0.031
K	17.6	18.8	0.693	0.740
L	11.0	11.4	0.433	0.449
N	3.95	4.75	0.156	0.187
P	2.2	2.6	0.087	0.102
Q	3.1	3.5	0.122	0.137
R	2.15	2.35	0.085	0.093
U	6.1	6.5	0.240	0.256
W	2.8	3.2	0.110	0.125

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