

Low Voltage Bias Stabilizer with Enable

- Maintains Stable Bias Current in N-Type Discrete Bipolar Junction and Field Effect Transistors
- Provides Stable Bias Using a Single Component Without Use of Emitter Ballast and Bypass Components
- Operates Over a Wide Range of Supply Voltages Down to 1.8 Vdc
- Reduces Bias Current Variation Due to Temperature and Unit-to-Unit Parametric Changes
- Consumes < 0.5 mW at $V_{CC} = 2.75$ V
- Active High Enable is CMOS Compatible

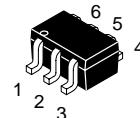
This device provides a reference voltage and acts as a DC feedback element around an external discrete, NPN BJT or N-Channel FET. It allows the external transistor to have its emitter/source directly grounded and still operate with a stable collector/drain DC current. It is primarily intended to stabilize the bias of discrete RF stages operating from a low voltage regulated supply, but can also be used to stabilize the bias current of any linear stage in order to eliminate emitter/source bypassing and achieve tighter bias regulation over temperature and unit variations. The "ENABLE" polarity nulls internal current, Enable current, and RF transistor current in "STANDBY." This device is intended to replace a circuit of three to six discrete components.

The combination of low supply voltage, low quiescent current drain, and small package make the MDC5001T1 ideal for portable communications applications such as:

- Cellular Telephones
- Pagers
- PCN/PCS Portables
- GPS Receivers
- PCMCIA RF Modems
- Cordless Phones
- Broadband and Multiband Transceivers and Other Portable Wireless Products

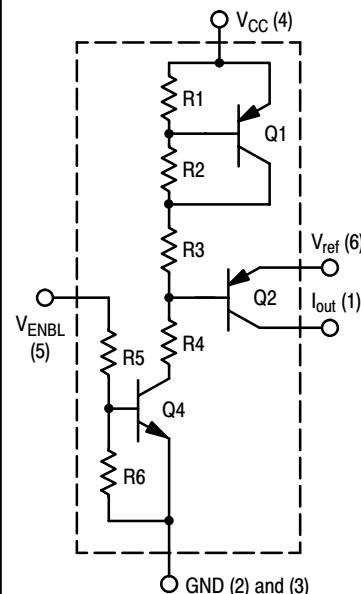
MDC5001T1

**SILICON
SMALLBLOCK™
INTEGRATED CIRCUIT**



**CASE 419B-01, Style 19
SOT-363**

INTERNAL CIRCUIT DIAGRAM



MDC5001T1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	15	Vdc
Ambient Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature	T_J	150	°C
Collector Emitter Voltage (Q2)	V_{CEO}	-15	V
Enable Voltage (Pin 5)	V_{ENBL}	V_{CC}	V

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Power Dissipation (FR-5 PCB of 1" x 0.75" x 0.062", $T_A = 25^\circ\text{C}$) Derate above 25°C	P_D	150 1.2	mW mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	833	°C/W

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Recommended Operating Supply Voltage	V_{CC}	1.8	2.75	10	Volts
Power Supply Current ($V_{CC} = 2.75$ V) V_{ref} , I_{out} are unterminated See Figure 8	I_{CC}	—	130	200	µA
Q2 Collector Emitter Breakdown Voltage ($I_{C2} = 10$ µA, $I_{B2} = 0$)	$V_{(BR)CEO2}$	15			Volts
Reference Voltage ($V_{ENBL} = V_{CC} = 2.75$ V, $V_{out} = 0.7$ V) ($I_{out} = 30$ µA) ($I_{out} = 150$ µA) See Figure 1	V_{ref}	2.050 2.110	2.075 2.135	2.100 2.160	Volts
Reference Voltage ($V_{ENBL} = V_{CC} = 2.75$ V, $V_{out} = 0.7$ V, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$) V_{CC} Pulse Width = 10 mS, Duty Cycle = 1% ($I_{out} = 10$ µA) ($I_{out} = 30$ µA) ($I_{out} = 100$ µA) See Figures 2 and 11	ΔV_{ref}		± 5.0 ± 15 ± 25	± 10 ± 30 ± 50	mV

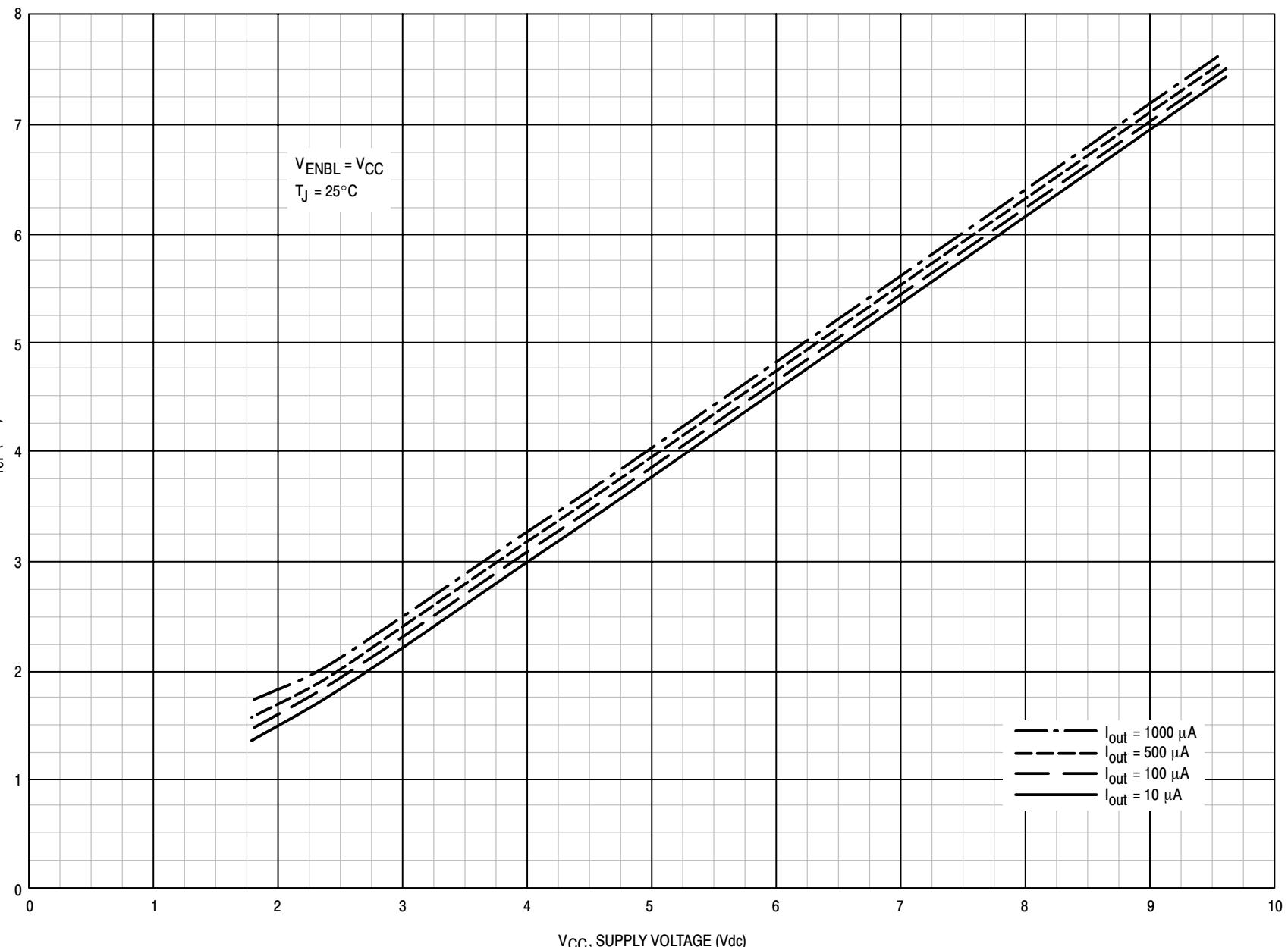
MDC5001T1

The following SPICE models are provided as a convenience to the user and every effort has been made to insure their accuracy. However, no responsibility for their accuracy is assumed by ON Semiconductor.

.MODEL Q4 NPN		.MODEL Q1, Q2 PNP		RESISTOR VALUES
BF = 136	NE = 1.6	BF = 87	NK = 0.5	R1 = 12 K
BR = 0.2	NF = 1.005	BR = 0.6	NR = 1.0	R2 = 6 K
CJC = 318.6 f	RB = 140	CJC = 800E-15	RB = 720	R3 = 3.4 K
CJE = 569.2 f	RBM = 70	CJE = 46E-15	RBM = 470	R4 = 12 K
CJS = 1.9 p	RC = 180	EG = 1.215	RC = 180	R5 = 20 K
EG = 1.215	RE = 1.6	FC = 0.5	RE = 26	R6 = 40 K
FC = 0.5	TF = 553.6 p	IKF = 3.8E-04	TF = 15E-9	
IKF = 24.41 m	TR = 10 n	IKR = 2.0	TR = 50E-09	
IKR = 0.25	VAF = 267.6	IRB = 0.9E-3	VAF = 54.93	
IRB = 0.0004	VAR = 12	IS = 1.027E-15	VAR = 20	
IS = 256E-18	VJC = 0.4172	ISC = 10E-18	VAR = 20	
ISC = 1 f	VJE = 0.7245	ISE = 1.8E-15	VJC = 0.4172	
ISE = 500E-18	VJS = 0.39	ITF = 2E-3	VJE = 0.4172	
ITF = 0.9018	VTF = 10	MJC = 0.2161	VTF = 10	
MJC = 0.2161	XTB = 1.5	MJE = 0.2161	XTB = 1.5	
MJE = 0.3373	XTF = 2.077	NC = 0.8	XTF = 2.0	
MJS = 0.13	XTI = 3	NE = 1.38	XTI = 3	
NC = 1.09		NF = 1.015		

These models can be retrieved electronically by accessing the ON Semiconductor Web page at <http://design-net.sps.mot.com/models> and searching the section on SMALLBLOCK™ models

TYPICAL OPEN LOOP CHARACTERISTICS



TYPICAL OPEN LOOP CHARACTERISTICS

(Refer to Circuits of Figures 10 through 15)

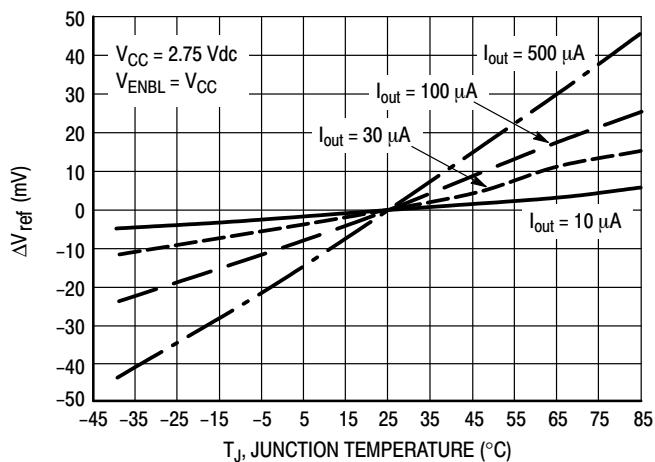


Figure 2. ΔV_{ref} versus T_J @ I_{out}

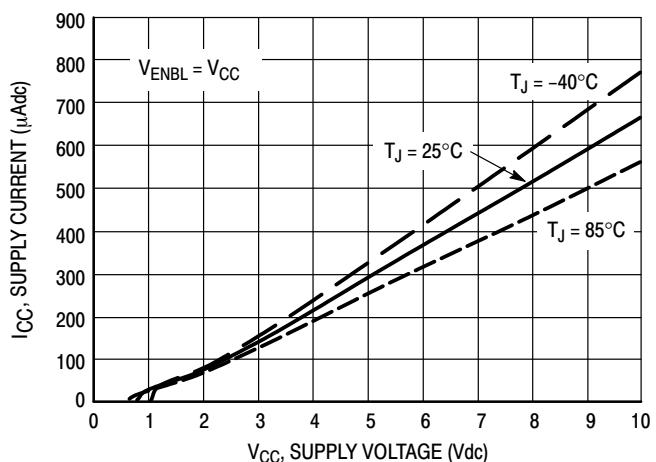


Figure 3. I_{cc} versus V_{cc} @ T_J

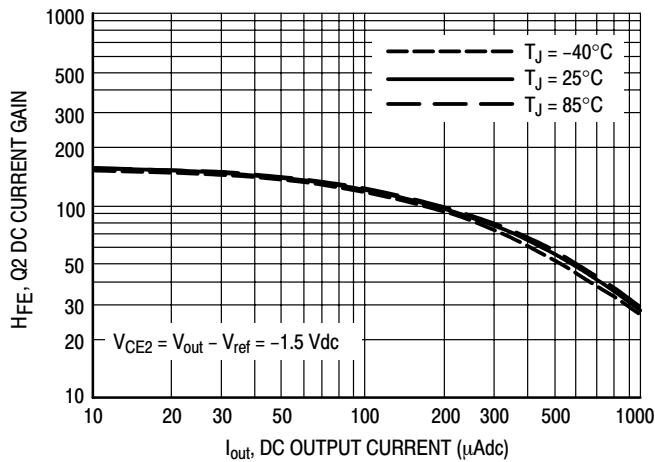


Figure 4. Q2 Current Gain versus Output Current @ T_J

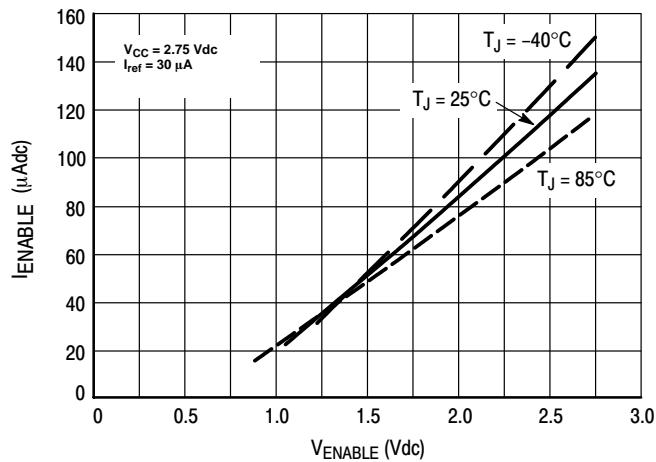


Figure 5. I_{enable} versus V_{enable}

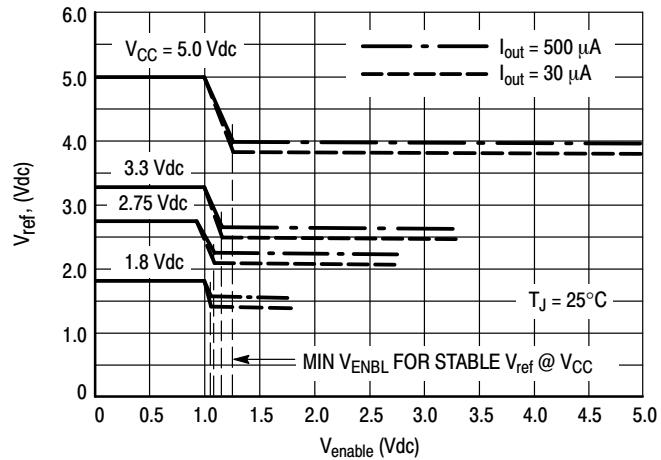


Figure 6. V_{ref} versus V_{enable} @ V_{cc} and I_{out}

TYPICAL CLOSED LOOP PERFORMANCE

(Refer to Circuits of Figures 16 & 17)

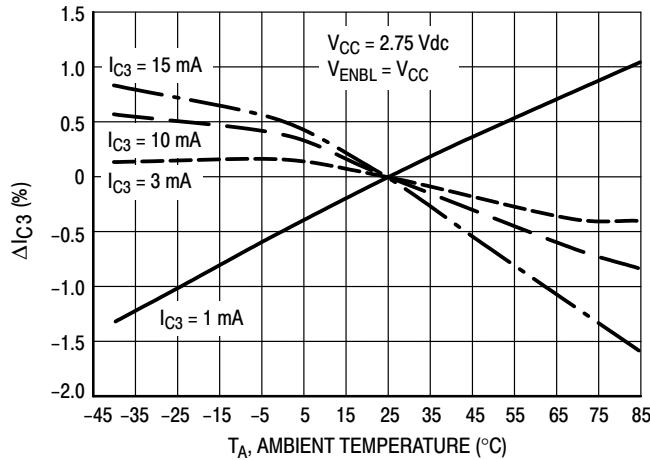


Figure 7. ΔI_{C3} versus T_A @ I_{C3}

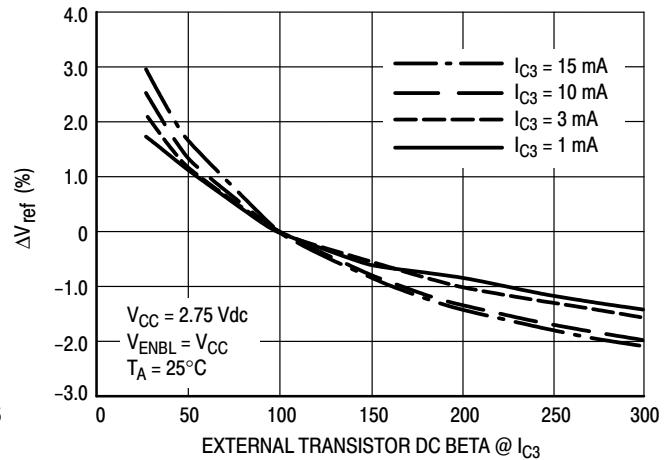


Figure 8. ΔV_{ref} versus External Transistor DC Beta @ I_{C3}

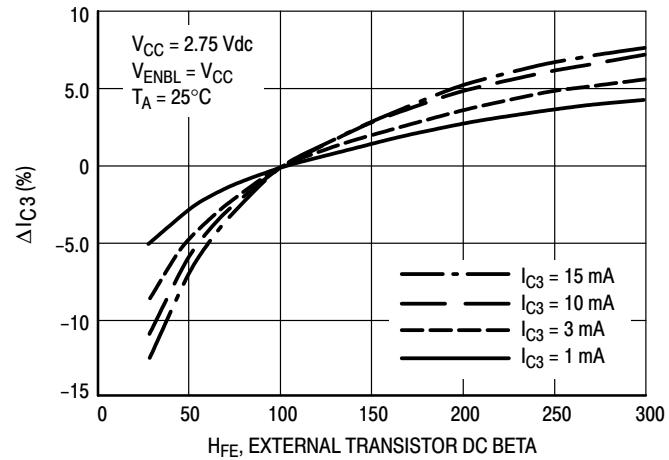


Figure 9. ΔI_{C3} versus External Transistor DC Beta @ I_{C3}

OPEN LOOP TEST CIRCUITS

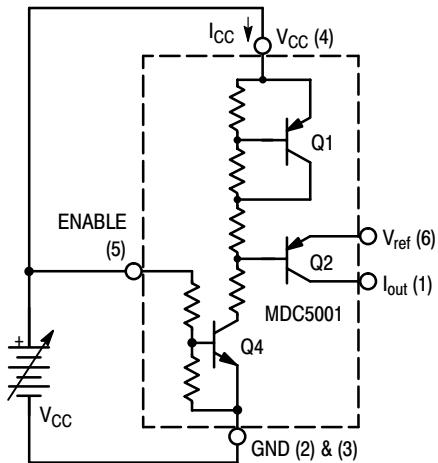


Figure 10. I_{CC} versus V_{CC} Test Circuit

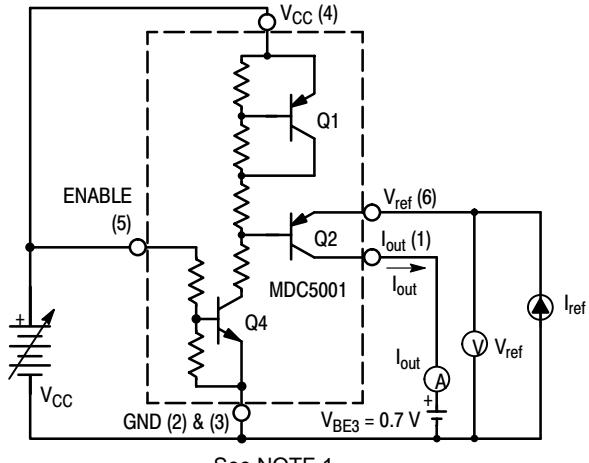


Figure 11. V_{ref} versus V_{CC} Test Circuit

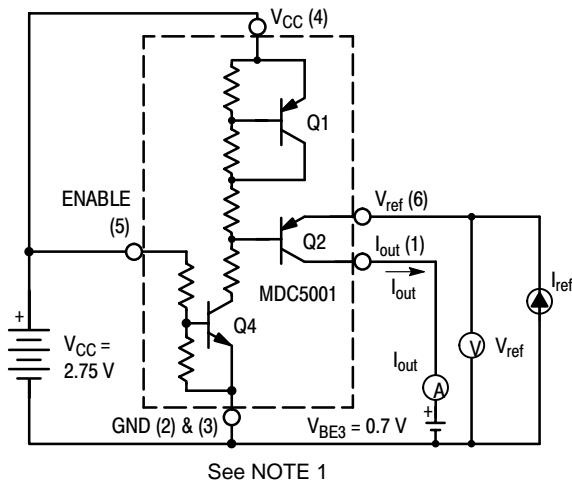


Figure 12. V_{ref} versus T_J Test Circuit

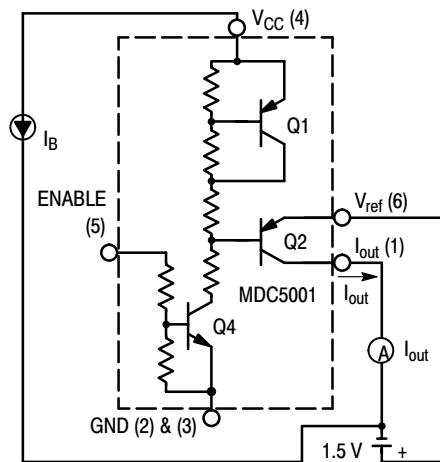


Figure 13. H_{FE} versus I_{out} Test Circuit

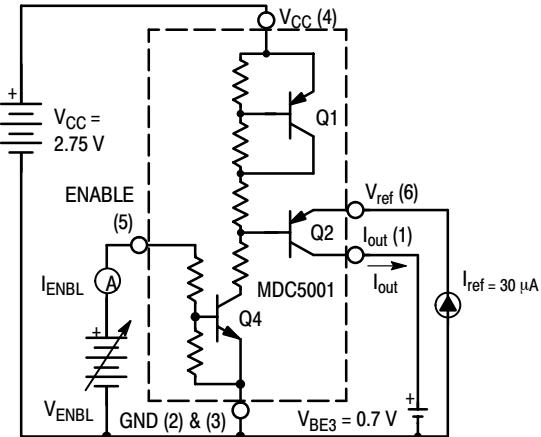


Figure 14. I_{ENBL} versus V_{ENBL} Test Circuit

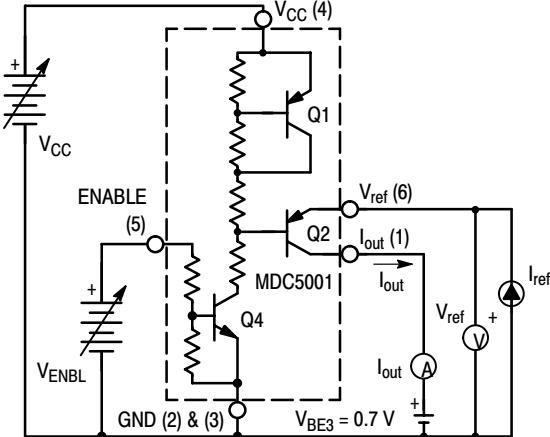


Figure 15. V_{ref} versus V_{ENBL} Test Circuit

NOTE 1: V_{BE3} is used to simulate actual operating conditions that reduce V_{CE2} & H_{FE2} , and increase I_{B2} & V_{ref} .

CLOSED LOOP TEST CIRCUITS

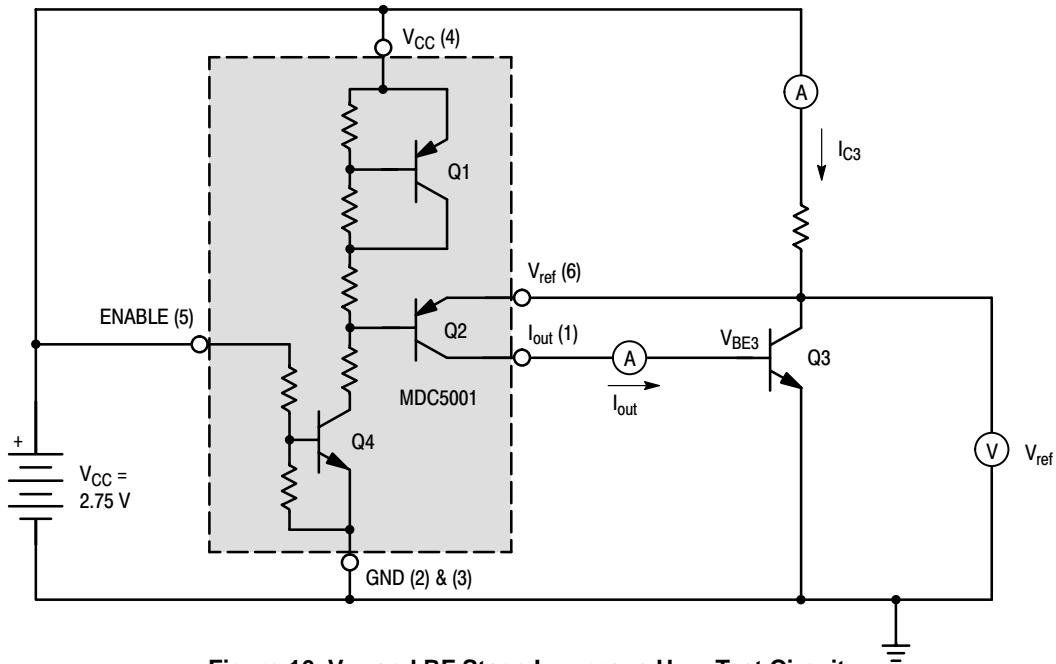


Figure 16. V_{ref} and RF Stage I_{C3} versus H_{FE3} Test Circuit

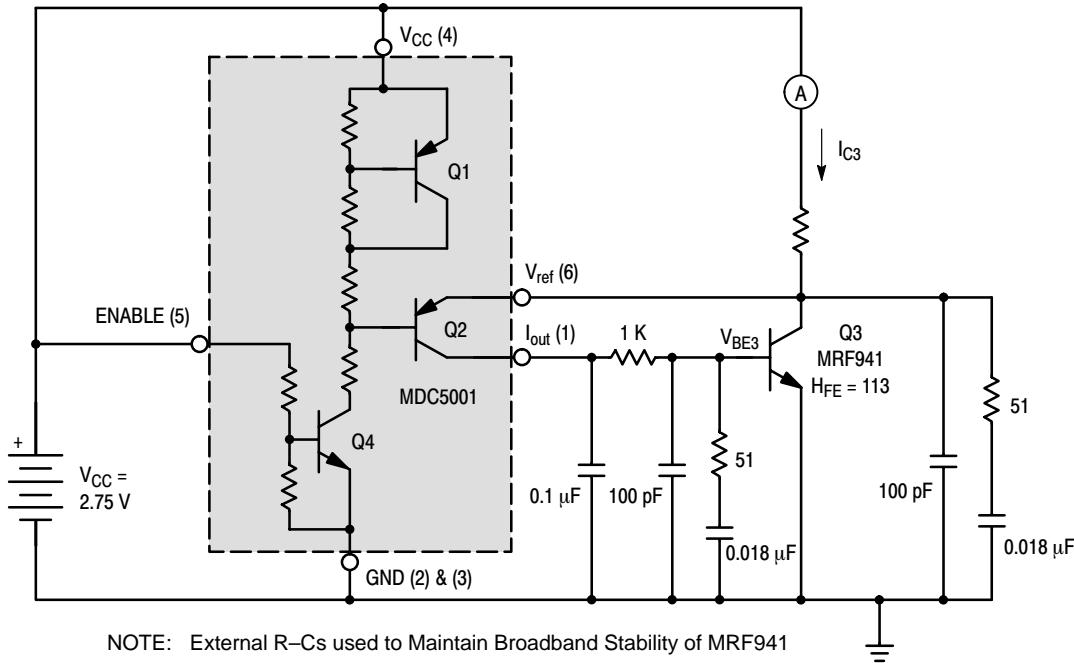
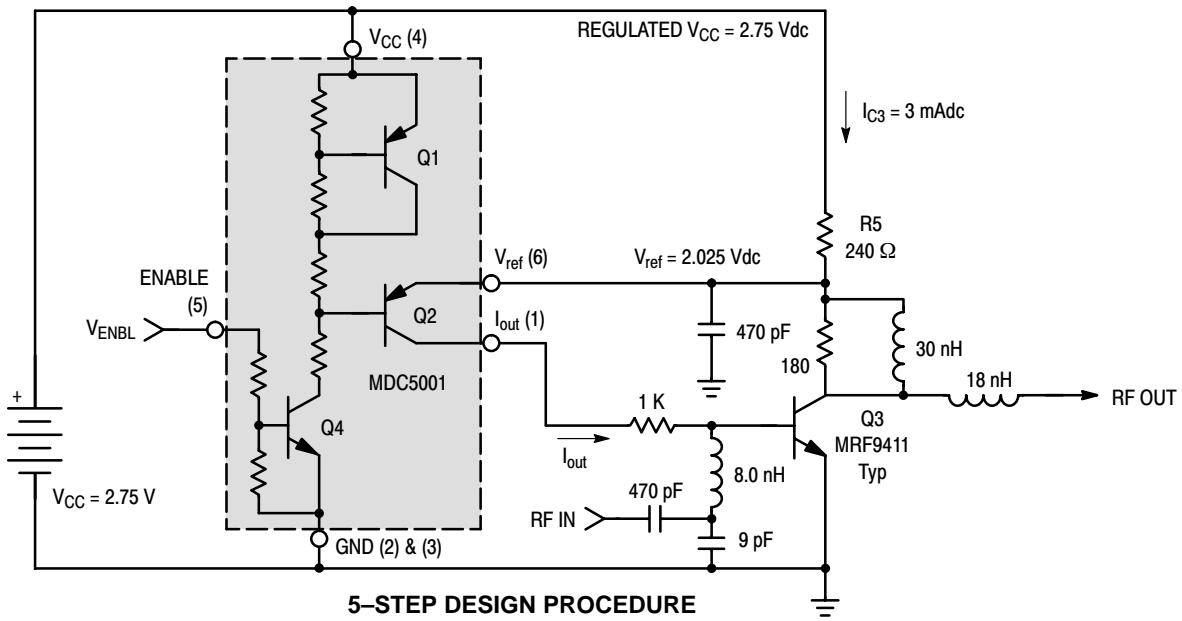


Figure 17. RF Stage I_{C3} versus T_A Test Circuit

APPLICATION CIRCUITS

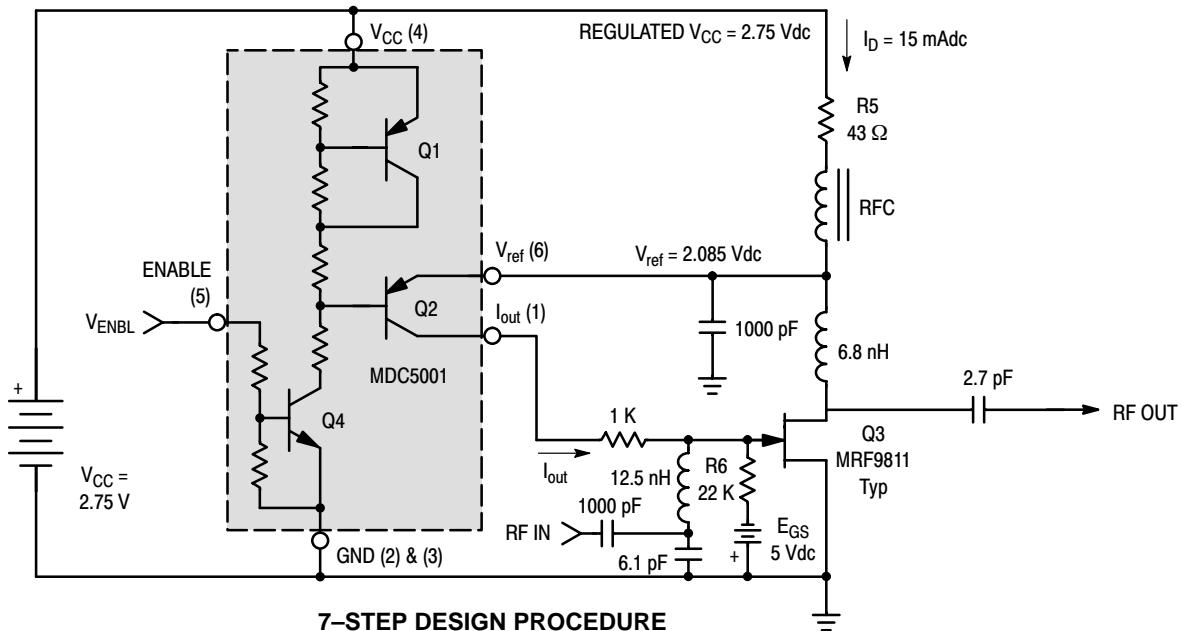


5-STEP DESIGN PROCEDURE

- Step 1: Choose V_{CC} (1.8 V Min to 10 V Max)
- Step 2: Insure that Min V_{ENBL} is \geq minimum indicated in Figures 5 and 6.
- Step 3: Choose bias current, I_{C3} , and calculate needed I_{out} from typ H_{FE3}
- Step 4: From Figure 1, read V_{ref} for V_{CC} and I_{out} calculated.
- Step 5: Calculate Nominal $R5 = (V_{CC} - V_{ref}) \div (I_{C3} + I_{out})$. Tweak as desired.

Figure 18. Class A Biasing of a Typical 900 MHz BJT Amplifier Application

MDC5001T1



7-STEP DESIGN PROCEDURE

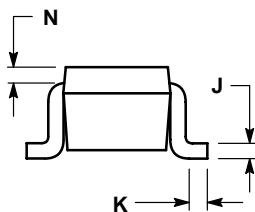
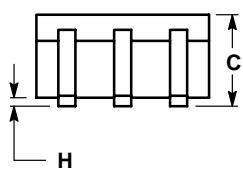
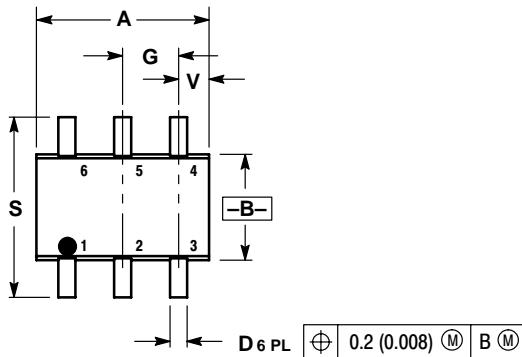
- Step 1: Choose V_{CC} (1.8 V Min to 10 V Max)
- Step 2: Insure that Min V_{ENBL} is \geq minimum indicated in Figures 5 and 6.
- Step 3: Choose bias current, I_D , and determine needed gate-source voltage, V_{GS} .
- Step 4: Choose I_{out} keeping in mind that too large an I_{out} can impair MDC5000 $\Delta V_{ref}/\Delta T_J$ performance (Figure 2) but too large an $R6$ can cause I_{DGO} & I_{GSO} to bias on the FET.
- Step 5: Calculate $R6 = (V_{GS} + E_{GS}) \div I_{out}$
- Step 6: From Figure 1, read V_{ref} for V_{CC} & I_{out} chosen
- Step 7: Calculate Nominal $R5 = (V_{CC} - V_{ref}) \div (I_D + I_{out})$. Tweak as desired.

Figure 19. Class A Biasing of a Typical 890 MHz Depletion Mode GaAs FET Amplifier

MDC5001T1

PACKAGE DIMENSIONS

SC-88 (SOT-363) CASE 419B-01 ISSUE G

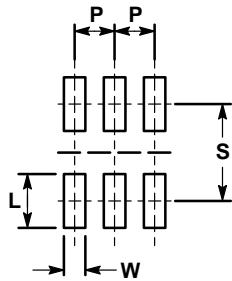


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20
V	0.012	0.016	0.30	0.40

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

PACKAGE DIMENSIONS



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
L	0.035		0.9	
P	0.026 BSC		0.65 BSC	
S	0.063 NOM		1.6 NOM	
W	0.014 NOM		0.34 NOM	

STYLE 19:
 PIN 1. I OUT
 2. GND
 3. GND
 4. V CC
 5. V EN
 6. V REF

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