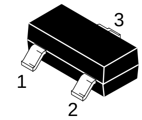
Integrated Relay/ Inductive Load Driver

MDC3105LT1

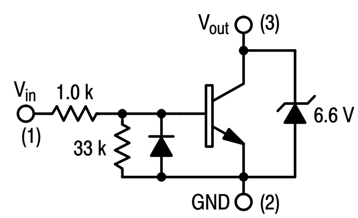
RELAY/INDUCTIVE LOAD DRIVER SILICON SMALLBLOCK™ INTEGRATED CIRCUIT

- Provides a Robust Driver Interface between D.C. Relay Coil and Sensitive Logic Circuits
- Optimized to Switch Relays from a 3 V to 5 V Rail
- Capable of Driving Relay Coils Rated up to 2.5 W at 5 V
- Features Low Input Drive Current & Good Back–to–Front Transient Isolation
- Internal Zener Eliminates Need for Free–Wheeling Diode
- Internal Zener Clamp Routes Induced Current to Ground for Quieter System Operation
- Guaranteed Off State with No Input Connection
- Supports Large Systems with Minimal Off–State Leakage
- ESD Resistant in Accordance with the 2000 V Human Body Model
- Low Sat Voltage Reduces System Current Drain by Allowing Use of Higher Resistance Relay Coils



CASE 318–08, STYLE 6
SOT–23 (TO–236AB)

INTERNAL CIRCUIT DIAGRAM



Applications Include:

- **Telecom:** Line Cards, Modems, Answering Machines, FAX Machines, Feature Phone Electronic Hook Switch
- **Computer & Office:** Photocopiers, Printers, Desktop Computers
- **Consumer:** TVs & VCRs, Stereo Receivers, CD Players, Cassette Recorders, TV Set Top Boxes
- **Industrial:** Small Appliances, White Goods, Security Systems, Automated Test Equipment, Garage Door Openers
- **Automotive:** 5.0 V Driven Relays, Motor Controls, Power Latches, Lamp Drivers

This device is intended to replace an array of three to six discrete components with an integrated SMT part. It is available in a SOT–23 package. It can be used to switch 3 to 6 Vdc inductive loads such as relays, solenoids, incandescent lamps, and small DC motors without the need of a free–wheeling diode.

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	6.0	Vdc
Input Voltage	$V_{in(fwd)}$	6.0	Vdc
Reverse Input Voltage	$V_{in(rev)}$	–0.5	Vdc
Repetitive Pulse Zener Energy Limit (Duty Cycle ≤ 0.01%)	Ezpk	50	mJ
Output Sink Current — Continuous	I_O	500	mA
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

March, 2001 – Rev. 2
Publication Order Number:
MDC3105LT1/D

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Total Device Power Dissipation[1] Derate above 25°C	P_D	225 1.8	mW mW/°C
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	556	°C/W

1. FR–5 PCB of 1″ x 0.75″ x 0.062″, T_A = 25°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Output Zener Breakdown Voltage	$V_{(BRout)}$	6.2	6.6	7.0	V
(@ IT = 10 mA Pulse)	$V_{(–BRout)}$	—	–0.7	—	V
Output Leakage Current @ 0 Input Voltage (V_O = 5.5 Vdc, V_{in} = O.C., T_A = 25°C) (V_O = 5.5 Vdc, V_{in} = O.C., T_A = 85°C)	I_{OO}	 — —	 — —	 5.0 30	μA
Guaranteed “OFF” State Input Voltage (I_O ≤ 100 μA)	$V_{in(off)}$	—	—	0.4	V
ON CHARACTERISTICS					
Input Bias Current (H_{FE} Limited) (I_O = 250 mA, V_O = 0.25 Vdc, T_A = –40°C)	I_{in}	 —	 1.5	 2.5	mAdc
Output Saturation Voltage (I_O = 250 mA, I_{in} = 1.5 mA, T_A = –40°C)	$V_{O(sat)}$	 —	 0.25	 0.4	Vdc
Output Sink Current — Continuous (T_A = –40°C, V_{CE} = 0.25 Vdc, I_{in} = 1.5 mA)	$I_{O(on)}$	 200	 250	 —	mA

TYPICAL APPLICATION–DEPENDENT SWITCHING PERFORMANCE

SWITCHING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units
Propagation Delay Times:					nS
High to Low Propagation Delay; Figure 1 (5.0 V 74HC04)	t_{PHL}	—	55	—	
Low to High Propagation Delay; Figure 1 (5.0 V 74HC04)	t_{PLH}	—	430	—	
High to Low Propagation Delay; Figures 1, 13 (3.0 V 74HC04)	t_{PHL}	—	85	—	
Low to High Propagation Delay; Figures 1, 13 (3.0 V 74HC04)	t_{PLH}	—	315	—	
High to Low Propagation Delay; Figures 1, 14 (5.0 V 74LS04)	t_{PHL}	—	55	—	
Low to High Propagation Delay; Figures 1, 14 (5.0 V 74LS04)	t_{PLH}	—	2.4	—	µS
Transition Times:					nS
Fall Time; Figure 1 (5.0 V 74HC04)	t_f	—	45	—	
Rise Time; Figure 1 (5.0 V 74HC04)	t_r	—	160	—	
Fall Time; Figures 1, 13 (3.0 V 74HC04)	t_f	—	70	—	
Rise Time; Figures 1, 13 (3.0 V 74HC04)	t_r	—	195	—	
Fall Time; Figures 1, 14 (5.0 V 74LS04)	t_f	—	45	—	
Rise Time; Figures 1, 14 (5.0 V 74LS04)	t_r	—	2.4	—	µS

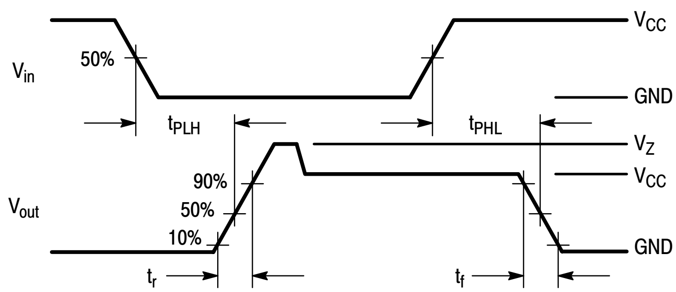


Figure 1. Switching Waveforms

TYPICAL PERFORMANCE CHARACTERISTICS

(ON CHARACTERISTICS)

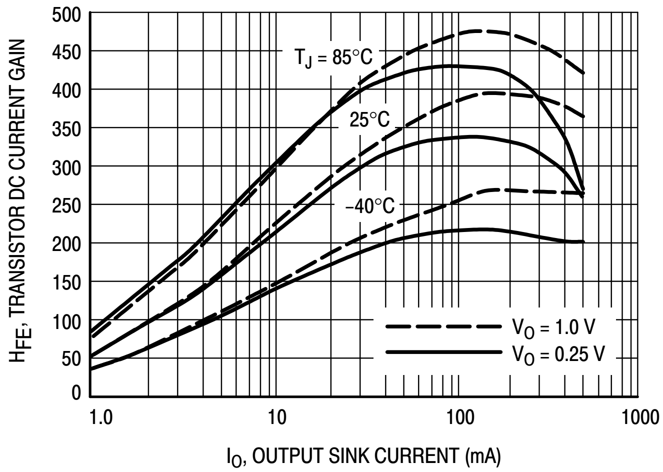


Figure 2. Transistor DC Current Gain

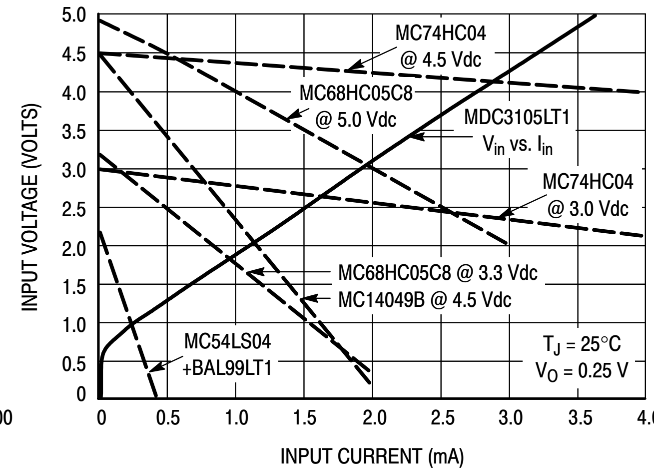


Figure 3. Input V–I Requirement Compared to Possible Source Logic Outputs

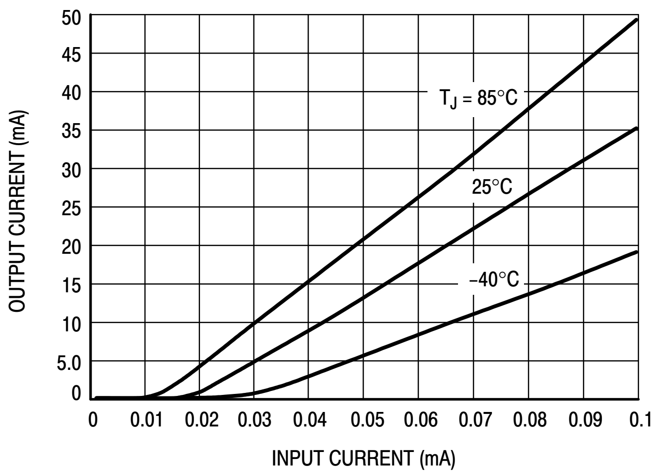


Figure 4. Threshold Effects

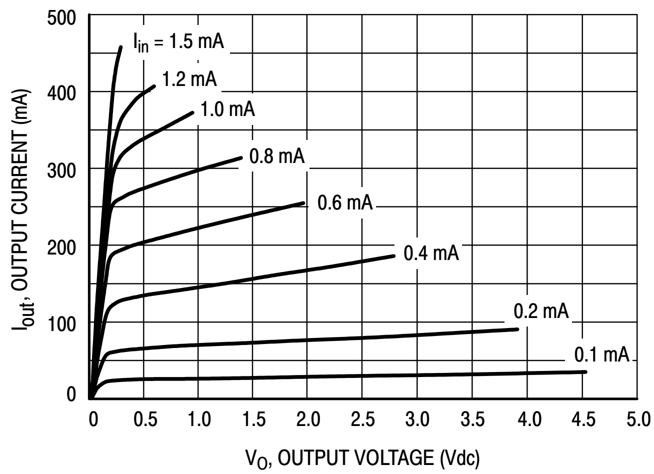


Figure 5. Transistor Output V–I Characteristic

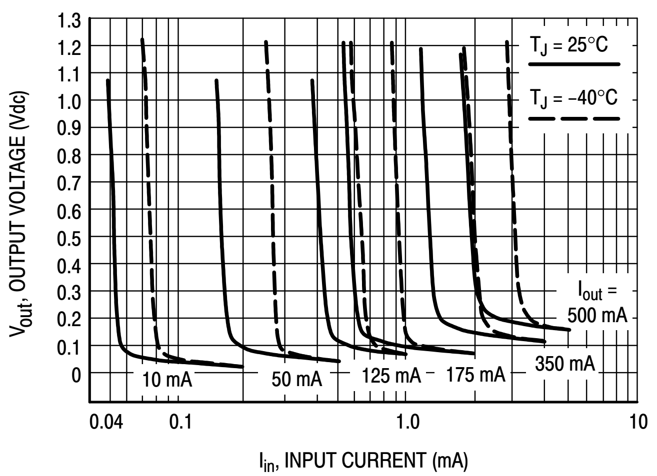


Figure 6. Output Saturation Voltage versus I_{out}/I_{in}

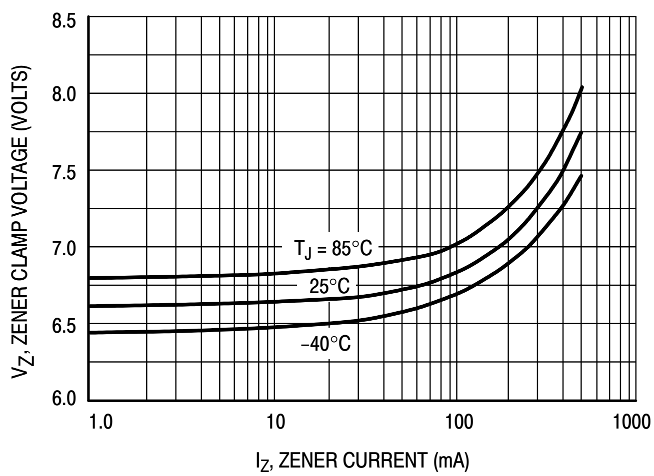


Figure 7. Zener Clamp Voltage versus Zener Current

TYPICAL PERFORMANCE CHARACTERISTICS

(OFF CHARACTERISTICS)

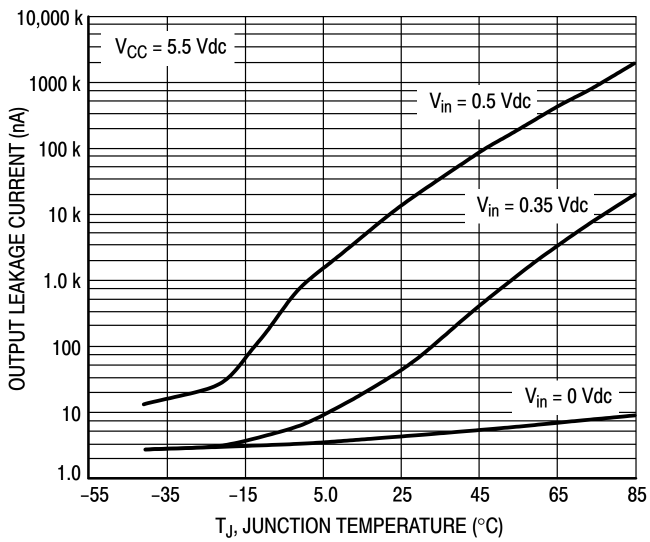


Figure 8. Output Leakage Current versus Temperature

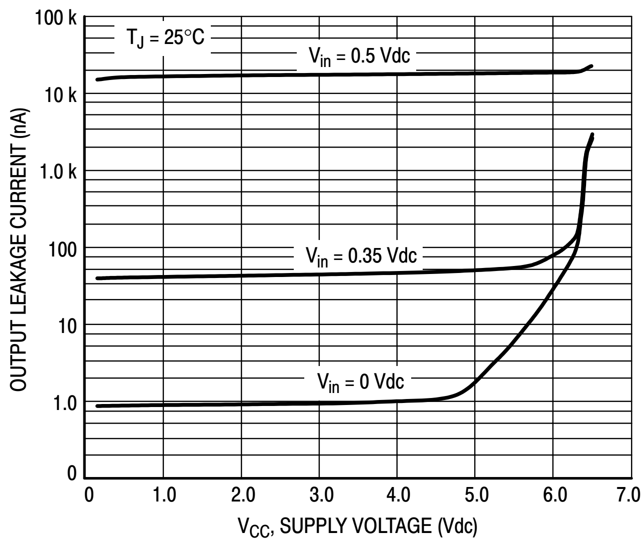


Figure 9. Output Leakage Current versus Supply Voltage

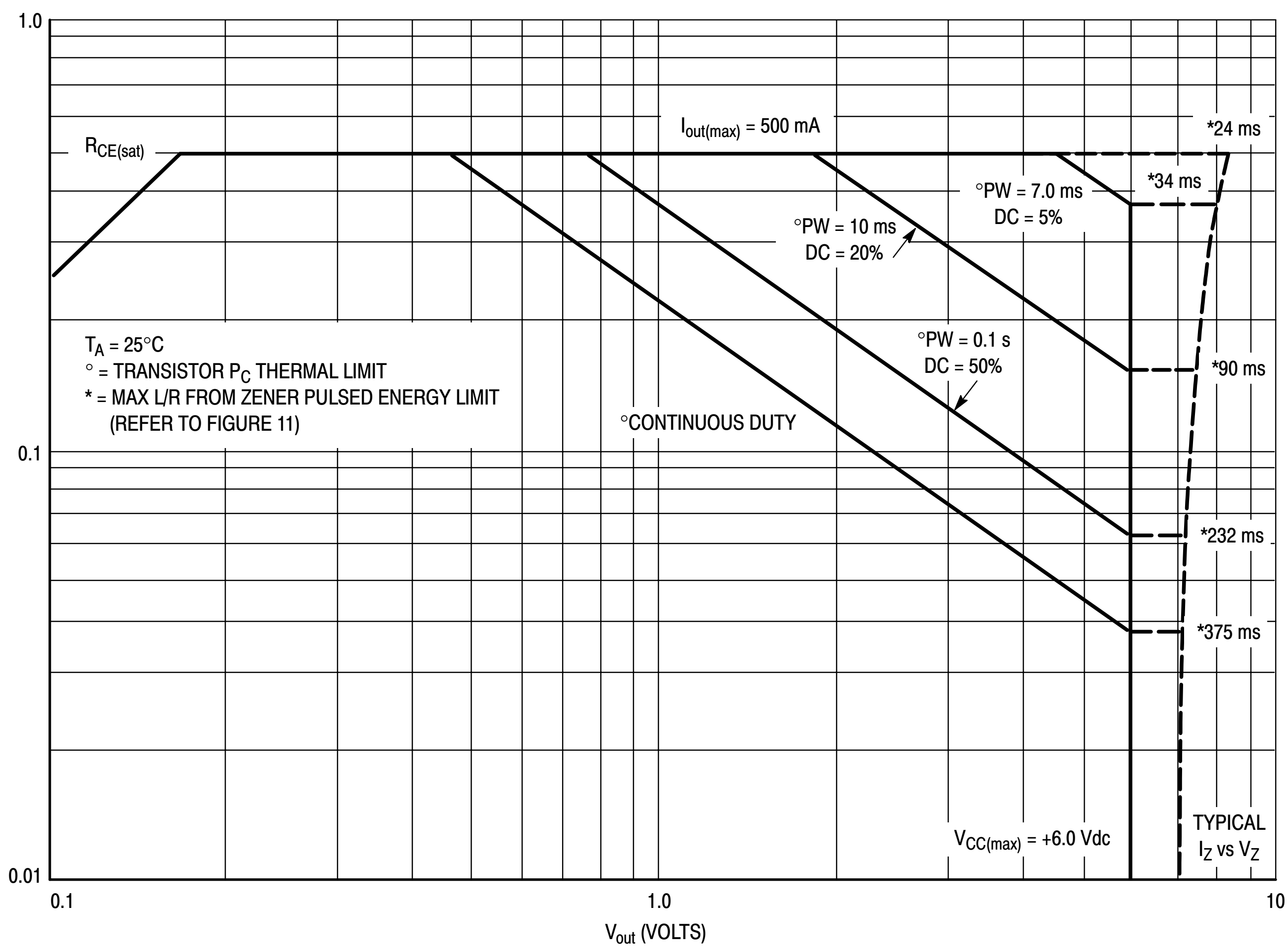


Figure 10. Safe Operating Area

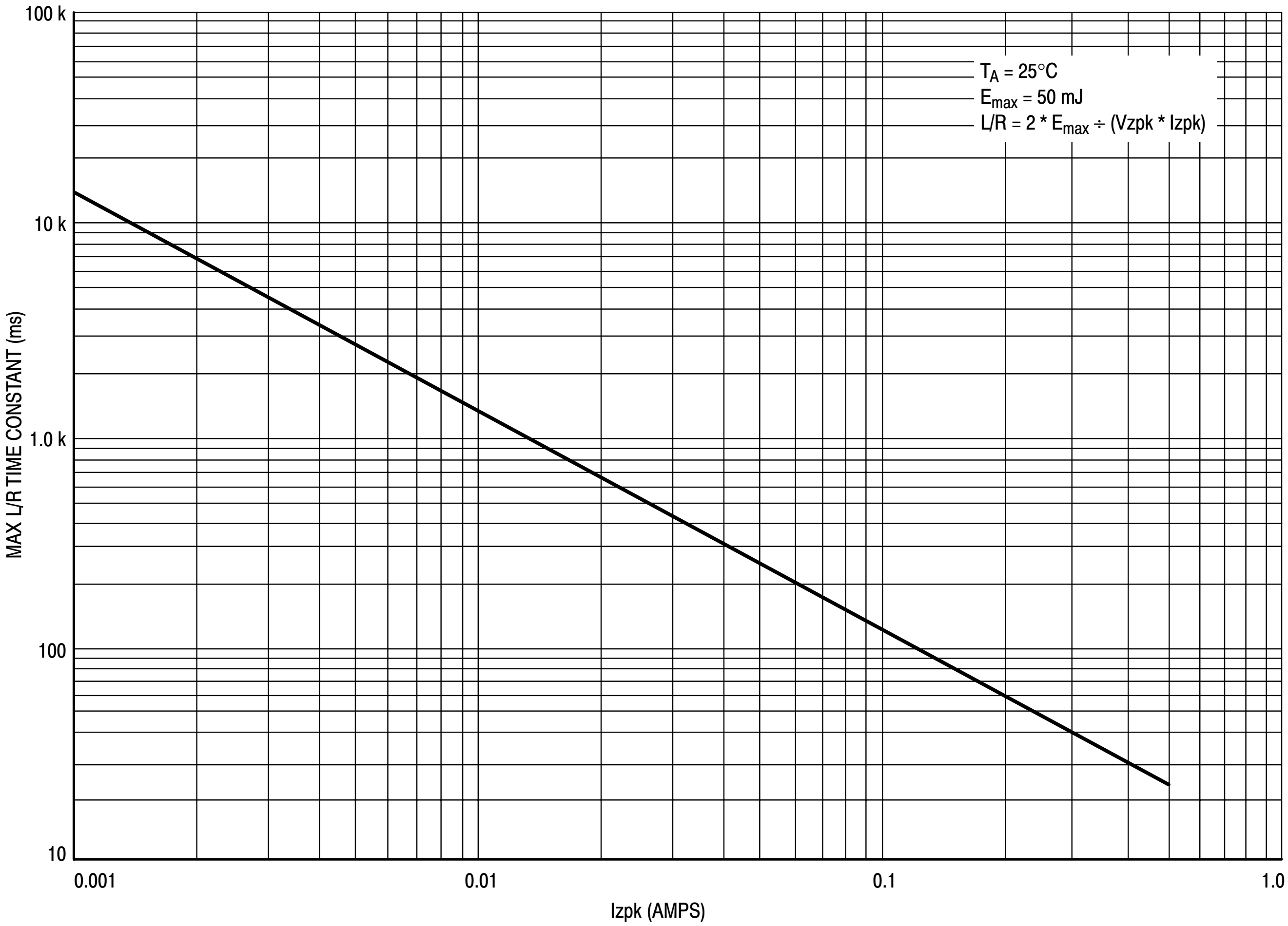


Figure 11. Zener Repetitive Pulse Energy Limit on L/R Time Constant

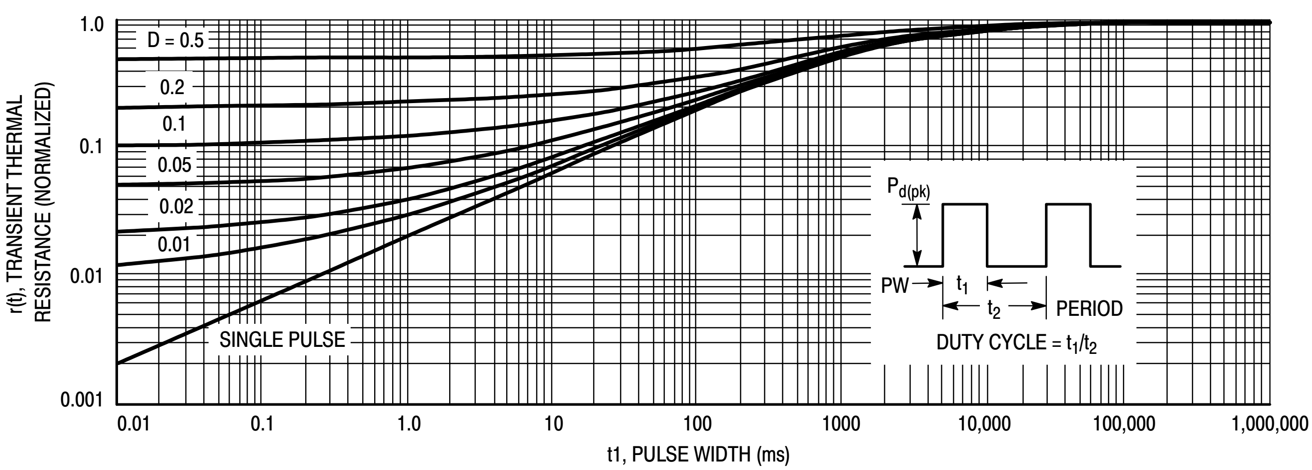


Figure 12. Transient Thermal Response

Using TTR Designing for Pulsed Operation

For a repetitive pulse operating condition, time averaging allows one to increase a device’s peak power dissipation rating above the average rating by dividing by the duty cycle of the repetitive pulse train. Thus, a continuous rating of 200 mW of dissipation is increased to 1.0 W peak for a 20% duty cycle pulse train. However, this only holds true for pulse widths which are short compared to the thermal time constant of the semiconductor device to which they are applied.

For pulse widths which are significant compared to the thermal time constant of the device, the peak operating condition begins to look more like a continuous duty operating condition over the time duration of the pulse. In these cases, the peak power dissipation rating cannot be merely time averaged by dividing the continuous power rating by the duty cycle of the pulse train. Instead, the average power rating can only be scaled up a reduced amount in accordance with the device’s transient thermal response, so that the device’s max junction temperature is not exceeded.

Figure 12 of the MDC3105LT1 data sheet plots its transient thermal resistance, r(t) as a function of pulse width in ms for various pulse train duty cycles as well as for a single pulse and illustrates this effect. For short pulse widths near the left side of the chart, r(t), the factor, by which the continuous duty thermal resistance is multiplied to determine how much the peak power rating can be increased above the average power rating, approaches the duty cycle of the pulse train, which is the expected value. However, as the pulse width is increased, that factor eventually approaches 1.0 for all duty cycles indicating that the pulse width is sufficiently long to appear as a continuous duty condition to this device. For the MDC3105LT1, this pulse width is about 100 seconds. At this and larger pulse widths, the peak power dissipation capability is the same as the continuous duty power capability.

To use Figure 12 to determine the peak power rating for a specific application, enter the chart with the worst case pulse condition, that is the max pulse width and max duty cycle and determine the worst case r(t) for your application. Then calculate the peak power dissipation allowed by using the equation,

$$Pd(pk) = (T_{Jmax} – T_{Amax}) \div (R_{\theta JA} * r(t))$$

$$Pd(pk) = (150°C – T_{Amax}) \div (556°C/W * r(t))$$

Thus for a 20% duty cycle and a PW = 40 ms, Figure 12 yields r(t) = 0.3 and when entered in the above equation, the max allowable Pd(pk) = 390 mW for a max T_A = 85°C.

Also note that these calculations assume a rectangular pulse shape for which the rise and fall times are insignificant compared to the pulse width. If this is not the case in a specific application, then the V_O and I_O waveforms should be multiplied together and the resulting power waveform integrated to find the total dissipation across the device. This then would be the number that has to be less than or equal to the Pd(pk) calculated above. A circuit simulator having a waveform calculator may prove very useful for this purpose.

Notes on SOA and Time Constant Limitations

Figure 10 is the Safe Operating Area (SOA) for the MDC3105LT1. Device instantaneous operation should never be pushed beyond these limits. It shows the SOA for the Transistor “ON” condition as well as the SOA for the zener during the turn–off transient. The max current is limited by the Izpk capability of the zener as well as the transistor in addition to the max input current through the resistor. It should not be exceeded at any temperature. The BJT power dissipation limits are shown for various pulse widths and duty cycles at an ambient temperature of 25°C. The voltage limit is the max V_{CC} that can be applied to the device. When the input to the device is switched off, the BJT “ON” current is instantaneously dumped into the zener diode where it begins its exponential decay. The zener clamp voltage is a function of that BJT current level as can be seen by the bowing of the V_Z versus I_Z curve at the higher currents. In addition to the zener’s current limit impacting this device’s 500 mA max rating, the clamping diode also has a peak energy limit as well. This energy limit was measured using a rectangular pulse and then translated to an exponential equivalent using the 2:1 relationship between the L/R time constant of an exponential pulse and the pulse width of a rectangular pulse having equal energy content. These L/R time constant limits in ms appear along the V_Z versus I_Z curve for the various values of I_Z at which the Pd lines intersect the V_{CC} limit. The L/R time constant for a given load should not exceed these limits at their respective currents. Precise L/R limits on zener energy at intermediate current levels can be obtained from Figure 11.

Designing with this Data Sheet

1. Determine the maximum inductive load current (at max V_{CC}, min coil resistance & usually minimum temperature) that the MDC3105 will have to drive and make sure it is less than the max rated current.
2. For pulsed operation, use the Transient Thermal Response of Figure 12 and the instructions with it to determine the maximum limit on transistor power dissipation for the desired duty cycle and temperature range.
3. Use Figures 10 & 11 with the SOA notes above to insure that instantaneous operation does not push the device beyond the limits of the SOA plot.
4. While keeping any $V_{O(sat)}$ requirements in mind, determine the max input current needed to achieve that output current from Figures 2 & 6.
5. For levels of input current below 100 μA, use the input threshold curves of Figure 4 to verify that there will be adequate input current available to turn on the MDC3105 at all temperatures.
6. For levels of input current above 100 μA, enter Figure 3 using that max input current and determine the input voltage required to drive the MDC3105 from the solid V_{in} versus I_{in} line. Select a suitable drive source family from those whose dotted lines cross the solid input characteristic line to the right of the I_{in}, V_{in} point.
7. Using the max output current calculated in step 1, check Figure 7 to insure that the range of zener clamp voltage over temperature will satisfy all system & EMI requirements.
8. Using Figures 8 & 9, insure that “OFF” state leakage over temperature and voltage extremes does not violate any system requirements.
9. Review circuit operation and insure none of the device max ratings are being exceeded.

APPLICATIONS DIAGRAMS

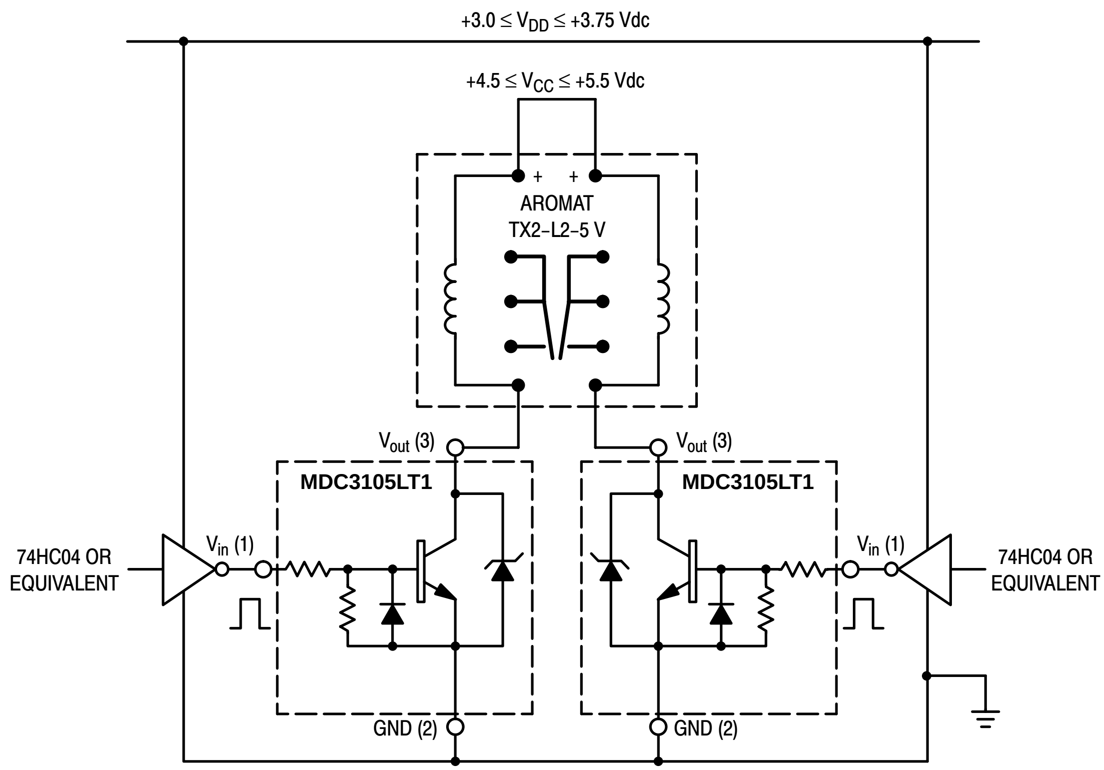


Figure 13. A 200 mW, 5.0 V Dual Coil Latching Relay Application with 3.0 V–HCMOS Level Translating Interface

Max Continuous Current Calculation

for TX2–5V Relay, R1 = 178 Ω Nominal @ R_A = 25°C

Assuming ±10% Make Tolerance,
R1 = 178 Ω * 0.9 = 160 Ω Min @ T_A = 25°C

T_C for Annealed Copper Wire is 0.4%/°C

R1 = 160 Ω * [1+(0.004) * (–40°–25°)] = 118 Ω Min @ –40°C

I_O Max = (5.5 V Max – 0.25V) /118 Ω = 45 mA

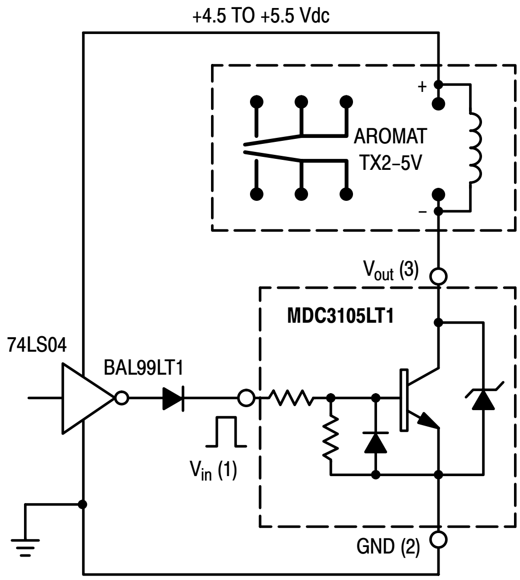


Figure 14. A 140 mW, 5.0 V Relay with TTL Interface

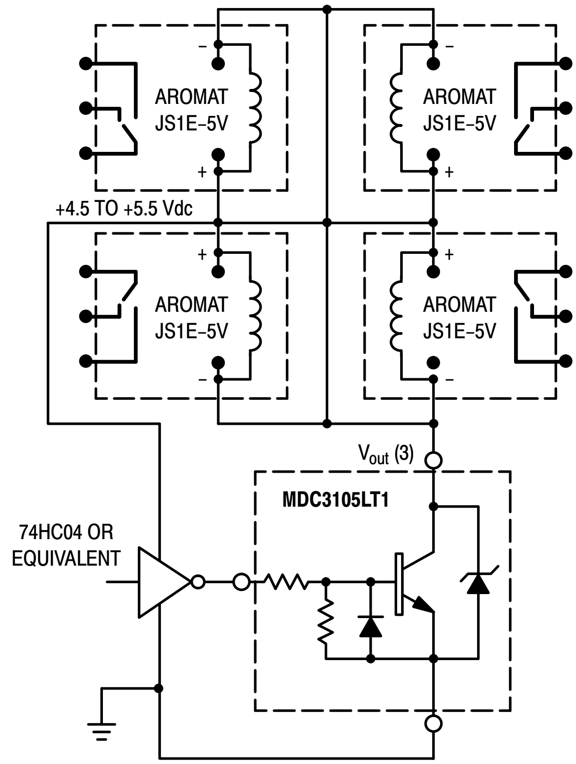


Figure 15. A Quad 5.0 V, 360 mW Coil Relay Bank

TYPICAL OPERATING WAVEFORMS

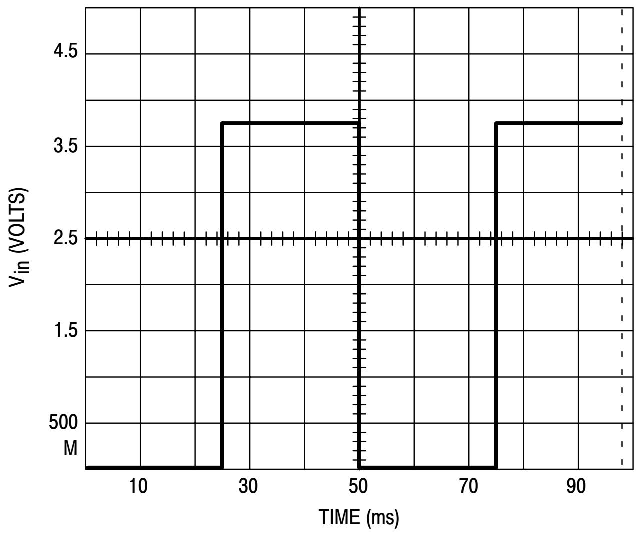


Figure 16. 20 Hz Square Wave Input

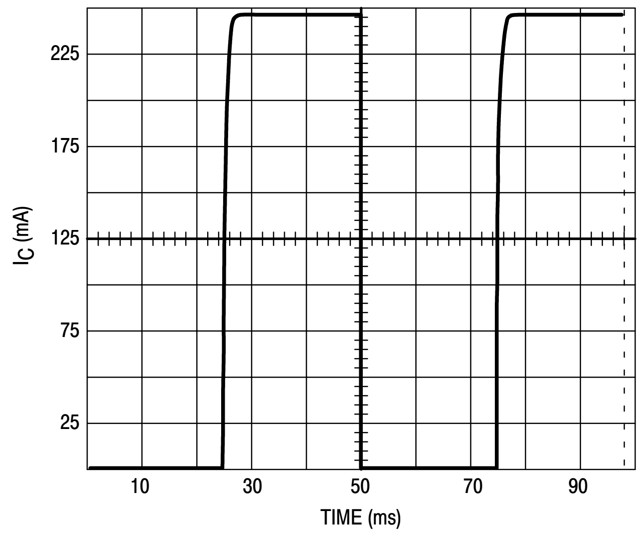


Figure 17. 20 Hz Square Wave Response

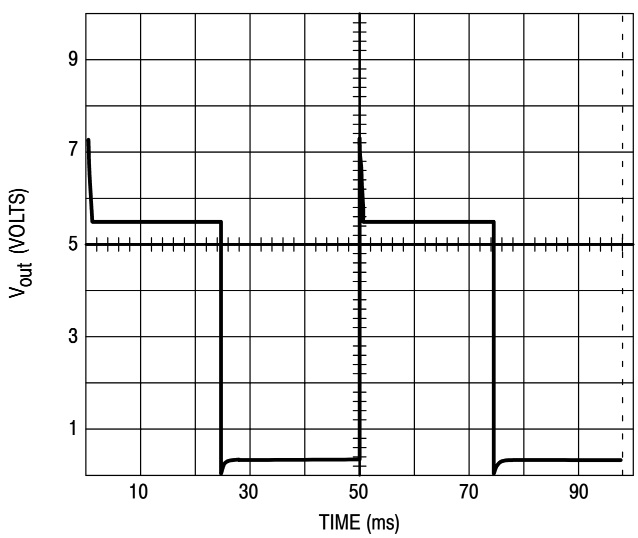


Figure 18. 20 Hz Square Wave Response

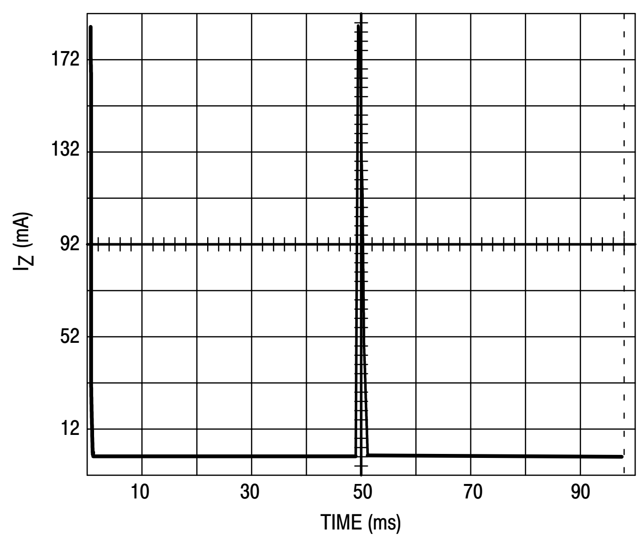
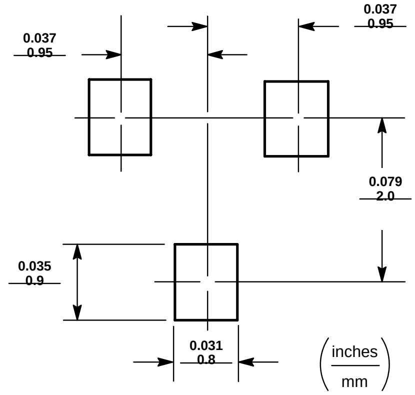


Figure 19. 20 Hz Square Wave Response

INFORMATION FOR USING THE SOT–23 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT–23

SOT–23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the SOT–23 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150°C - 25°C}{556°C/W} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDERING PRECAUTIONS

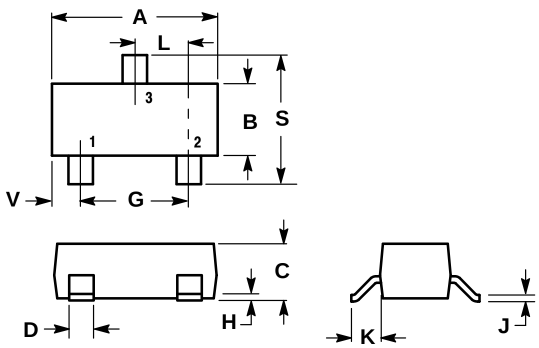
The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.
- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient should be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

PACKAGE DIMENSIONS

SOT–23 (TO–236)
CASE 318–08
ISSUE AF



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

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