- **High performance, low power pipeline burst SRAM**
  - Ultra low power for green PC and battery powered PC
- **High Performance**
  - 133-166MHz Speed grades
  - 3-1-1-1 Burst Read
  - 1-1-1-1 Burst Write
  - 3-1-1-1-1-1-1-1... pipeline operation
- **Low Power**
  - Low active power
  - Ultra low power ZZ standby mode
  - Single 3.3V supply (V_{DD})
  - Isolated 3.3V or 2.5V I/O supply (V_{DDQ})
- **Compatibility**
  - Individual Byte Write and Global Write masking
  - Interleave and burst address support
  - Industry standard 100-Pin PBSRAM pinout
  - Industry standard PBSRAM specification
- **Applications**
  - Processor L2 Cache
  - Ideal for high speed, low power communications buffers
  - Power sensitive portable DSP applications

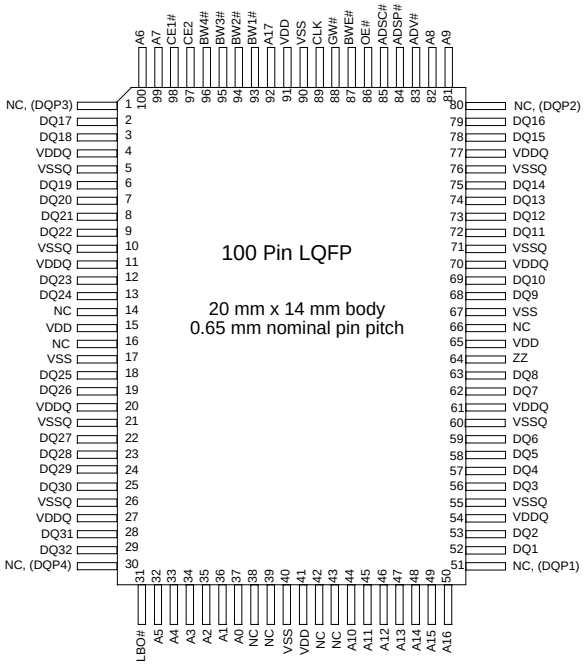


Figure 1. Pin Function

Overview

The MoSys MC803256K is a high performance, low power pipeline-burst-SRAM (PBSRAM). Fabricated using an advanced low power, high performance CMOS process, the MoSys MC803256K is backward pin and function compatible with standard 32Kx32/36, 64Kx32/36 and 128Kx32/36 PBSRAMs with additional operating features like low power ZZ standby mode and linear burst order addressing. These additional operating features are defined so that, with proper implementation, PC boards can work transparently with 32Kx32/36, 64Kx32/36, 128Kx32/36 or 256Kx32/36 configurations, allowing the designer maximum configuration flexibility within a single footprint layout.

The MoSys MC803256K supports PBSRAM operating modes at maximum burst frequency including indefinite pipeline read or write (3-1-1-1-1-1-1...)

Parameter	Symbol	-7R5	-6	Unit
Cycle Time	tKC	7.5	6	ns
Access Time	tKQ	4.5	3.5	ns
Clock to High-Z	tKQHZ	4	3.4	ns

Available in 256Kx32 and 256Kx36 bit densities, the MoSys MC803256K is packaged in a standard 100 lead LQFP.

Lowest Power

The MC803256K affords systems dramatic power savings due to the benefits of its proprietary MoSys technology. Peak operating power of a typical PBSRAM is 5x that of the MC803256K. Making it ideal for portable applications, as well as applications requiring a large amount of RAM.

Part Number Designation

Example*: MC803256K32L-10 I*
Device Designation: *MC8*:, Series: *03*
Organization: *256K32*
Package Type: L=LQFP
Speed: – 7R5 133MHz
– 6 166MHz
Temp: *I* = Industrial Temperature

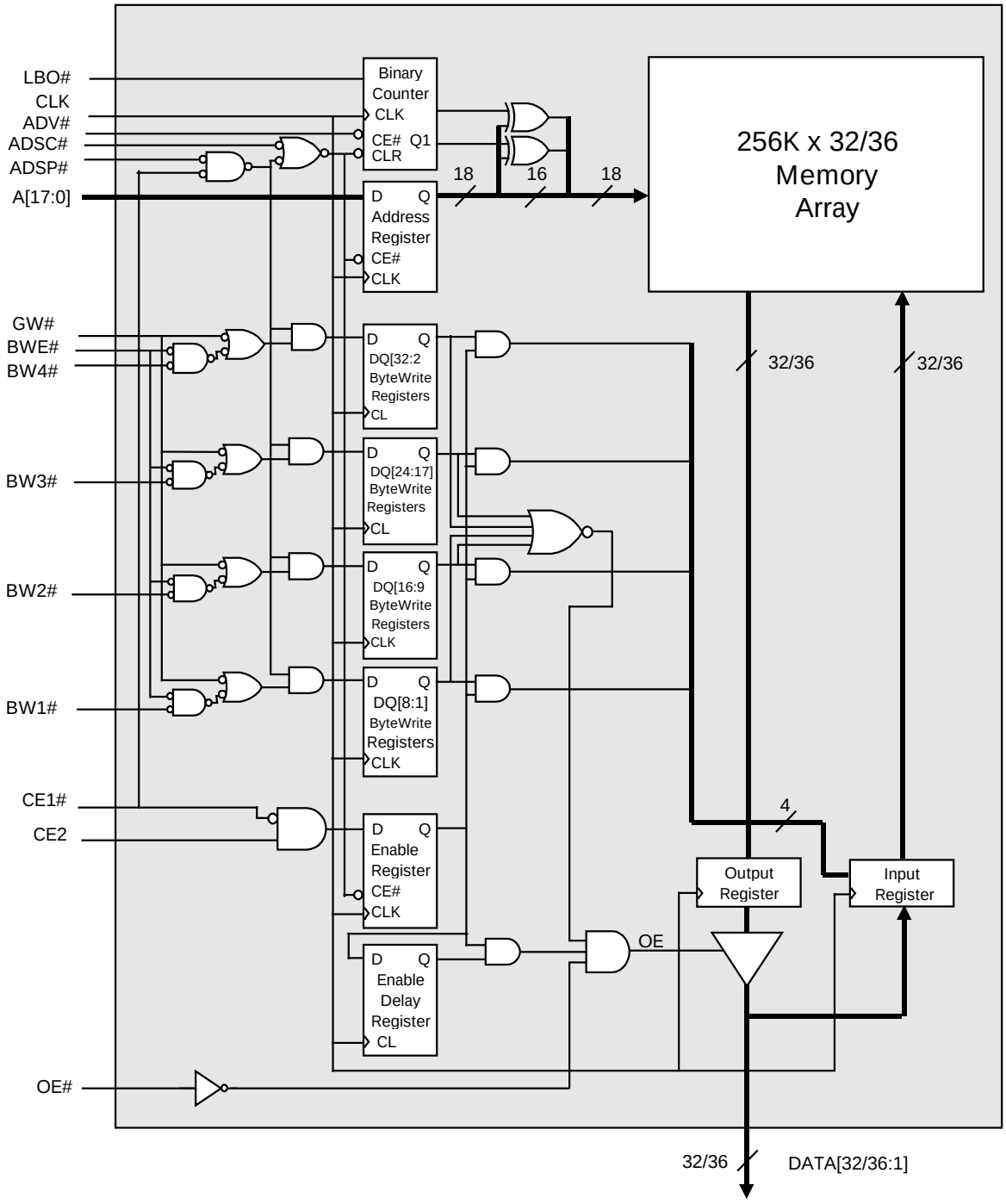


Figure 2 Functional Block Diagram

Table 1. LQFP Pin Description

Pin Number	Symbol	Type	Description
92, 50, 49, 48, 47, 46, 45, 44, 81, 82, 99, 100, 32, 33, 34, 35, 36 ,37	A[17:0]	Input	Processor Addresses
96,95, 94, 93	BW[4:1]#	Input	Processor host bus byte enables.
88	GW#	Input	Global Write from cache controller
87	BWE#	Input	Byte Write Enable from controller
89	CLK	Input	Processor host bus clock
98	CE1#	Input	ADSP# mask and ADSC# chip enable
97	CE2	Input	Depth expansion chip enable
86	OE#	Input	Asynchronous output enable
83	ADV#	Input	Burst address counter advance
84	ADSP#	Input	ADS# of processor
85	ADSC#	Input	ADS# of controller
64	ZZ	Input	Low power sleep mode
31	LBO#	Input	Linear Burst Order
29, 28, 25, 24, 23, 22, 19, 18, 13, 12, 9, 8, 7, 6, 3, 2, 79, 78, 75, 74, 73, 72, 69, 68, 63, 62, 59, 58, 57, 56, 53, 52	DQ[32:1]	I/O	Data I/O pins
30, 1, 80, 51	NC/DQP[4:1]	I/O	Data parity I/O pins
14, 16, 38, 39, 42, 43, 66	NC	-	unused
15, 41, 65, 91	VDD	3.3 Volts	Power
17, 40, 67, 90	VSS	Ground	Ground
4, 11, 20, 27, 54, 61, 70, 77	VDDQ	I/O Sup-ply	I/O Buffer Supply
5, 10, 21, 26, 55, 60, 71, 76	VSSQ	I/O Ground	I/O Buffer Ground

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	Core Supply Voltage		4.0	V
V_{DDQ}	I/O Supply Voltage		$V_{DDQ} \leq V_{DD}$ +0.5, $V_{DDQ} \leq 4.0$	V
V_{ih}	Input High Voltage		V_{DDQ} +0.5	V
V_{il}	Input Low Voltage	V_{SSQ}-0.5		V
Ts	Storage Temperature	-65	150	°C

Notes: Max Vih is not to exceed maximum VDDQ

Table 3. Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Max	Units
V_{DD}	Supply Voltage	3.3V ±5%	3.135	3.465	V
V_{DDQ}	I/O Supply Voltage	2.5V +38%/-5%	2.375	3.465	V
V_{ih}	Input High Voltage		1.8	V_{DDQ} + .3	V
V_{il}	Input Low Voltage		-0.3	0.8	V
V_{oh}	Output High Voltage	I_{oh} = -5 mA	2.4		V
V_{ol}	Output Low Voltage	I_{ol} = 5 mA		0.4	V
T_{AC}	Commercial Operating Temp.		0	70	°C
T_{AI}	Industrial Operating Temp.		-40	85	°C

Table 4. Absolute Maximum AC Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{ih}	Input High Voltage	1.8	V_{DDQ}+1.0	V
V_{il}	Input Low Voltage	V_{SSQ} - 1.0	0.8	V
tOVR	Overshoot/Undershoot Voltage Duration		0.2*tCY	ns
tSET	Overshoot/Undershoot Settling Time		0.8*tCY	ns

Table 5. Maximum DC Current Requirements

Symbol	Condition	Current	Units
I_{DD}	Operating current, device selected; all inputs ≤ Vil or ≥ Vih; cycle time ≥ tKC min, V_{DD}= max, 0 pF load	60	mA
I_{DD1}	Idle current, device selected; ADSP#, ADSC#, GW#, BW#s, ADV# and all other inputs ≥ 2.8 volts; cycle time ≥ tKC min, V_{DD}= max, 0 pF load	10	mA
I_{DDZ}	Sleep mode, clock stopped, all inputs ≥ 2.8 v, V_{DD}= max	2	mA

Table 6. Pin Capacitance

Symbol	Parameter	Max	Units
C_I	Input Pin Capacitance	4	pF
$C_{I/O}$	I/O Pin Capacitance	6	pF

Table 6. AC Timing Characteristics at Recommended Operating Conditions

		-6 (166 MHz)		-7R5 (133 MHz)		
Sym	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
tAAH	ADV# hold	0.5		0.5		ns
tAAS	ADV# setup	1.5		2		ns
tADSH	ADSx# hold	0.5		0.5		ns
tADSS	ADSx# setup	1.5		2		ns
tAH	Address hold	0.5		0.5		ns
tAS	Address setup	1.5		2		ns
tCEH	Chip Enable hold	0.5		0.5		ns
tCES	Chip Enable setup	1.5		2		ns
tDH	Write Data hold	0.5		0.5		ns
tDS	Write Data setup	1.5		2		ns
tKC	Clock cycle	6		7.5		ns
tKH	Clock high	1.5		2		ns
tKL	Clock low	1.5		2		ns
tKQ	Clock to output valid		3.5		4.5	ns
tKQHZ	Clock to output high-Z	1.5	3.4	1.5	4	ns
tKQLZ	Clock to output low-Z	0		0		ns
tKQX	Clock to output invalid	1.5		1.5		ns
tOELZ	OE# to output low-Z	0		0		ns
tOEHZ	OE# to output high-Z		3.8		4.5	ns
tOEQ	OE# to output valid		3.8		4.5	ns
tOEQX	OE# to output invalid	0		0		ns
tWS	GW#, BWx# setup	1.5		2		ns
tWH	GW#, BWx# hold	0.5		0.5		ns
tZZs	ZZ standby		100		100	ns
tZZREC	ZZ recovery	100		100		ns

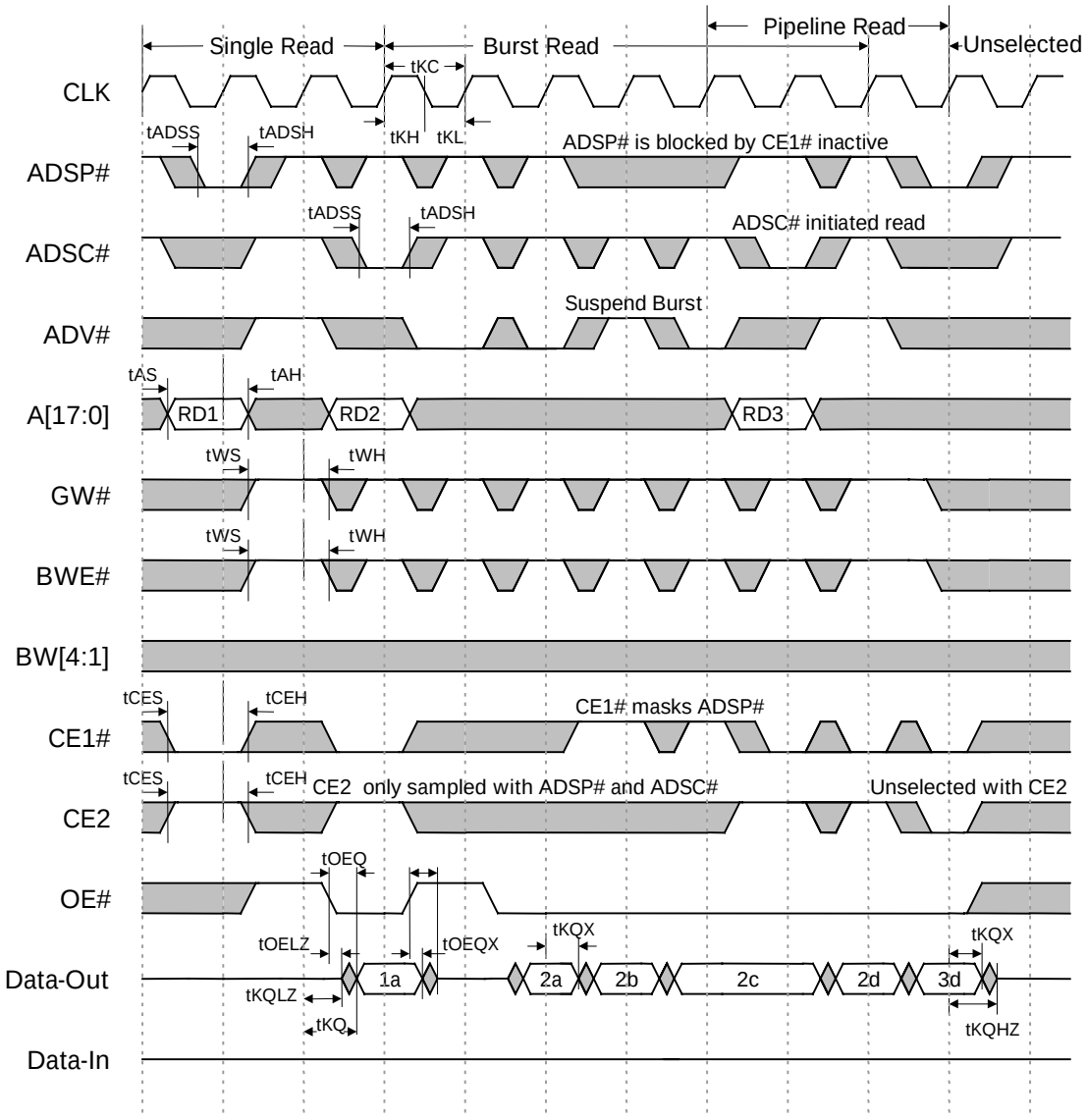


Figure 3 Read Cycle Timing

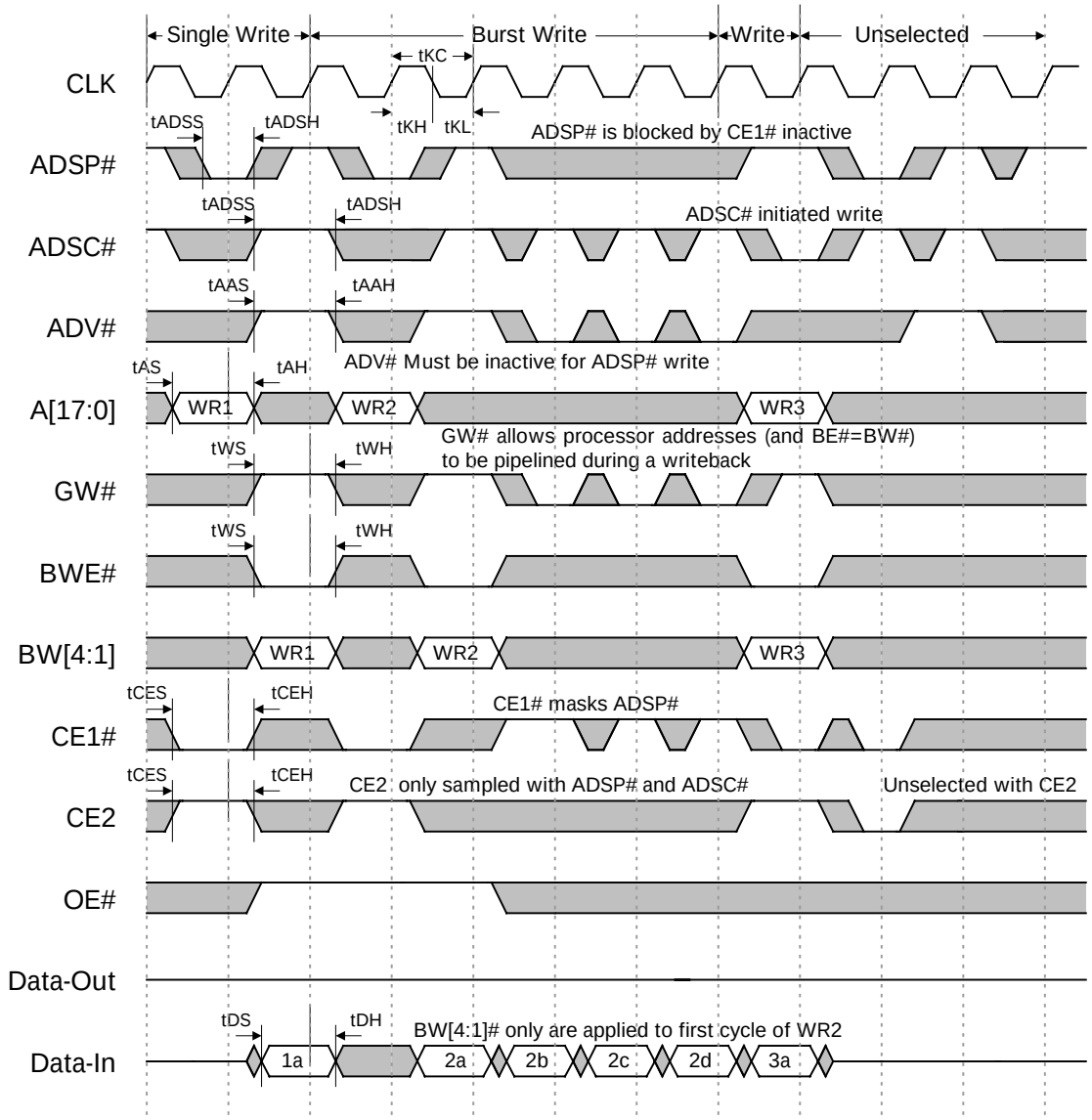


Figure 4 Write Cycle Timing

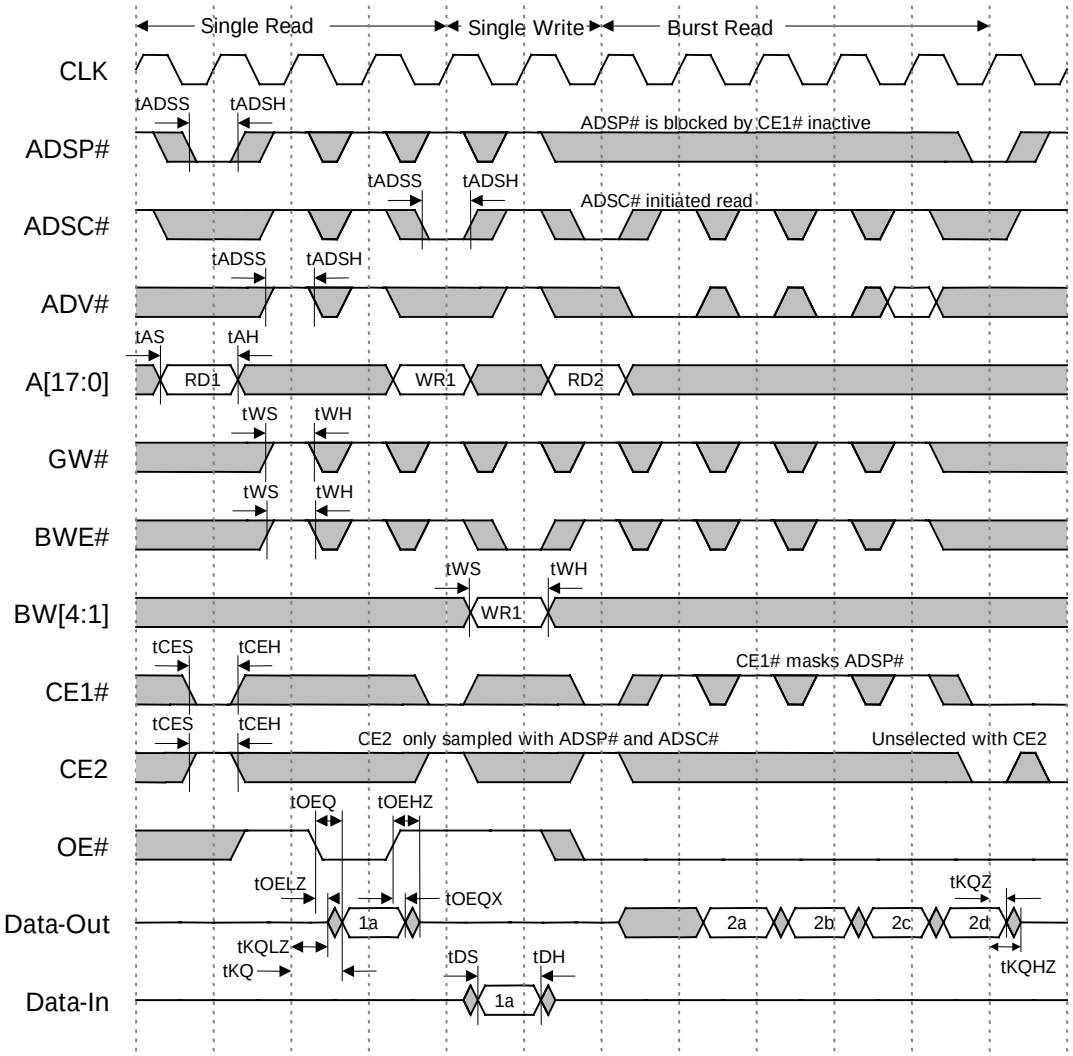


Figure 5 Read/Write Cycle Timing

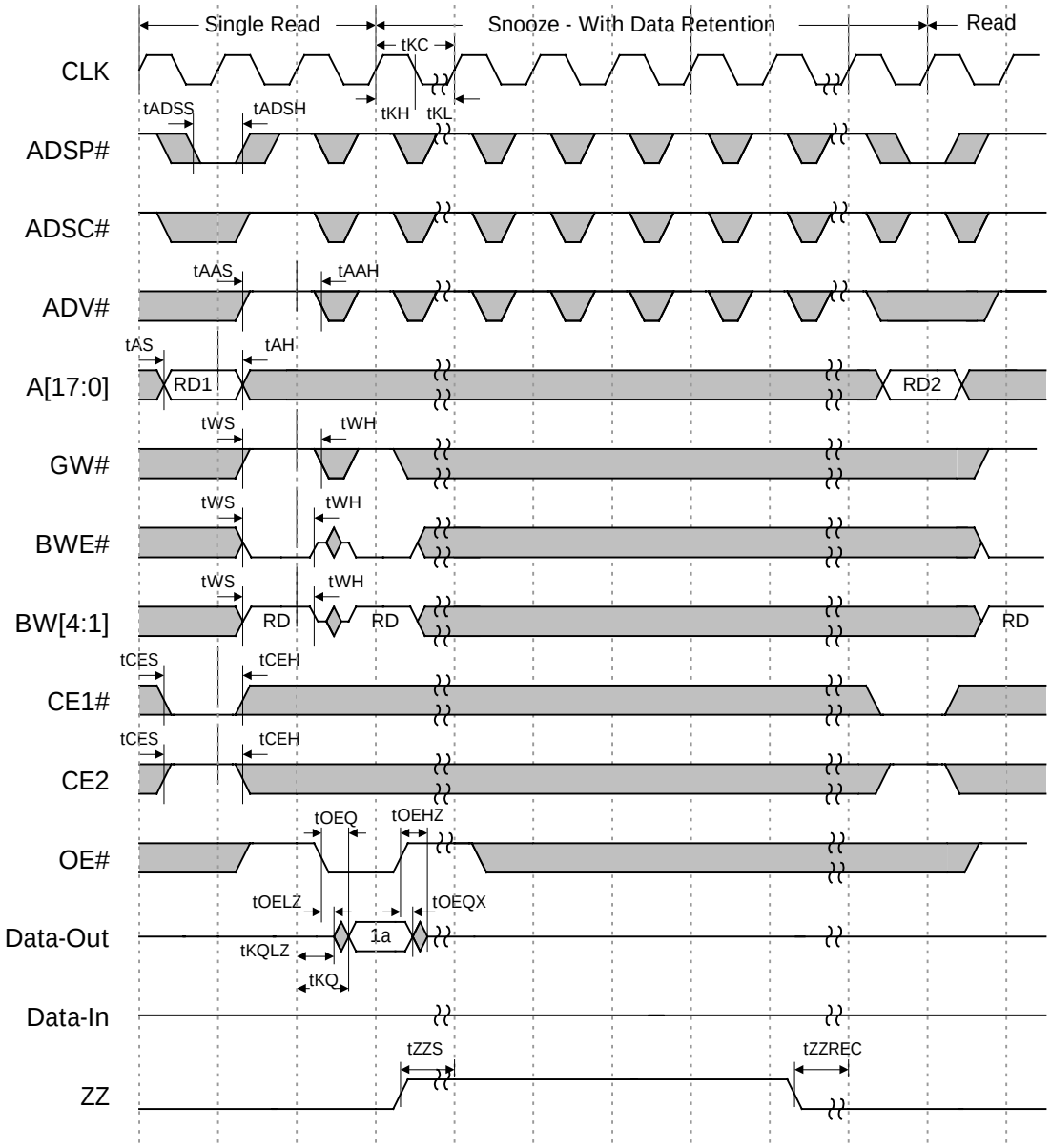
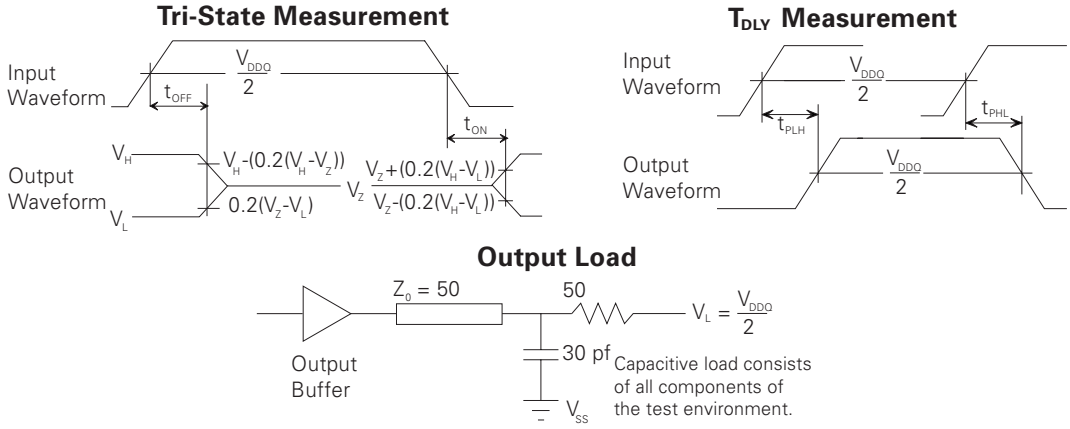


Figure 6 ZZ and RD Timing

Test and Measurement



Test Structure and Measurement Points

Notes

1 Valid Delay Measurement is made from the VDDQ / 2 on the input waveform to the VDDQ / 2 on the output waveform. Input waveform should have a slew rate of 1V/ns.

2 Tri-state t_{off} measurement is made from the VDDQ/2 on the input waveform to the output waveform moving 20% from its initial to final value VDDQ/2.

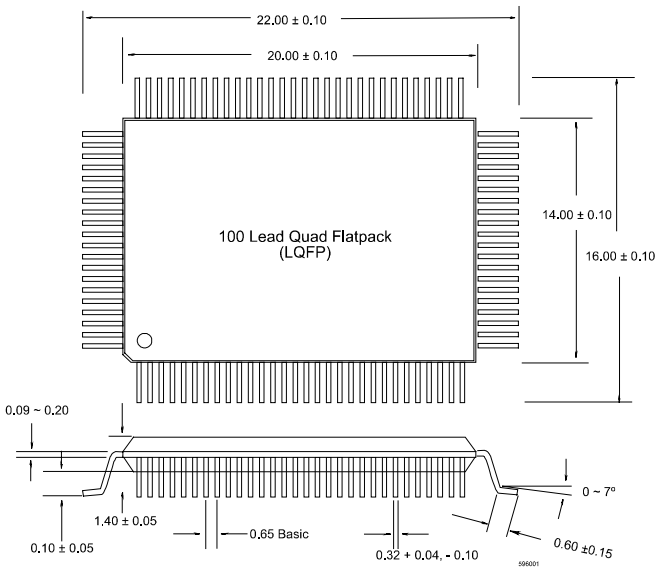


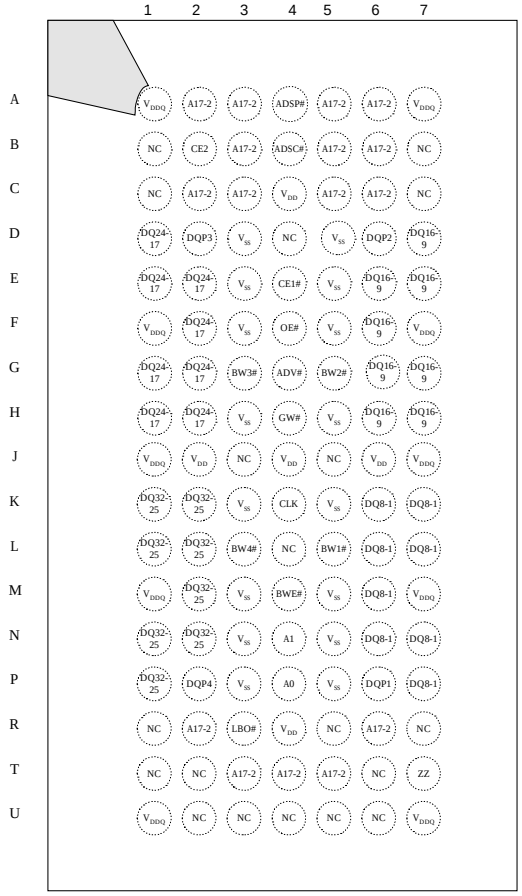
Figure 7. LQFP Mechanical Characteristics

BGA Pin Description

Pin Location	Symbol	Type	Description
2A, 2C, 2R, 3A, 3B, 3C, 3T, 4T, 5A, 5B, 5C, 5T, 6A, 6B, 6C, 6R, 4N, 4P	A[17:0]	Input	Processor Addresses
3L, 3G, 5G, 5L	BW[4:1]#	Input	Processor host bus byte enables.
4H	GW#	Input	Global Write from cache controller
4M	BWE#	Input	Byte Write Enable from controller
4K	CLK	Input	Processor host bus clock
4E	CE1#	Input	ADSP# mask and ADSC# chip enable
2B	CE2	Input	Depth expansion chip enable
4F	OE#	Input	Asynchronous output enable
4G	ADV#	Input	Burst address counter advance
4A	ADSP#	Input	ADS# of processor
4B	ADSC#	Input	ADS# of controller
7T	ZZ	Input	Low power sleep mode
3R	LBO#	Input	Linear Burst Order
1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 1D, 1E, 2E, 2F, 1G, 2G, 1H, 2H, 7D, 6E, 7E, 6F, 6G, 7G, 6H, 7H, 6K, 7K, 6L, 7L, 6M, 6N, 7N, 7P	DQ[32:1]	I/O	Data I/O pins
2P, 2D, 6D, 6P	NC/DQP[4:1]	I/O	Data parity I/O pins
1B, 7B, 1C, 7C, 4D, 3J, 5J, 4L, 1R, 5R 7R, 1T, 2T, 6T, 2U, 3U, 4U, 5U, 6U	NC	-	unused
4C, 2J, 4J, 6J, 4R	VDD	3.3 Volts	Power
3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P	VSS	Ground	Ground
1A, 7A, 1F1 7F, 1J, 7J, 1M, 7M, 1U, 7U	VDDQ	I/O Supply	I/O Buffer Supply

BGA Pin Location (Top View)

	1	2	3	4	5	6	7
A	V_{DDQ}	A17-2	A17-2	ADSP#	A17-2	A17-2	V_{DDQ}
B	NC	CE2	A17-2	ADSC#	A17-2	A17-2	NC
C	NC	A17-2	A17-2	V_{DD}	A17-2	A17-2	NC
D	DQ24-17	DQP3	V_{SS}	NC	V_{SS}	DQP2	DQ16-9
E	DQ24-17	DQ24-17	V_{SS}	CE1#	V_{SS}	DQ16-9	DQ16-9
F	V_{DDQ}	DQ24-17	V_{SS}	OE#	V_{SS}	DQ16-9	V_{DDQ}
G	DQ24-17	DQ24-17	BW3#	ADV#	BW2#	DQ16-9	DQ16-9
H	DQ24-17	DQ24-17	V_{SS}	GW#	V_{SS}	DQ16-9	DQ16-9
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQ32-25	DQ32-25	V_{SS}	CLK	V_{SS}	DQ8-1	DQ8-1
L	DQ32-25	DQ32-25	BW4#	NC	BW1#	DQ8-1	DQ8-1
M	V_{DDQ}	DQ32-25	V_{SS}	BWE#	V_{SS}	DQ8-1	V_{DDQ}
N	DQ32-25	DQ32-25	V_{SS}	A1	V_{SS}	DQ8-1	DQ8-1
P	DQ32-25	DQP4	V_{SS}	A0	V_{SS}	DQP1	DQ8-1
R	NC	A17-2	LBO#	V_{DD}	NC	A17-2	NC
T	NC	NC	A17-2	A17-2	A17-2	NC	ZZ
U	V_{DDQ}	NC	NC	NC	NC	NC	V_{DDQ}



119-Pin BGA (Top View)