MC74VHC244

Octal Bus Buffer

The MC74VHC244 is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology.

The MC74VHC244 is a noninverting 3–state buffer, and has two active–low output enables. This device is designed to be used with 3–state memory address drivers, etc.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7 V, allowing the interface of 5 V systems to 3 V systems.

- High Speed: t_{PD} = 3.9 ns (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 4 μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 5.5 V Operating Range
- Low Noise: V_{OLP} = 0.9 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 136 FETs

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

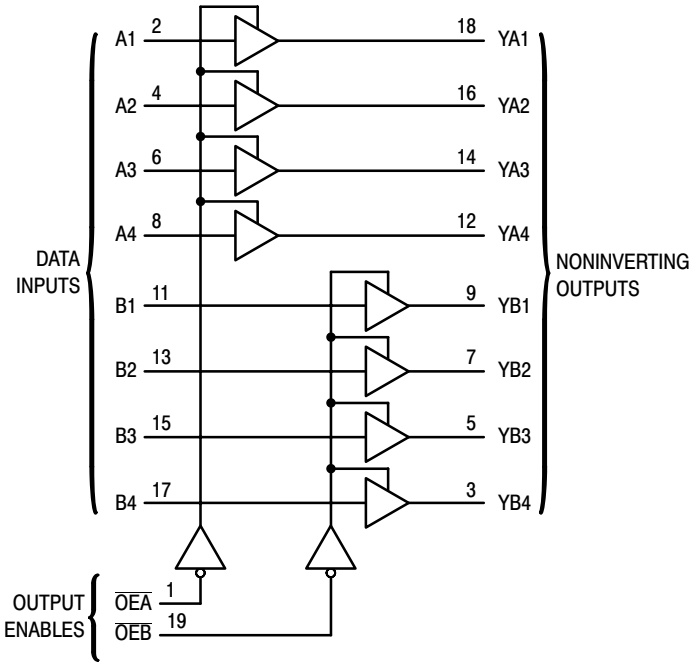

Figure 1. LOGIC DIAGRAM

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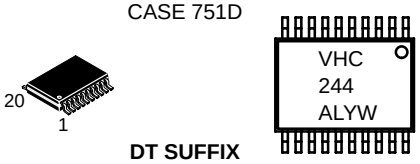
DEVICE MARKING

DW SUFFIX
20–LEAD SOIC WIDE PACKAGE
CASE 751D

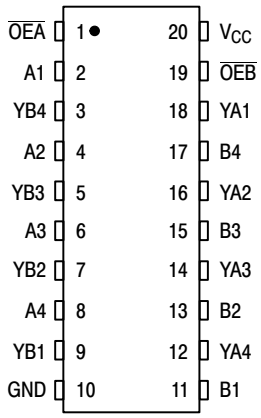


DT SUFFIX
20–LEAD TSSOP PACKAGE
CASE 948E

M SUFFIX
20–LEAD SOIC EIAJ PACKAGE
CASE 967

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information in the Ordering Information Table on page 3 of this data sheet.

MAXIMUM RATINGS (Note 1)

Symbol	Parameter		Value	Unit
V_{CC}	Positive DC Supply Voltage		–0.5 to +7.0	V
V_{IN}	Digital Input Voltage		–0.5 to +7.0	V
V_{OUT}	DC Output Voltage		–0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current		–20	mA
I_{OK}	Output Diode Current		±20	mA
I_{OUT}	DC Output Current, per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±75	mA
P_D	Power Dissipation in Still Air	SOIC Package TSSOP	500 450	mW
T_{STG}	Storage Temperature Range		–65 to +150	°C
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	>2000 >200 >2000	V
$I_{LATCH–UP}$	Latch–Up Performance	Above V_{CC} and Below GND at 125°C (Note 5)	±300	mA
θ_{JA}	Thermal Resistance, Junction to Ambient	SOIC Package TSSOP	96 128	°C/W

1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
2. Tested to EIA/JESD22–A114–A
3. Tested to EIA/JESD22–A115–A
4. Tested to JESD22–C101–A
5. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{IN}	DC Input Voltage		0	5.5	V
V_{OUT}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature Range, all Package Types		–55	125	°C
t_r, t_f	Input Rise or Fall Time	V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	0	100 20	ns/V

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

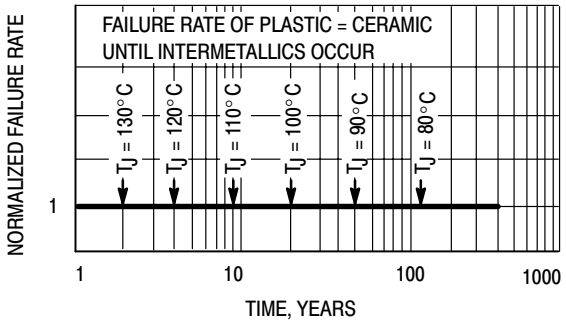


Figure 2. Failure Rate vs. Time Junction Temperature

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	$-55°C \le T_A \le 125°C$ Min	$-55°C \le T_A \le 125°C$ Max	Unit
V_{IH}	Minimum High–Level Input Voltage		2.0	1.5			1.5	1.5	1.5		V
			3.0 to 5.5	V_{CCX} 0.7			V_{CCX} 0.7	V_{CCX} 0.7	V_{CCX} 0.7		
V_{IL}	Maximum Low–Level Input Voltage		2.0			0.5		0.5		0.5	V
			3.0 to 5.5			V_{CCX} 0.3		V_{CCX} 0.3		V_{CCX} 0.3	
V_{OH}	Maximum High–Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OH} = –50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		V_{IN} = V_{IH} or V_{IL} I_{OH} = –4 mA I_{OH} = –8 mA	3.0 4.5	2.58 3.94			2.48 3.8		2.34 3.66		
V_{OL}	Maximum Low–Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OL} = 50 μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{IN} = V_{IH} or V_{IL} I_{OH} = 4 mA I_{OH} = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{OZ}	Maximum 3–State Leakage Current	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND	5.5			±0.25		±2.5		±2.5	μA
I_{CC}	Maximum Quiescent Supply Current (per package)	V_{IN} = V_{CC} or GND	5.5			4.0		40.0		40.0	μA

ORDERING INFORMATION

Device	Package	Shipping
MC74VHC244DW	SOIC WIDE	38 Units/Rail
MC74VHC244DWR2	SOIC WIDE	1000/Tape & Reel
MC74VHC244DT	TSSOP	75 Units/Rail
MC74VHC244DTR2	TSSOP	2500/Tape & Reel
MC74VHC244M	SOIC EIAJ	1600 Units/Box
MC74VHC244MEL	SOIC EIAJ	2000/Tape & Reel

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OEA}$, $\overline{OEB}$	A, B	YA, YB
L	L	L
L	H	H
H	X	Z

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Conditions	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	$-55°C \le T_A \le 125°C$ Min	$-55°C \le T_A \le 125°C$ Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to YA or B to YB	$V_{CC} = 3.3 \pm 0.3V$ $C_L = 15pF$		5.8	8.4	1.0	10.0	1.0	11.0	ns
		$V_{CC} = 3.3 \pm 0.3V$ $C_L = 50pF$		8.3	11.9	1.0	13.5	1.0	14.5	
		$V_{CC} = 5.0 \pm 0.5V$ $C_L = 15pF$		3.9	5.5	1.0	6.5	1.0	7.5	
		$V_{CC} = 5.0 \pm 0.5V$ $C_L = 50pF$		5.4	7.5	1.0	8.5	1.0	9.5	
t_{PZL}, t_{PZH}	Output Enable Time $\overline{OEA}$ to YA or $\overline{OEB}$ to YB	$V_{CC} = 3.3 \pm 0.3V$ $R_L = 1k\Omega$ $C_L = 15pF$		6.6	10.6	1.0	12.5	1.0	13.5	ns
		$V_{CC} = 3.3 \pm 0.3V$ $R_L = 1k\Omega$ $C_L = 50pF$		9.1	14.1	1.0	16.0	1.0	17.0	
		$V_{CC} = 5.0 \pm 0.5V$ $R_L = 1k\Omega$ $C_L = 15pF$		4.7	7.3	1.0	8.5	1.0	9.5	
		$V_{CC} = 5.0 \pm 0.5V$ $R_L = 1k\Omega$ $C_L = 50pF$		6.2	9.3	1.0	10.5	1.0	11.5	
t_{PLZ}, t_{PHZ}	Output Disable Time $\overline{OEA}$ to YA or $\overline{OEB}$ to YB	$V_{CC} = 3.3 \pm 0.3V$ $R_L = 1k\Omega$ $C_L = 50pF$		10.3	14.0	1.0	16.0	1.0	17.0	ns
		$V_{CC} = 5.0 \pm 0.5V$ $R_L = 1k\Omega$ $C_L = 50pF$		6.7	9.2	1.0	10.5	1.0	11.5	
t_{OSLH}, t_{OSHL}	Output to Output Skew	$V_{CC} = 3.3 \pm 0.3V$ $C_L = 50pF$ (Note 6)			1.5		1.5		1.5	ns
		$V_{CC} = 5.0 \pm 0.5V$ $C_L = 50pF$ (Note 6)			1.0		1.0		1.5	
C_{in}	Maximum Input Capacitance			4	10		10		10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)			6						pF

		Typical @ 25°C, $V_{CC} = 5.0V$	
C_{PD}	Power Dissipation Capacitance (Note 7)	19	pF

6. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per bit). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns, $C_L = 50$pF, $V_{CC} = 5.0$ V)

Symbol	Parameter	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.6	0.9	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.6	– 0.9	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

SWITCHING WAVEFORMS

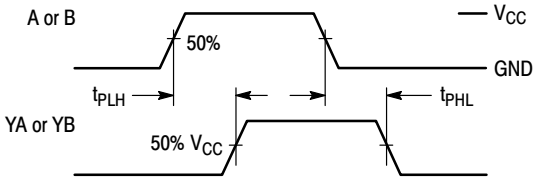


Figure 3.

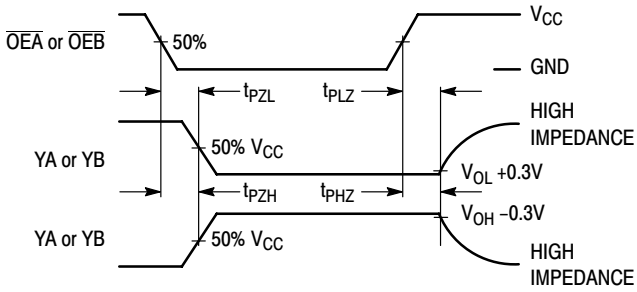
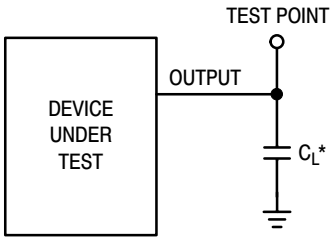


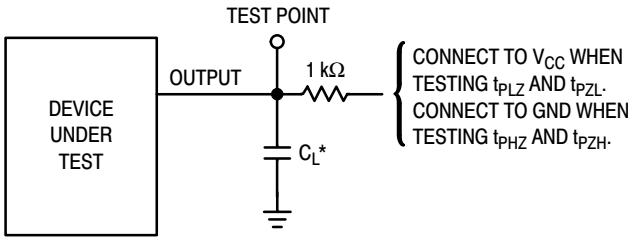
Figure 4.

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 5. Test Circuit



*Includes all probe and jig capacitance

Figure 6. Test Circuit

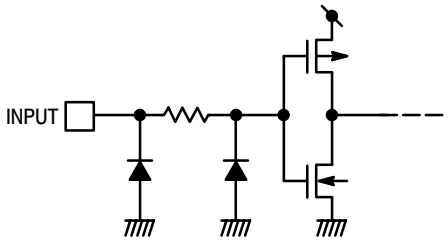
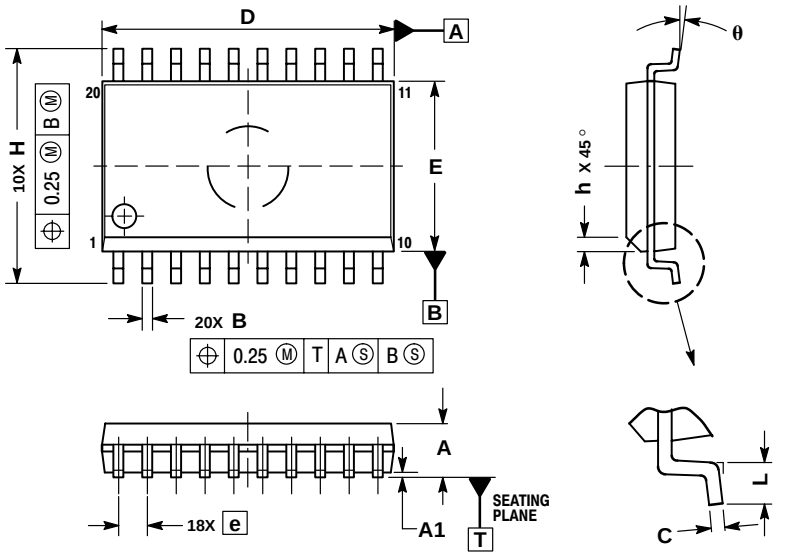


Figure 7. Input Equivalent Circuit

OUTLINE DIMENSIONS

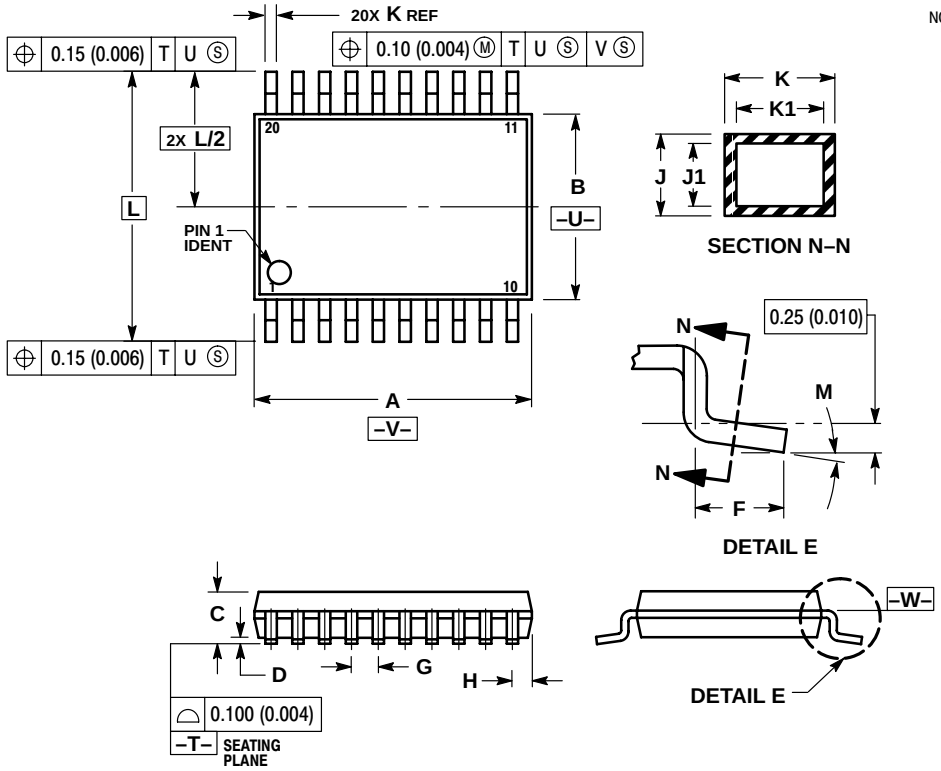
DW SUFFIX
SOIC
CASE 751D–05
ISSUE F



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

DT SUFFIX
TSSOP
CASE 948E–02
ISSUE A

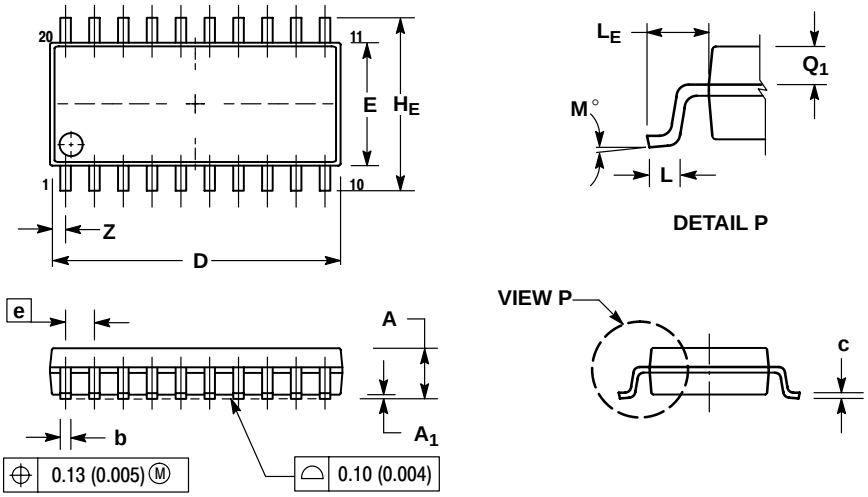


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

OUTLINE DIMENSIONS

M SUFFIX
SOIC EIAJ
CASE 967–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
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