

MC74LVX139

Dual 2-to-4 Decoder/ Demultiplexer

The MC74LVX139 is an advanced high speed CMOS 2-to-4 decoder/ demultiplexer fabricated with silicon gate CMOS technology.

When the device is enabled ($\overline{E}$ = low), it can be used for gating or as a data input for demultiplexing operations. When the enable input is held high, all four outputs are fixed high, independent of other inputs.

The inputs tolerate voltages up to 7 V, allowing the interface of 5 V systems to 3 V systems.

- High Speed: t_{PD} = 6.0 ns (Typ) at V_{CC} = 3.3 V
- Low Power Dissipation: I_{CC} = 4 μ A (Max) at T_A = 25°C
- High Noise Immunity: V_{NIH} = V_{NIL} = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 3.6 V Operating Range
- Low Noise: V_{OLP} = 0.5 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 100 FETs or 25 Equivalent Gates

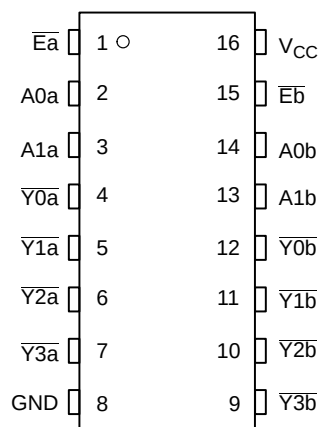


Figure 1. Pin Assignment

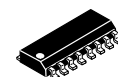
FUNCTION TABLE

Inputs		Outputs				
$\overline{E}$	A1 A0	Y0	Y1	Y2	Y3	
H	X X	H	H	H	H	
L	L L	L	H	H	H	
L	L H	H	L	H	H	
L	H L	H	H	L	H	
L	H H	H	H	H	L	



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SOIC-16
D SUFFIX
CASE 751B

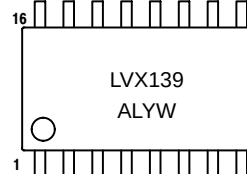
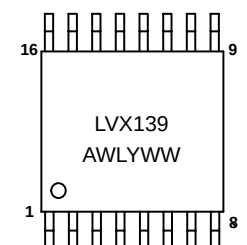


TSSOP-16
DT SUFFIX
CASE 948F



SOIC EIAJ-16
M SUFFIX
CASE 966

MARKING DIAGRAMS



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC74LVX139D	SO-16	48 Units/Rail
MC74LVX139DR2	SO-16	2500 Units/Reel
MC74LVX139DT	TSSOP-16	96 Units/Rail
MC74LVX139DTR2	TSSOP-16	2000 Units/Reel
MC74LVX139M	SO EIAJ-16	48 Units/Rail
MC74LVX139MEL	SO EIAJ-16	2000 Units/Reel

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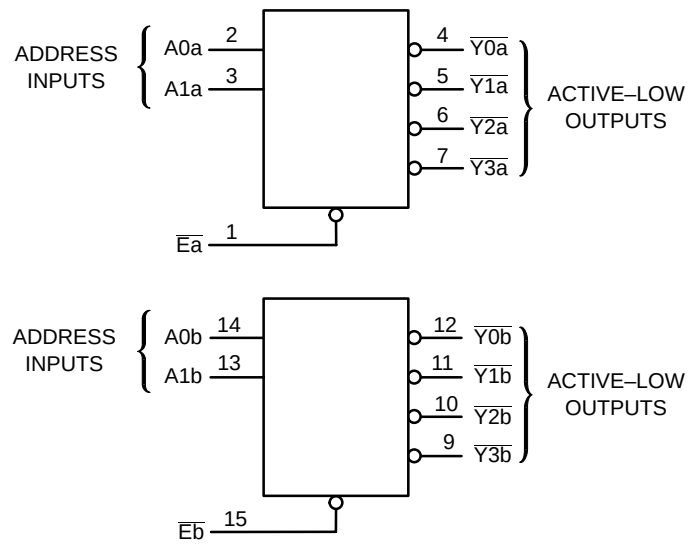


Figure 2. Logic Diagram

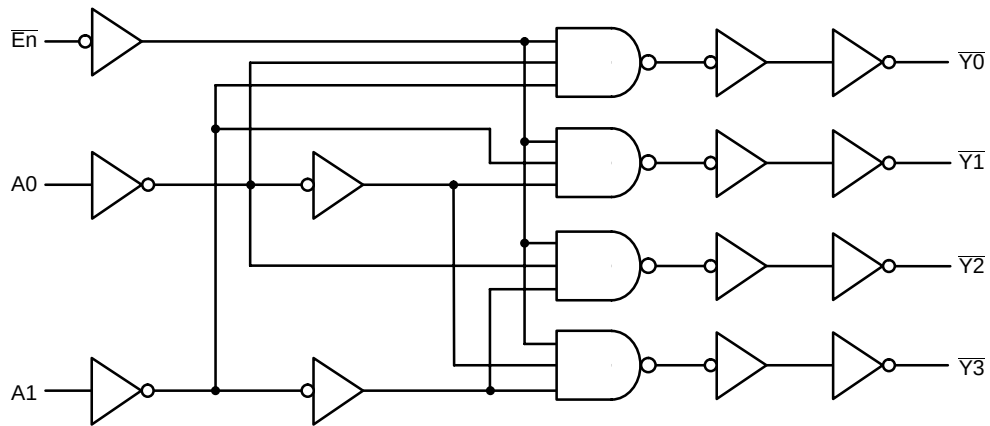


Figure 3. Expanded Logic Diagram
(1/2 of Device)

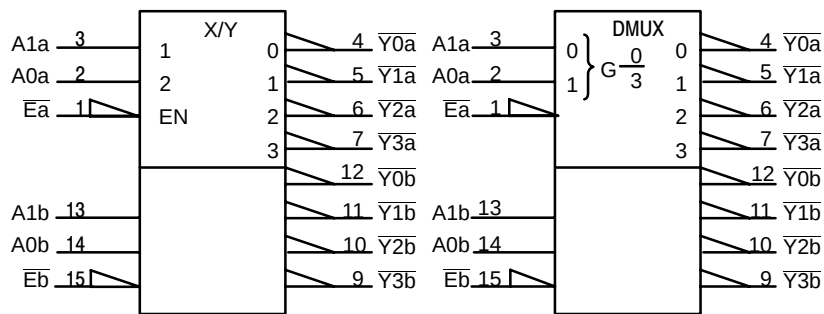


Figure 4. IEC Logic Diagram

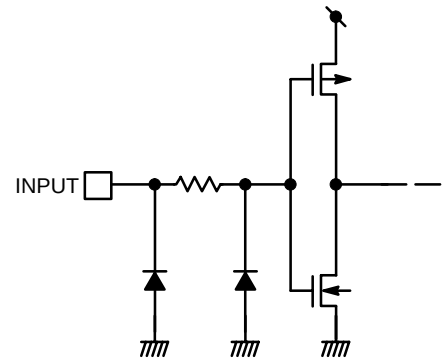


Figure 5. Input Equivalent Circuit

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MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Value	Unit
V _{CC}	Positive DC Supply Voltage	−0.5 to +7.0	V
V _{IN}	Digital Input Voltage	−0.5 to +7.0	V
V _{OUT}	DC Output Voltage	−0.5 to V _{CC} +0.5	V
I _{IK}	Input Diode Current	−20	mA
I _{OK}	Output Diode Current	± 20	mA
I _{OUT}	DC Output Current, per Pin	± 25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 75	mA
P _D	Power Dissipation in Still Air SOIC Package TSSOP	200 180	mW
T _{STG}	Storage Temperature Range	−65 to +150	°C
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 2.) Machine Model (Note 3.) Charged Device Model (Note 4.)	>2000 >200 >2000	V
I _{LATCH-UP}	Latch-Up Performance Above V _{CC} and Below GND at 125°C (Note 5.)	± 300	mA
θ _{JA}	Thermal Resistance, Junction to Ambient SOIC Package TSSOP	143 164	°C/W

1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
2. Tested to EIA/JESD22–A114–A
3. Tested to EIA/JESD22–A115–A
4. Tested to JESD22–C101–A
5. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
V _{CC}	DC Supply Voltage	2.0	3.6	V
V _{IN}	DC Input Voltage	0	5.5	V
V _{OUT}	DC Output Voltage Output in 3–State High or Low State	0	V _{CC}	V
T _A	Operating Temperature Range, all Package Types	−40	85	°C
t _r , t _f	Input Rise or Fall Time V _{CC} = 5.0 V ± 0.5 V	0	100	ns/V

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DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	Minimum High-Level Input Voltage		2.0 3.0 3.6	0.75 V _{CC} 0.7 V _{CC} 0.7 V _{CC}			0.75 V _{CC} 0.7 V _{CC} 0.7 V _{CC}		V
V _{IL}	Maximum Low-Level Input Voltage		2.0 3.0 3.6			0.25 V _{CC} 0.3 V _{CC} 0.3 V _{CC}		0.25 V _{CC} 0.3 V _{CC} 0.3 V _{CC}	V
V _{OH}	High-Level Output Voltage	I _{OH} = -50 μA I _{OH} = -50 μA I _{OH} = -4 mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0 3.0		1.9 2.9 2.48		V
V _{OL}	Low-Level Output Voltage	I _{OL} = 50 μA I _{OH} = 50 μA I _{OH} = 4 mA	2.0 3.0 3.0		0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I _{IN}	Input Leakage Current	V _{IN} = 5.5 V or GND	0 to 3.6			±0.1		±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per package)	V _{IN} = V _{CC} or GND	3.6	1.0	1.0	2.0			μA

AC ELECTRICAL CHARACTERISTICS Input t_r = t_f = 3.0 ns

Symbol	Parameter	Test Conditions	T _A = 25°C			-40°C ≤ T _A ≤ 85°C		Unit
			Min	Typ	Max	Min	Max	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, A to Y	V _{CC} = 2.7 V C _L = 15 pF C _L = 50 pF		8.5 11.0	15.0 16.5	1.0 1.0	17.8 18.0	ns
		V _{CC} = 3.3 V ± 0.3 V C _L = 15 pF C _L = 50 pF		6.0 8.5	10.0 13.0	1.0 1.0	12.0 15.0	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, E to Y	V _{CC} = 2.7 V C _L = 15 pF C _L = 50 pF		8.0 10.0	13.0 16.5	1.0 1.0	15.5 18.0	ns
		V _{CC} = 3.3 V ± 0.3 V C _L = 15 pF C _L = 50 pF		5.5 7.5	8.2 13.0	1.0 1.0	10.0 15.0	
C _{IN}	Maximum Input Capacitance			4	10		10	pF

C _{PD}	Power Dissipation Capacitance (Note 6.)	Typical @ 25°C, V _{CC} = 3.3 V	pF
		26	

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/2 (per decoder). C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

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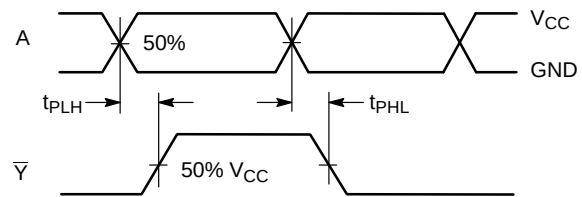


Figure 6. Switching Waveform

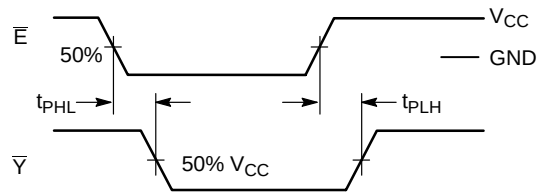
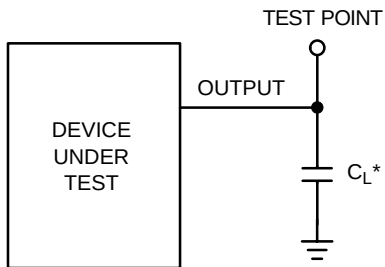
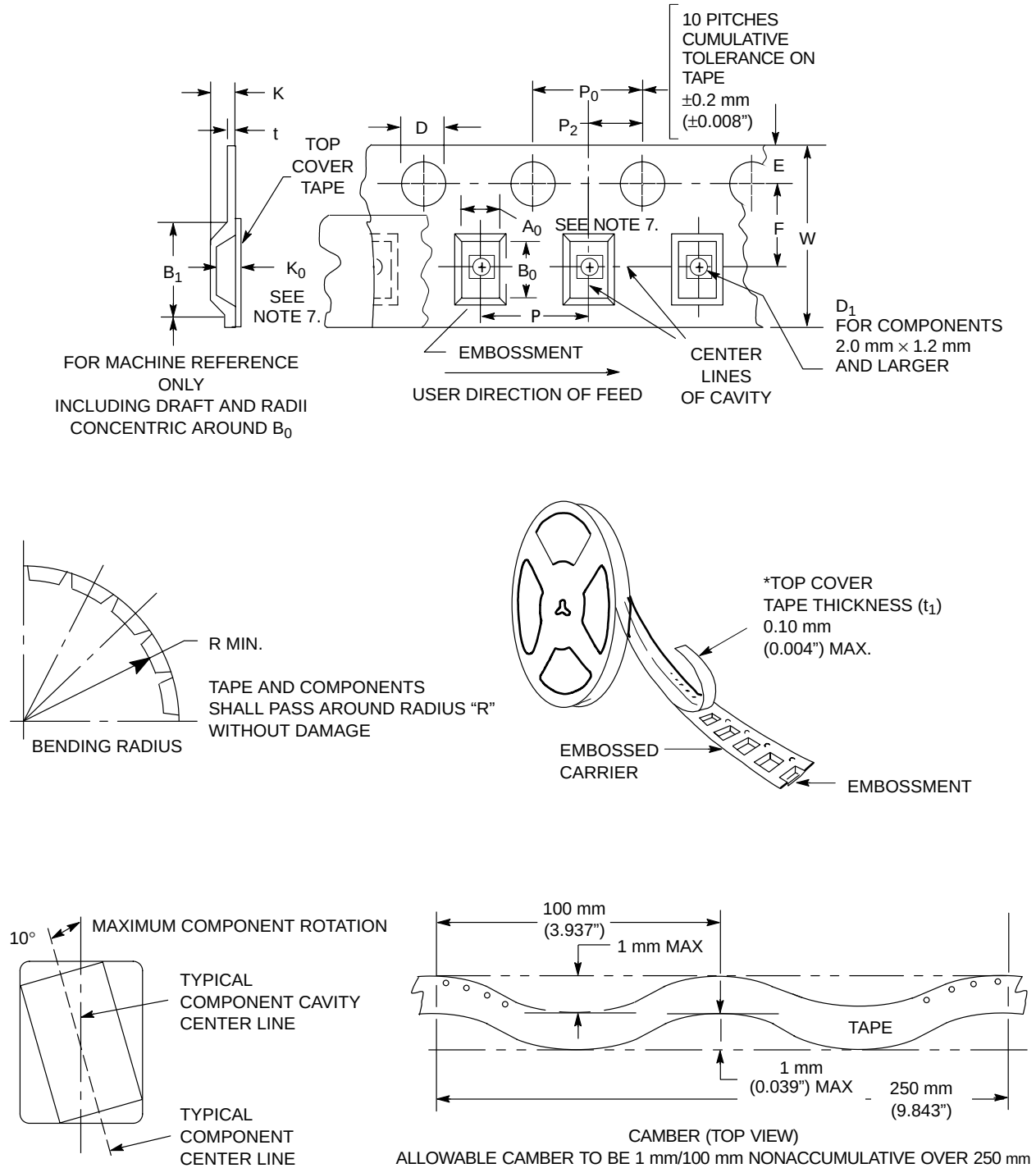


Figure 7. Switching Waveform



*Includes all probe and jig capacitance

Figure 8. Test Circuit



7. A_0 , B_0 , and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

Figure 9. Carrier Tape Specifications

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EMBOSSED CARRIER DIMENSIONS (See Notes 8. and 9.)

Tape Size	B ₁ Max	D	D ₁	E	F	K	P	P ₀	P ₂	R	T	W
8 mm	4.35 mm (0.179")	1.5 mm + 0.1 -0.0 (0.059" +0.004 -0.0)	1.0 mm Min (0.179")	1.75 mm ±0.1 (0.069 ±0.004")	3.5 mm ±0.5 (1.38 ±0.002")	2.4 mm Max (0.094")	4.0 mm ±0.10 (0.157 ±0.004")	4.0 mm ±0.1 (0.157 ±0.004")	2.0 mm ±0.1 (0.079 ±0.004")	25 mm (0.98")	0.6 mm (0.024)	8.3 mm (0.327)
12 mm	8.2 mm (0.323")		1.5 mm Min (0.060)		5.5 mm ±0.5 (0.217 ±0.002")	6.4 mm Max (0.252")	4.0 mm ±0.10 (0.157 ±0.004") 8.0 mm ±0.10 (0.315 ±0.004")			30 mm (1.18")		12.0 mm ±0.3 (0.470 ±0.012")
16 mm	12.1 mm (0.476")				7.5 mm ±0.10 (0.295 ±0.004")	7.9 mm Max (0.311")	4.0 mm ±0.10 (0.157 ±0.004") 8.0 mm ±0.10 (0.315 ±0.004") 12.0 mm ±0.10 (0.472 ±0.004")					16.3 mm (0.642)
24 mm	20.1 mm (0.791")				11.5 mm ±0.10 (0.453 ±0.004")	11.9 mm Max (0.468")	16.0 mm ±0.10 (0.63 ±0.004")					24.3 mm (0.957)

8. Metric Dimensions Govern—English are in parentheses for reference only.

9. A₀, B₀, and K₀ are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

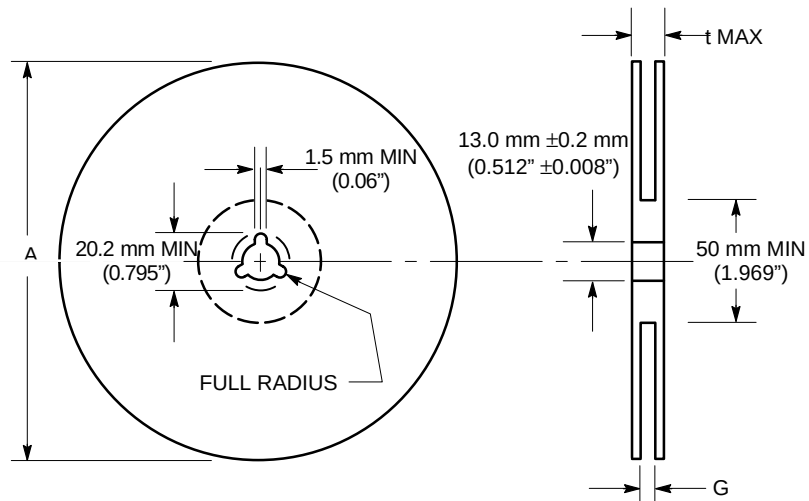


Figure 10. Reel Dimensions

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REEL DIMENSIONS

Tape Size	T&R Suffix	A Max	G	t Max
8 mm	T1, T2	178 mm (7")	8.4 mm, +1.5 mm, -0.0 (0.33" + 0.059", -0.00)	14.4 mm (0.56")
8 mm	T3, T4	330 mm (13")	8.4 mm, +1.5 mm, -0.0 (0.33" + 0.059", -0.00)	14.4 mm (0.56")
12 mm	R2	330 mm (13")	12.4 mm, +2.0 mm, -0.0 (0.49" + 0.079", -0.00)	18.4 mm (0.72")
16 mm	R2	360 mm (14.173")	16.4 mm, +2.0 mm, -0.0 (0.646" + 0.078", -0.00)	22.4 mm (0.882")
24 mm	R2	360 mm (14.173")	24.4 mm, +2.0 mm, -0.0 (0.961" + 0.078", -0.00)	30.4 mm (1.197")

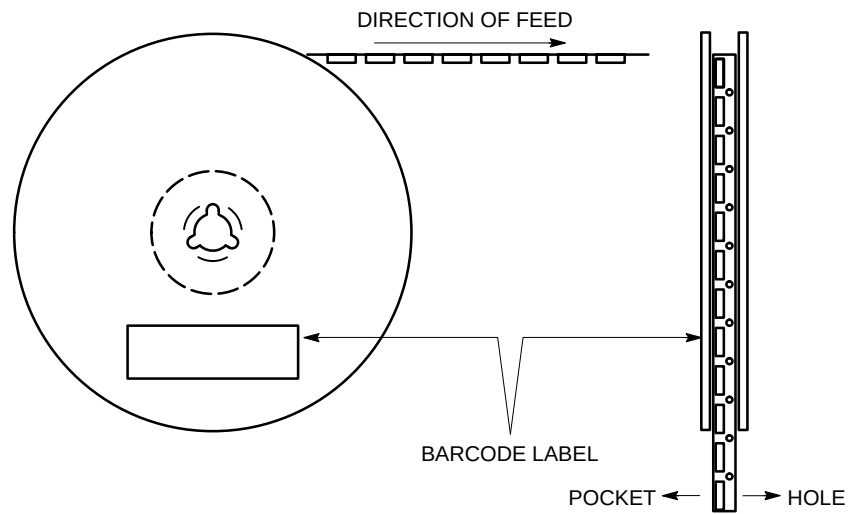


Figure 11. Reel Winding Direction

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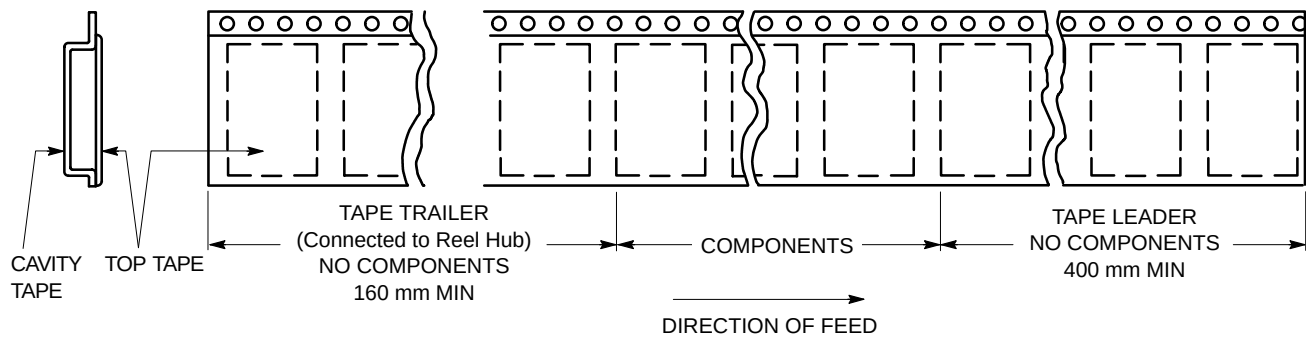


Figure 12. Tape Ends for Finished Goods

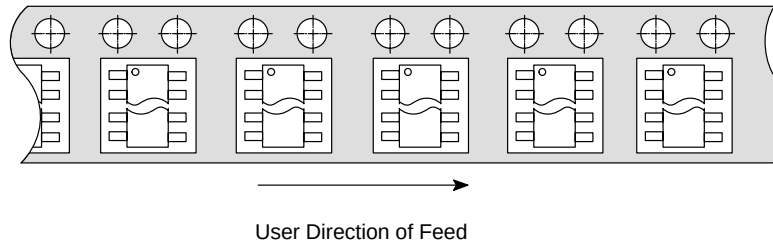


Figure 13. TSSOP and SOIC R2 Reel Configuration/Orientation

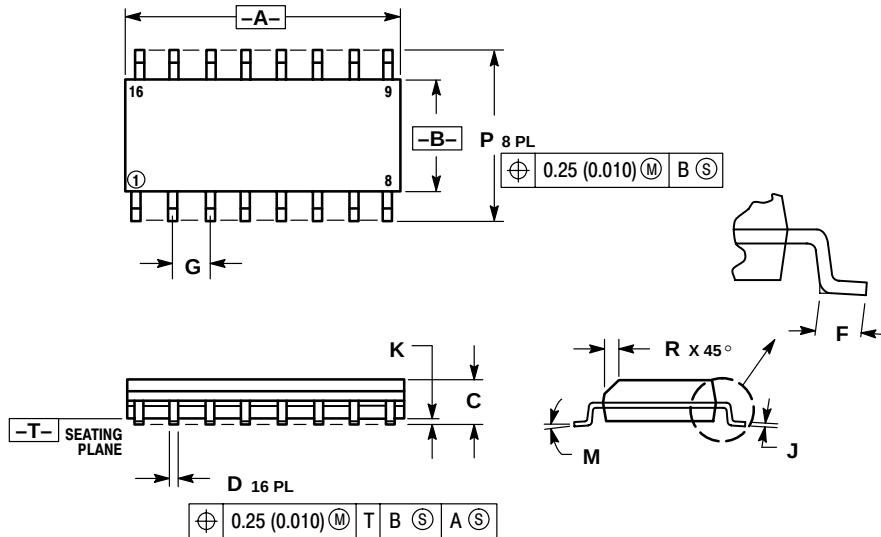
TAPE UTILIZATION BY PACKAGE

Tape Size	SOIC	TSSOP	QFN	SC88A / SOT-353 SC88/SOT-363
8 mm				5-, 6-Lead
12 mm	8-Lead	8-, 14-, 16-Lead	8-, 14-, 16-Lead	
16 mm	14-, 16-Lead	20-, 24-Lead	20-, 24-Lead	
24 mm	18-, 20-, 24-, 28-Lead	48-, 56-Lead	48-, 56-Lead	

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PACKAGE DIMENSIONS

SOIC-16
D SUFFIX
CASE 751B-05
ISSUE J



NOTES:

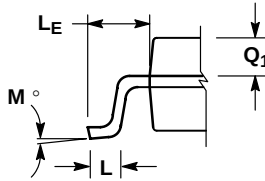
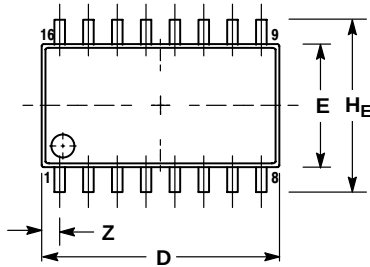
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2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

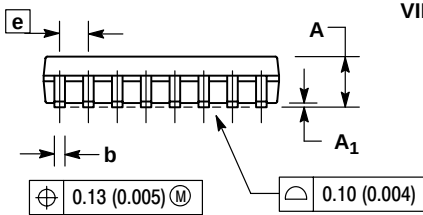
MC74LVX139

PACKAGE DIMENSIONS

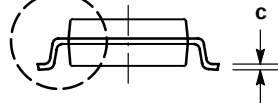
SOIC EIAJ-16
M SUFFIX
CASE 966-01
ISSUE O



DETAIL P



VIEW P



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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