

MC74LVX132

Product Preview

Quad 2-Input NAND Schmitt Trigger

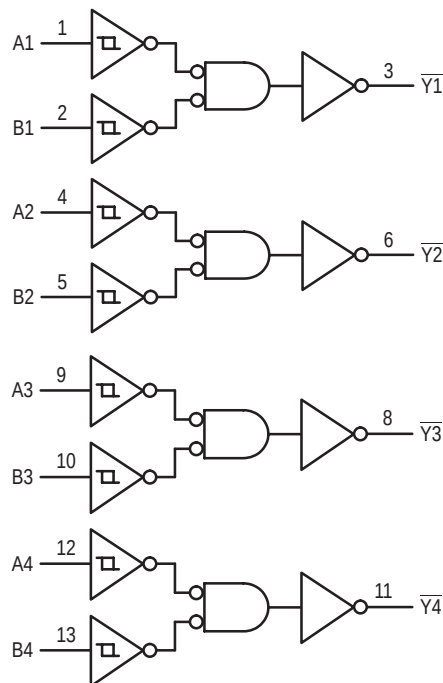
The MC74LVX132 is an advanced high speed CMOS Schmitt NAND trigger fabricated with silicon gate CMOS technology.

Pin configuration and function are the same as the MC74LVX00, but the inputs have hysteresis and, with its Schmitt trigger function, the LVX132 can be used as a line receiver which will receive slow input signals.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: $t_{PD} = 5.8\text{ns}$ (Typ) at $V_{CC} = 3.3\text{V}$
- Low Power Dissipation: $I_{CC} = 2\mu\text{A}$ (Max) at $T_A = 25^\circ\text{C}$
- Power Down Protection Provided on Inputs
- Low Noise: $V_{OLP} = 0.5\text{V}$ (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V

LOGIC DIAGRAM

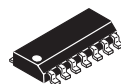


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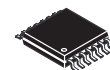


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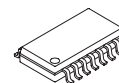
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14-LEAD SOIC
D SUFFIX
CASE 751A

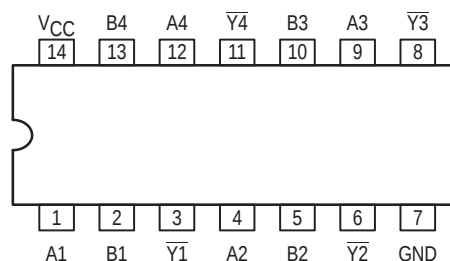


14-LEAD TSSOP
DT SUFFIX
CASE 948G



14-LEAD SOIC EIAJ
M SUFFIX
CASE 965

PIN CONNECTION AND
MARKING DIAGRAM (Top View)



For detailed package marking information, see the Marking Diagram section on page 5 of this data sheet.

ORDERING INFORMATION

Device	Package	Shipping
MC74LVX132D	SOIC	55 Units/Rail
MC74LVX132DT	TSSOP	96 Units/Rail
MC74LVX132M	SOIC EIAJ	50 Units/Rail

FUNCTION TABLE

A Input	B Input	$\bar{Y}$ Output
L	L	H
L	H	H
H	L	H
H	H	L

MC74LVX132

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V _{in}	DC Input Voltage	– 0.5 to + 7.0	V
V _{out}	DC Output Voltage	– 0.5 to V _{CC} + 0.5	V
I _{IK}	Input Diode Current	– 20	mA
I _{OK}	Output Diode Current	± 20	mA
I _{out}	DC Output Current, per Pin	± 25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 50	mA
P _D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T _{stg}	Storage Temperature	– 65 to + 150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	2.0	3.6	V
V _{in}	DC Input Voltage	0	5.5	V
V _{out}	DC Output Voltage	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	– 40	+ 125	°C

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} V	T _A = 25°C			T _A = ≤ 85°C		T _A = ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{T+}	Positive Threshold Voltage (3)		2.0	1.15	1.31	1.60	1.15	1.60	1.15	1.60	V
			3.0	1.50	1.82	2.25	1.50	2.25	1.50	2.25	
			3.6	1.70	2.12	2.60	1.70	2.60	1.70	2.60	
V _{T–}	Negative Threshold Voltage (3)		2.0	0.30	0.64	0.9	0.30	0.90	0.30	0.90	V
			3.0	0.75	1.13	1.45	0.75	1.45	0.75	1.45	
			3.6	1.00	1.46	1.90	1.00	1.90	1.00	1.90	
V _H	Hysteresis Voltage (3)		2.0	0.30	0.70	1.30	0.30	1.30	0.30	1.30	V
			3.0	0.30	0.76	1.50	0.30	1.50	0.30	1.50	
			3.6	0.35	0.69	1.60	0.35	1.60	0.35	1.60	
V _{OH}	Minimum High-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	I _{OH} = – 50μA I _{OH} = – 50μA I _{OH} = – 4mA	2.0	1.9	2.0		1.9		1.9		V
			3.0	2.9	3.0		2.9		2.9		
			3.0	2.58			2.48		2.34		
V _{OL}	Maximum Low-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50μA I _{OL} = 50μA I _{OL} = 4mA	2.0		0.0	0.1		0.1		0.1	V
			3.0		0.0	0.1		0.1		0.1	
			3.0			0.36		0.44		0.52	
I _{in}	Maximum Input Leakage Current	V _{in} = 5.5V or GND	3.6			± 0.1		± 1.0		± 1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{in} = V _{CC} or GND	3.6			2.0		20		20	μA

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A = \leq 85^\circ\text{C}$		$T_A = \leq 125^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, A or B to $\bar{Y}$	$V_{CC} = 2.7\text{V}$ $C_L = 15\text{pF}$		7.0	11.0	1.0	13.0	1.0	15.0	ns
		$C_L = 50\text{pF}$		10.0	16.0	1.0	18.7	1.0	20.0	
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$		5.8	10.6	1.0	12.5	1.0	14.5	
		$C_L = 50\text{pF}$		8.3	15.4	1.0	17.5	1.0	19.5	
t_{OSHL} , t_{OSLH}	Output to Output Skew (Note 1.)	$V_{CC} = 2.7\text{V}$ $C_L = 50\text{pF}$			1.5		1.5		1.5	ns
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 50\text{pF}$			1.5		1.5		1.5	
C_{in}	Maximum Input Capacitance			4	10		10		10	pF

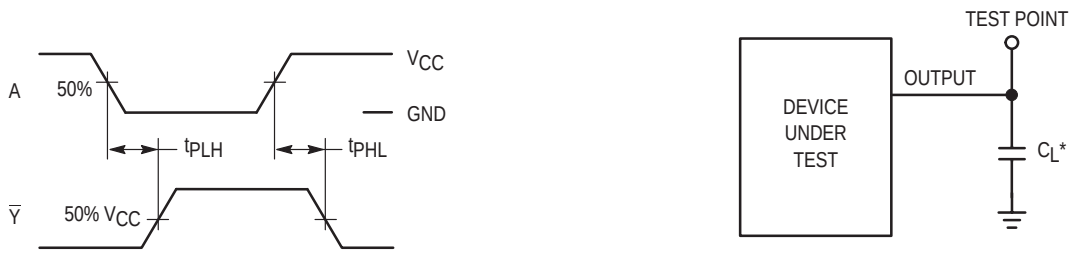
C _{PD}	Power Dissipation Capacitance (Note 1.)	Typical @ 25°C, V _{CC} = 5.0 V		pF
		11		

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/4$ (per gate). C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$, $C_L = 50\text{pF}$, $V_{CC} = 5.0\text{V}$)

Symbol	Characteristic	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.5	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	-0.3	-0.5	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

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*Includes all probe and jig capacitance

Figure 1. Switching Waveforms

Figure 2. Test Circuit

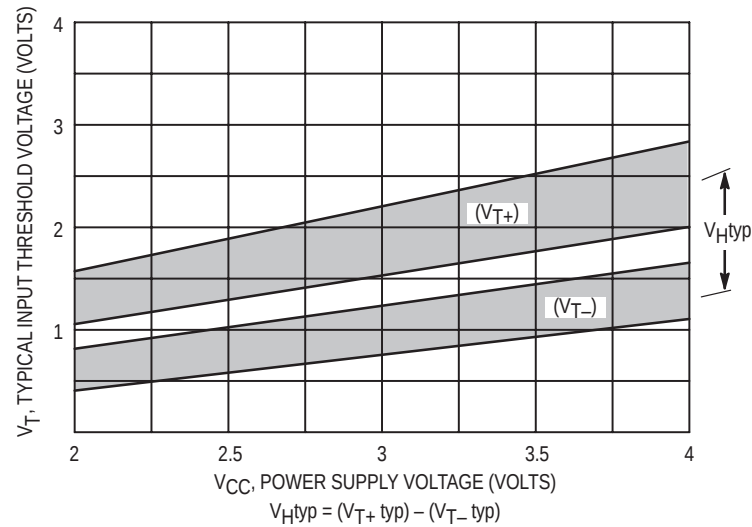
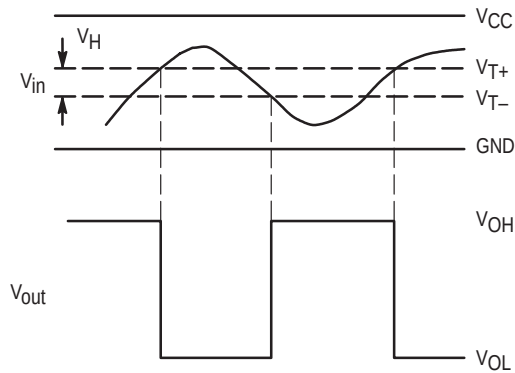


Figure 3. Typical Input Threshold, V_{T+}, V_{T-} versus Power Supply Voltage

(a) A Schmitt-Trigger Squares Up Inputs With Slow Rise and Fall Times



(b) A Schmitt-Trigger Offers Maximum Noise Immunity

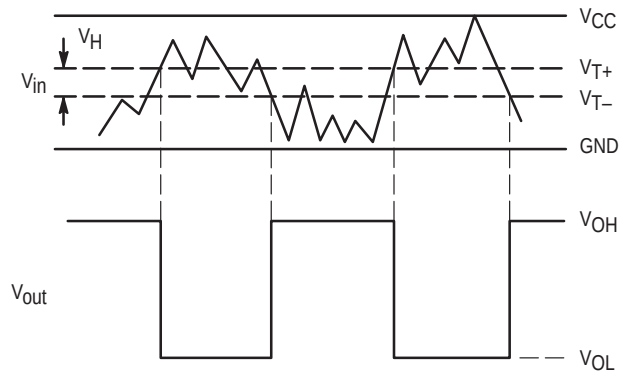


Figure 4. Typical Schmitt-Trigger Applications

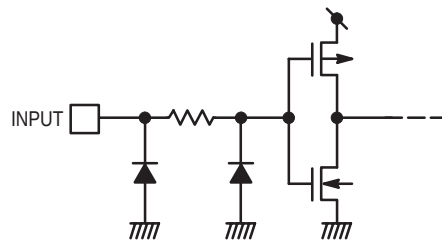
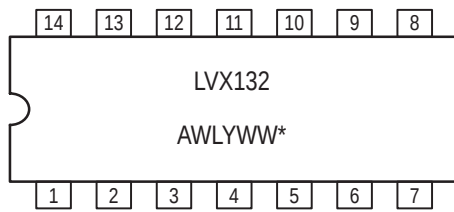


Figure 5. Input Equivalent Circuit

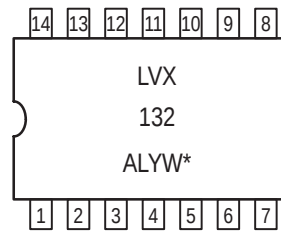
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MARKING DIAGRAMS

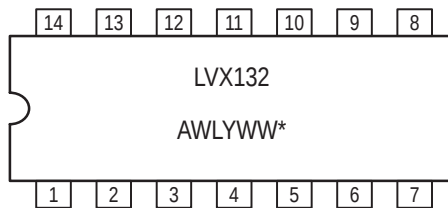
(Top View)



14-LEAD SOIC
D SUFFIX
CASE 751A



14-LEAD TSSOP
DT SUFFIX
CASE 948G



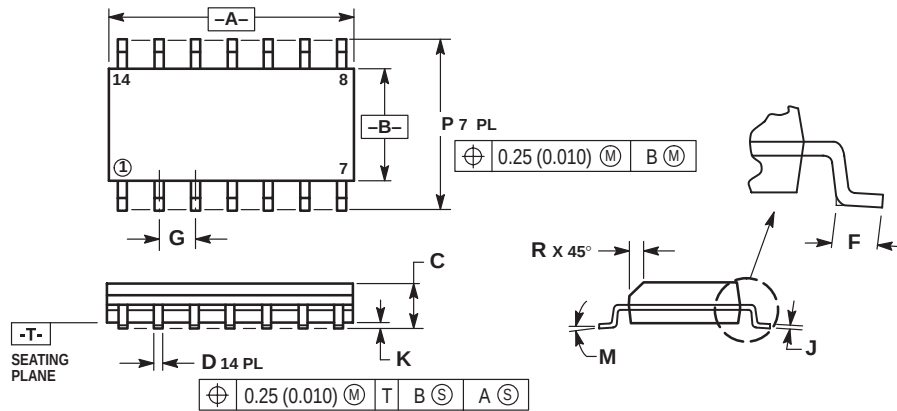
14-LEAD SOIC EIAJ
M SUFFIX
CASE 965

*See Applications Note #AND8004/D for date code and traceability information.

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PACKAGE DIMENSIONS

D SUFFIX PLASTIC SOIC PACKAGE CASE 751A-03 ISSUE F

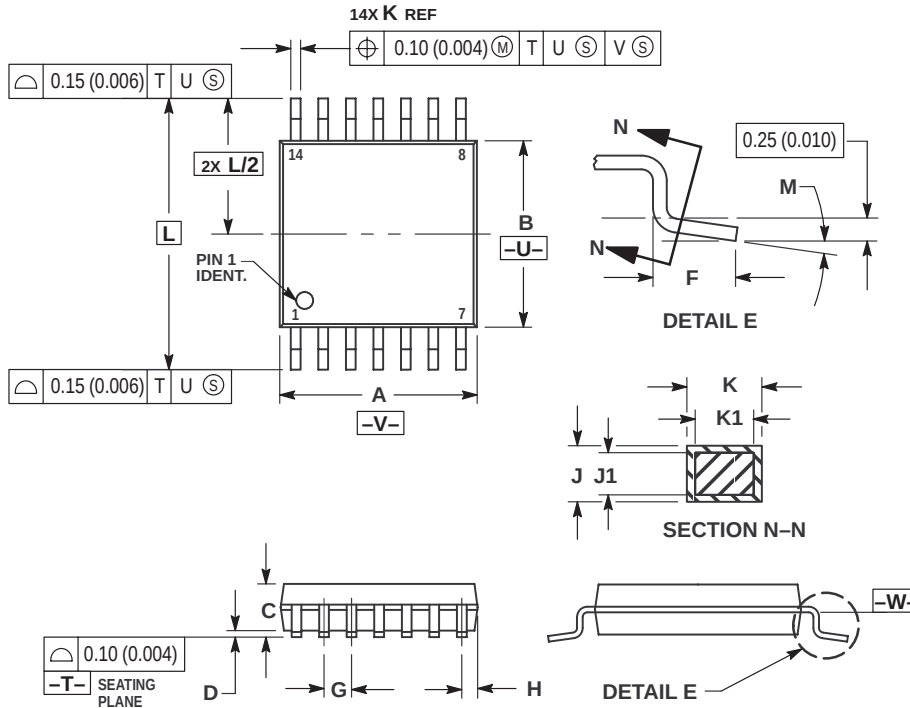


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

DT SUFFIX PLASTIC TSSOP PACKAGE CASE 948G-01 ISSUE O



NOTES:

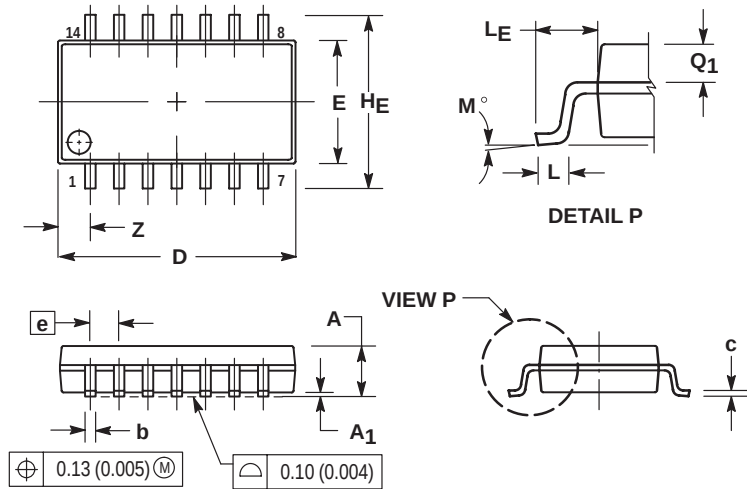
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
K	0.09	0.16	0.004	0.006
K1	0.19	0.30	0.007	0.012
L	0.19	0.25	0.007	0.010
M	6.40 BSC		0.252 BSC	
N	0°	8°	0°	8°

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PACKAGE DIMENSIONS

M SUFFIX
PLASTIC SOIC EIAJ PACKAGE
CASE 965-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	2.05	—	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q ₁	0.70	0.90	0.028	0.035
Z	—	1.42	—	0.056

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